Low Noise, Matched Dual Monolithic Transistor

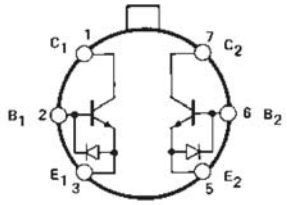
Preliminary Technical Data

MAT12

FEATURES

Low offset voltage (V_{OS}): 50 µV max
Very Low Voltage Noise: 1nV/√Hz max @ 100Hz
High Gain (h_{FE}):
  500 min at I_C = 1mA
  300 min at I_C = 1µA
Excellent Log Conformance: r_{BE} = 0.3 Ω
Low Offset Voltage Drift: 0.1 µV/°C max
High Gain Bandwidth Product: 200MHz

PIN CONFIGURATION



Note: Substrate is connected to case on TO-78 package. Substrate is normally connected to the most negative circuit potential, but can be floated

GENERAL DESCRIPTION

The design of the MAT12 series of NPN dual monolithic transistors is optimized for very low noise, low drift and low r_{BE}. Exceptional characteristics of the MAT12 include offset voltage of 50 µV max and high current gain (h_{FE}) which is maintained over a wide range of collector current. Device performance is specified over the full temperature range as well as at 25°C.

Input protection diodes are provided across the emitter-base junctions to prevent degradation of the device characteristics due to reverse-biased emitter current. The substrate is clamped to the most negative emitter by the parasitic isolation junction created by the protection diodes. This results in complete isolation between the transistors.

The MAT12 is ideal for applications where low noise is a priority. The MAT12 can be used as an input stage to make an amplifier with noise voltage of less than 1.0 nV/√*Hz* at 100 Hz. Other applications, such as log/antilog circuits, may use the excellent logging conformity of the MAT12. Typical bulk resistance is only 0.3 Ω to 0.4 Ω. The MAT12 electrical characteristics approach those of an ideal transistor when operated over a collector current range of 1µA to 10 mA.

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS; V_{CB} = 15V

V_{CB} = 15 V, I_O = 10μA, T_A = 25°C, unless otherwise specified.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current Gain	h_{FE}	I_C = 1mA (note 1)	500	605		
		-25°C≤T_A≤+85°C	325			
		I_C = 100μA	500	590		
		-25°C≤T_A≤+85°C	275			
		I_C = 10μA	400	550		
		-25°C≤T_A≤+85°C	225			
		I_C = 1μA	300	485		
		-25°C≤T_A≤+85°C	200			
Current Gain Match	Δh_{FE}	10μA ≤ I_C ≤ 1mA (note 2)		0.5	2	%
Noise Voltage Density	e_N	I_C = 1mA, V_{CB} = 0 (note 3)				
		f_O= 10Hz		1.6	2	nV/√Hz
		f_O= 100Hz		0.9	1	nV/√Hz
		f_O= 1kHz		0.85	1	nV/√Hz
		f_O= 10kHz		0.85	1	nV/√Hz
Offset Voltage	V_{OS}	V_{CB} = 0, 1μA ≤ I_C ≤ 1mA		10	50	μV
		-25°C≤T_A≤+85°C			70	uV
Offset Voltage Change vs. V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ V_{MAX} (note 4)		10	25	μV
		1μA ≤ I_C ≤ 1mA (note 5)				
Offset Voltage Change vs. I_C	$\Delta V_{OS}/\Delta I_C$	1μA ≤ I_C ≤ 1mA (note 5), V_{CB}=0		5	25	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	-25°C≤T_A≤+85°C		0.08	0.3	μV/ °C
		-25°C≤T_A≤+85°C, V_{OS} trimmed to zero		0.03	0.3	μV/ °C
Breakdown Voltage	BV_{CEO}		40			V
Gain-Bandwidth Product	f_T	I_C = 100mA, V_{CE} = 10V		200		MHz
Collector-Base Leakage Current	I_{CBO}	V_{CB}=V_{MAX}		25	200	pA
		-25°C≤T_A≤+85°C		2		nA
Collector-Collector Leakage Current	I_{CC}	V_{CC}=V_{MAX} (notes 6,7)		35	200	pA
		-25°C≤T_A≤+85°C		3		nA
Collector-Emitter Leakage Current	I_{CES}	V_{BE}=0 (notes 6,7)		35	200	pA
		-25°C≤T_A≤+85°C		3		nA

Input Bias Current	I_B	I_C = 10µA		25	nA
		-25°C≤T_A≤+85°C		45	nA
Input Offset Current	I_{OS}	I_C = 10µA		0.6	nA
		-25°C≤T_A≤+85°C		8	nA
Input Offset Current Drift	$\Delta I_{OS}/\Delta T$	I_C=10µA (note 6)			
		-25°C≤T_A≤+85°C	40	90	pA/°C
Offset Current Change vs. V_{CB}	$\Delta I_{OS}/\Delta V_{CB}$	0 ≤ V_{CB} ≤ V_{MAX} (note 4)	30	70	pA/V
Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1mA, I_B=100µA	0.05	0.1	V
Output Capacitance	C_{OB}	V_{CB}=15V, I_E=0	23		pF
Bulk Resistance	r_{BE}	10µA≤I_C≤10mA (note6)	0.3	0.5	Ω
Collector-Collector Capacitance	C_{CC}	V_{CC} = 0	35		pF

Notes:

1. Current gain is guaranteed with Collector-Base Voltage (V_{CB}) swept from 0 to V_{MAX} at the indicated collector currents.
2. Current Gain Match (Δh_{FE}) defined as: $\Delta h_{FE} = (100(\Delta I_B)(h_{FE\ min})/I_C)$
3. Noise Voltage Density is guaranteed, but not 100% tested
4. This is the maximum change in V_{OS} as V_{CB} is swept from 0V to 40V.
5. Measured at I_C=10µA and guaranteed by design over the specified range of I_C
6. Guaranteed by Design
7. I_{CC} and I_{CES} are verified by measurement of I_{CBO}

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Collector-Base Voltage (BV_{CBO})	40 V
Collector-Emitter Voltage (BV_{CEO})	40V
Collector-Collector Voltage (BV_{CC})	40V
Emitter-Emitter Voltage (BV_{EE})	40V
Collector Current (I_C)	20 mA
Emitter Current (I_E)	20 mA
Storage Temperature Range H Packages	−65°C to +150°C
Operating Temperature Range	−25°C to +85°C
Junction Temperature Range RM, CP Packages	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] Differential input voltage is limited to 5 V or the supply voltage, whichever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
TO-78 (H)	TBD	TBD	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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