天鈺科技股份有限公司
Eureka Microelectronics, Inc.

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EK7309 Preliminary Data Sheet	版 本 REV ：02
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文件制/修訂一覽表 Revision History

版本 REV.	修訂日期 REV Date	生效日期 Eff. Date	修訂頁次 REV. Page	制/修訂項目/ 內容 Revise item /Content
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Eureka Microelectronics, Inc.

EK7309

PRELIMINARY Rev 0.2

DATA SHEET

256-Outputs Gate Driver

EUREKA

EK7309

Contents

EUREKA   EK7309

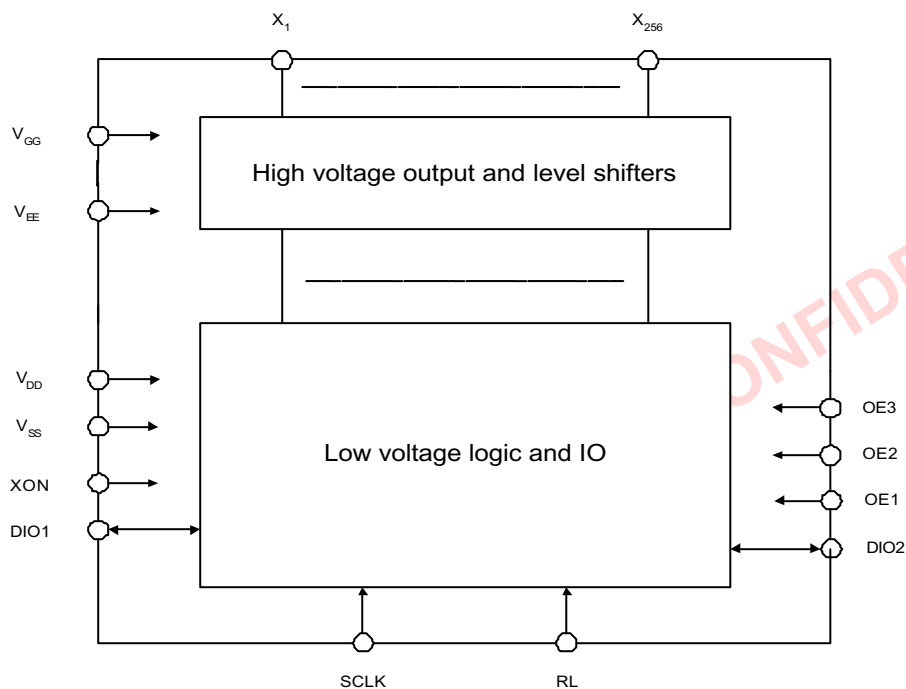## TFT Gate Driver (256 Outputs)

1. GENERAL DESCRIPTION

EK7309 is a TFT LCD gate driver with 256 outputs for XGA/SXGA display systems. The logic and control portion is implemented in standard CMOS circuits while the output drivers use high voltage CMOS design. The low voltage part includes a 256-stage bidirectional shift register with right and left shift I/O for cascading. The output of the shift register is then level translated to drive the high voltage output buffer. There are four supply voltages for EK7309. VDD/VSS are the supply voltages for logic interfaces. Typically VDD is at 3.3V while VSS is 0V. VGG and VEE are the supply voltages for the output driver. VEE is the most negative supply voltage for the internal substrate of EK7309.

EK7309 allows three output enable controls (OE1-3) and one global enable signal (XON).
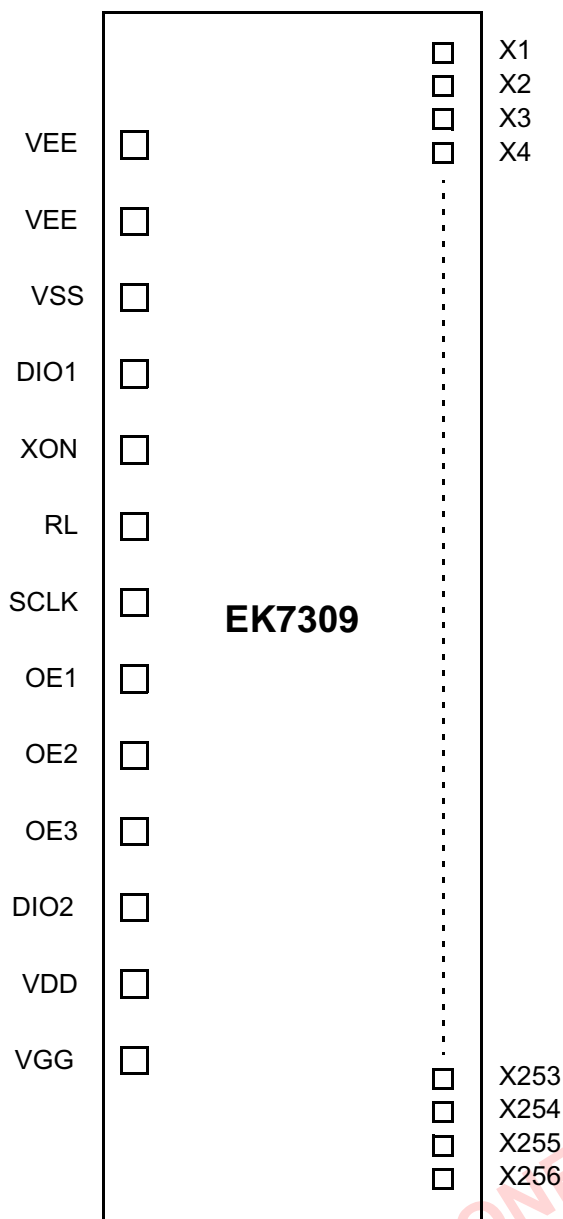
2. FEATURES

- 256 gate drive outputs
- Bidirectional shift control and cascadable
- Output enable and global on control
- Maximum shift clock frequency up to 100KHz
- 3.3V CMOS logic I/O
- High voltage output drive
- Operating supply range
  Logic (VDD-VSS: 3.3V)
  Output Drive (VGG -VEE: 40V)
- TCP package

3. BLOCK DIAGRAM

4. PIN CONFIGURATION

```
                          ┌───────────────────┐
                          │                ☐  │  X1
                          │                ☐  │  X2
                          │                ☐  │  X3
              VEE   ☐      │                ☐  │  X4
                          │                ┊  │
              VEE   ☐      │                ┊  │
                          │                ┊  │
              VSS   ☐      │                ┊  │
                          │                ┊  │
              DIO1  ☐      │                ┊  │
                          │                ┊  │
              XON   ☐      │                ┊  │
                          │                ┊  │
              RL    ☐      │                ┊  │
                          │                ┊  │
              SCLK  ☐      │    EK7309      ┊  │
                          │                ┊  │
              OE1   ☐      │                ┊  │
                          │                ┊  │
              OE2   ☐      │                ┊  │
                          │                ┊  │
              OE3   ☐      │                ┊  │
                          │                ┊  │
              DIO2  ☐      │                ┊  │
                          │                ┊  │
              VDD   ☐      │                ┊  │
                          │                ☐  │  X253
              VGG   ☐      │                ☐  │  X254
                          │                ☐  │  X255
                          │                ☐  │  X256
                          └───────────────────┘
```

IC top view. This diagram shows EK7309's pin configuration only. It does not necessarily correspond to the pad layout on the chip.

Figure-1

5. PIN FUNCTION DESCRIPTION

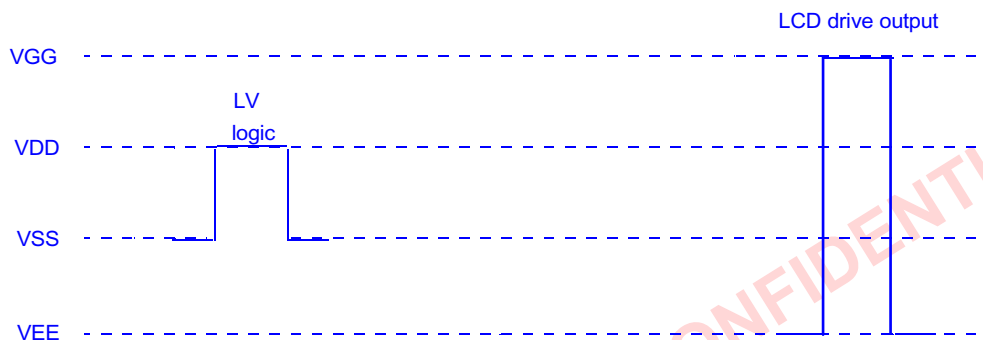| Name	Pin	Description
SCLK	I	Shift clock. This is a 3.3V CMOS level input for shift register clock. The rising edge of SCLK is used.
RL	I	Right/Left shift control. RL=1 is shift right (X1 -> X256), RL=0 is shift left (X256 -> X1).
DIO1 **DIO2**	I/O	**DIO1** **DIO2** RL = "H" Input Output RL = "H" Output Input
OE1, OE2, OE3	I	Output enable control. The output is forced low when OE is high. OE1 controls output 1,4,...,253,256. The control is asynchronous to SCLK. OE2 controls output 2,5,...,251,254. The control is asynchronous to SCLK. OE3 controls output 3,6,...,252,255. The control is asynchronous to SCLK.
XON	I	Global on control. When XON=0, all outputs are forced high. XON is asychronous to SCLK.
X [1-256]	O	Output drive. These are the gate drive outputs.The high level is VGG and the low level is VEE.
VDD	P	Positive supply voltage for LV logic . This is typically 3.3V.
VSS	P	Negative supply voltage for LV logic. This is typically 0V.
VGG	P	Positive supply voltage for the output driver. This is typically the most positive supply voltage to EK7309.
VEE	P	Negative supply voltage for the output drive and the substrate. This is the most negative supply voltage to EK7309.

Figure-2

6. FUNCTIONAL DESCRIPTION

6.1 When RL is "HIGH" and a start pulse inputs the DIO1 pin, this pulse is shifted right by the shift control register at the rising edge of SCLK. While the output of the shift control register is "HIGH", the Xn [n=1, 2, 3,..., 256] is pulled to VGG. If the output of the shift control register is "LOW", Xn [n=1, 2, 3,..., 256] is pushed to VEE; DIO2 is pulled to high at the falling edge of the 256th clock of SCLK and is pushed to low at the falling edge of the 257th clock of SCLK. Please refer to operating waveform (1).

6.2 When RL is "LOW" and a start pulse inputs the DIO2 pin, this pulse is shifted left by the shift control register at the rising edge of SCLK. While the output of the shift control register is "HIGH", the Xn [n=256, 255, 254,..., 1] is pulled to VGG. If the output of the shift control register is "LOW", Xn [n=256, 255, 254,..., 1] is pushed to VEE; DIO1 is pulled to high at the falling edge of the 256th clock of SCLK and is pushed to low at the falling edge of the 257th clock of SCLK. Please refer to operating waveform (2).

6.3 OE1, OE2, and OE3 can disable Xn [n=1, 2, 3,..., 256]. They are asynchronous to SCLK.
    Xn [n=1, 4, 7,..., 253, 256] is pushed to VEE when OE1 is "HIGH".
    Xn [n=2, 5, 8,..., 251, 254] is pushed to VEE when OE2 is "HIGH".
    Xn [n=3, 6, 9,..., 252, 255] is pushed to VEE when OE3 is "HIGH".
    Please refer to operating waveform (1) and (2).

6.4 The global on control XON can enable Xn [n=1, 2, 3,..., 256]. It is asynchronous to SCLK. Whenever XON is "LOW", all outputs of EK7309 are pulled to VGG at the same time. Please refer to operating waveform (3).

7. TIMING DIAGRAM

RL=1, shift right

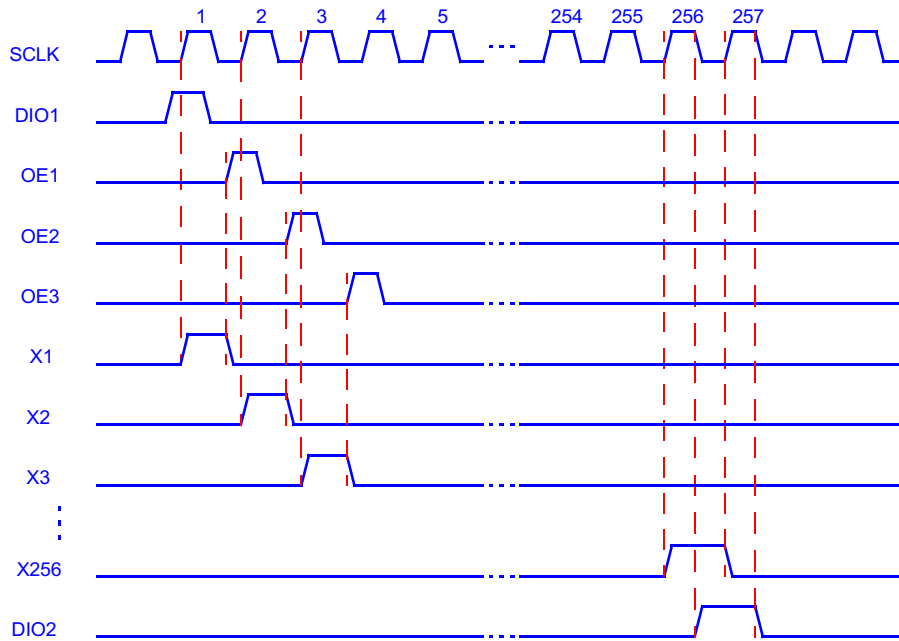**Figure-3 Operating Waveforms (1)**

RL=0, shift left
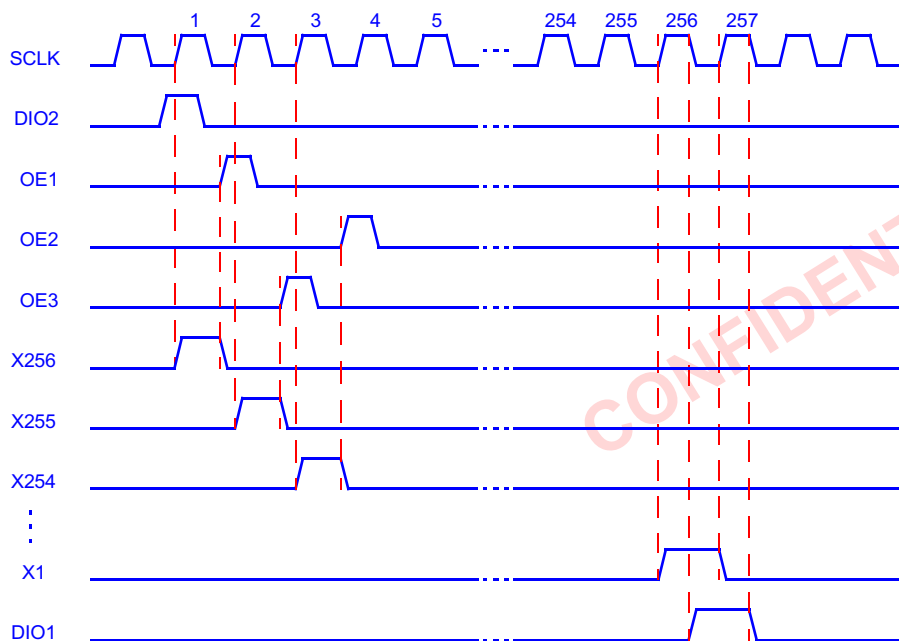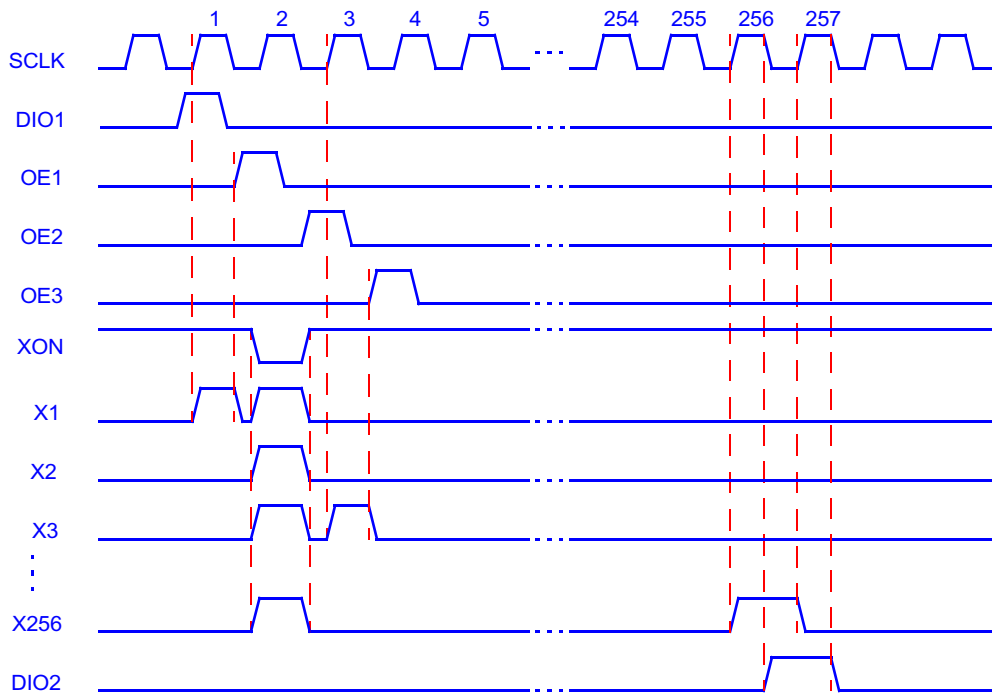

Figure-4 Operating Waveforms (2)

XON=0, RL=1

Figure-5 Operating Waveforms (3)

8. ABSOLUTE MAXIMUM RATING

8.1 ABSOLUTE MAZIMUM RATING

V_{LL} = 0V

Symbol	Parameter	Rating	Unit
V_{DD}	Logic Supply Voltage	-0.3 ~ +7.0	V
V_{GG}	Positive Supply Voltage	-0.3 ~ +45	V
V_{EE}	Most Negative Supply Voltage	V_{GG}-45 ~ +0.3	V
V_{IN}	Logic Input Voltage	-0.3 ~ V_{DD} +0.3	V
T_a	Operation Ambient Temperature	-30 ~ +85	°C
T_{stg}	Storage Temperature Range	-55 ~ +120	°C

8.2 RECOMMENDED OPERATING RANGE

V_{LL} = 0V

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Logic Supply Voltage	3.0	3.3	3.6	V
V_{GG}	Positive Supply Voltage	10		V_{EE} + 40	V
V_{EE}	Most Negative Supply Voltage	-25		-5	V
T_a	Operation Ambient Temperature	-20		**+70**	°C

Note: Power ON/OFF sequence is as below:
1. Power ON sequence: VSS → VDD → VEE → VGG.
2. Power OFF sequence: VGG → VEE → VDD → VSS.

Figure-6

9. DC ELECTRICAL CHARACTERISTICS

9.1 Supply current

Ta = 25℃, V_{SS} = 0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{VDD1}	Operating current	f_{SCLK} = 15.7KHz f_{SL} = 60Hz V_{DD} = 3.3V V_{EE} = -15V V_{GG} = 15V no loading			800	µA
I_{VGG1}					300	µA
I_{VDD}	Standby current	V_{DD} = 3.3V V_{EE} = -15V V_{GG} = 15V			600	µA
I_{VGG2}					100	µA

9.2 Input pin: RL, SCLK, OE1, OE2, OE3, XON

Ta = 25℃, V_{SS} = 0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH1}	Input Voltage, HIGH		$0.8 \times V_{DD}$		V_{DD}	V
V_{IL1}	Input Voltage, LOW		0		$0.2 \times V_{DD}$	V
I_{LI1}	Input Leakage Current	XON except	-2		+2	µA

9.3 I/O pin: DIO1, DIO2

Ta = 25℃, V_{SS} = 0V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{IH2}	Input Voltage, HIGH		$0.8 \times V_{DD}$		V_{DD}	V
V_{IL2}	Input Voltage, LOW		0		$0.2 \times V_{DD}$	V
V_{OH}	Output Voltage, HIGH	-100µA	V_{DD}-0.4			V
V_{OL}	Output Voltage, LOW	100µA			0.4	V

9.4 Output pin: X1 ~ X256

$T_a = 25°C$, $V_{SS} = 0V$

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{LO1}	Output Leakage Current		-50		50	μA
R_{ON}-V_{GG}		$V_{GG} = 15V$ $V_{EE} = -15V$ $V_{OM} = V_{GG} -0.5V$ V_{OM} is X1-X256		600	1000	ohm
R_{ON}-V_{GG}	Output ON Resistance	$V_{GG} = 15V$ $V_{EE} = -10V$ $V_{OM} = V_{EE}+0.5V$ V_{OM} is X1-X256		600	1000	ohm

10. AC CHARACTERISTICS

$T_a = 25°C$, $V_{SS} = 0V$

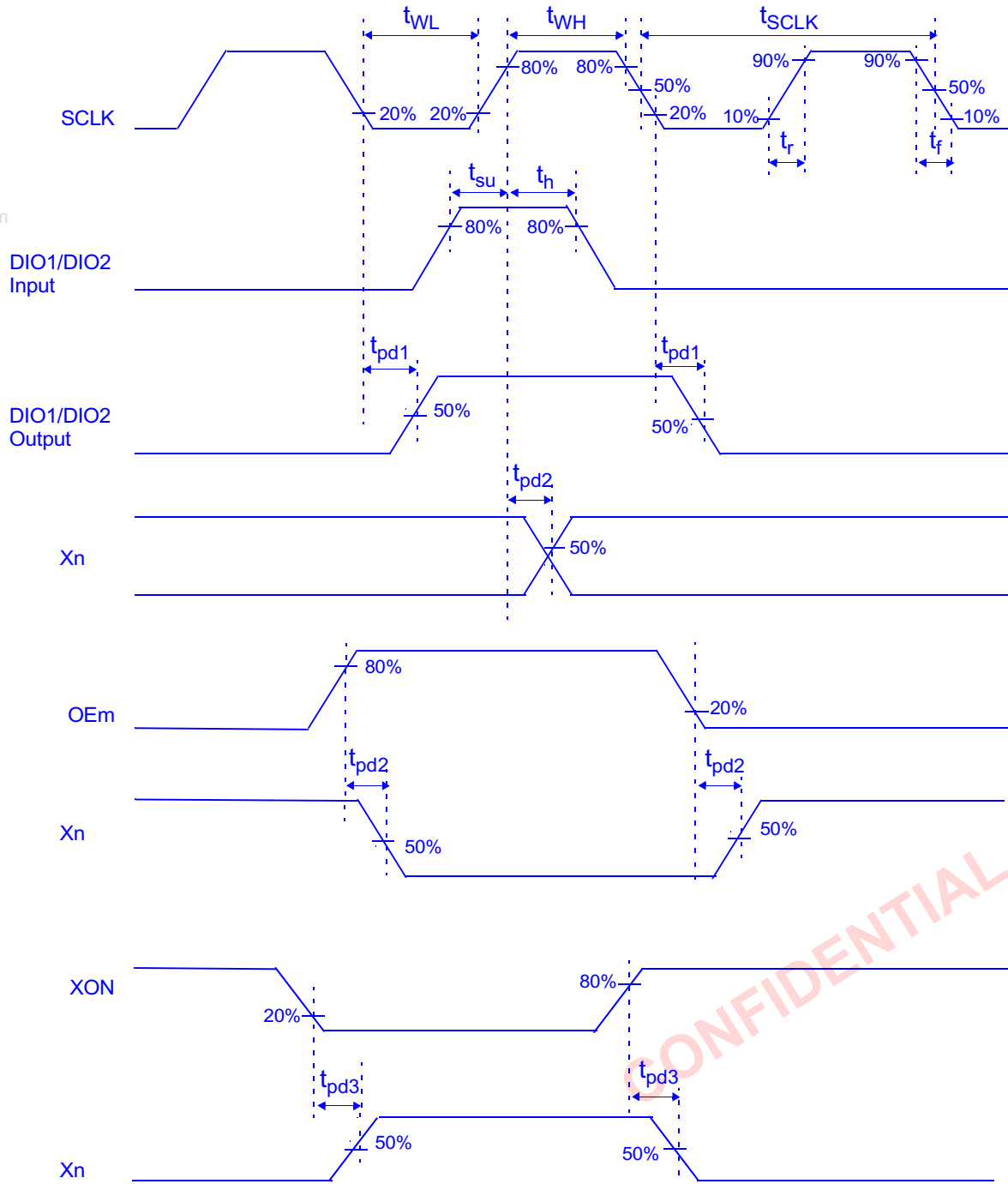| Symbol	Parameter	Condition	Min	Typ	Max	Unit
t_{SCLK}	Shift Clock Period		10			µs
t_{WH}	Shift Clock Pulse Width, HIGH		4			µs
t_{WL}	Shift Clock Pulse Width, LOW		4			µs
t_r	Shift Clock Rise Time				100	ns
t_f	Shift Clock Fall Time				100	ns
t_{su}	DIO1/DIO2 Input Setup Time		50			ns
t_n	DIO1/DIO2 Input Hold Time		350			ns
t_{pd1}	DIO1/DIO2 Output Delay Time	CL = 50pF			300	ns
t_{pd2}	Xn Output Delay Time	CL = 300pF			800	ns
t_{pd3}	Xn Output Delay Time (XON only)	CL = 300pF			1000	ns

AC Characteristics Waveforms

Figure-7

DEFINITIONS

Data Sheet status	
Objective specification	This data sheet contains target or goal specification for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specification.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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