Current Mode PWM Controller

FEATURES

- Burst Mode function
- Low startup current (6.5uA)
- Low operating current (2.3mA)
- Built-edge blanking
- Built-in synchronized slope compensation
- Current mode
- External Programmable PWM Switching Frequency
- By-cycle current limit protection (OCP)
- VDD over-voltage clamping protection
- Low voltage shut down function (UVLO)
- Gate Drive Output Voltage Clamp (18V)
- Frequency jitter feature
- Constant output power limit
- Overload protection (OLP)
- Work does not produce audio noise

APPLICATIONS

Offline AC/DC flyback converter for

- Power Adaptor
- Open-frame SMPS
- Battery Charger
- Set-Top Box Power Supplies

GERNERAL DESCRIPTION

WIS2269 is a highly integrated, high performance current mode PWM controller chip. Apply to the power adapter and other small and medium-power switch power supply.

In order to reduce standby power consumption to meet the higher standards of environmental protection, the chip provides a pulse mode (Burst Mode) function, very low starting current and operating current. Pulse mode that is in the light load or no load conditions, WIS2269 can linearly decrease the switching frequency chip, thereby reducing switching loss; by optimizing the design, WIS2269 has a very low starting current and operating current, is not only beneficial to start the circuit design, and the start circuit can be used in high-value startup resistor, to reduce power consumption, improve power conversion efficiency.

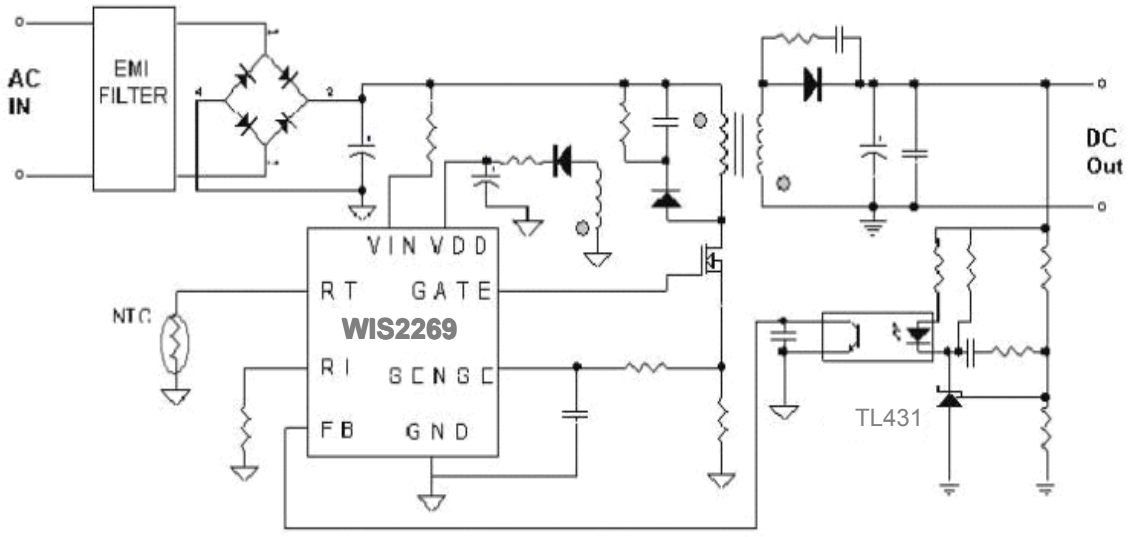
WIS2269 built-in synchronized slope compensation circuit, to prevent the PWM controller when working in high-duty cycle may have harmonic oscillation. WIS2269 side in the current sample input pin edge blanking function built in, can effectively remove the current feedback signal of the glitch. Help to reduce the number of external components, reducing overall system cost.

WIS2269 offers a variety of comprehensive resume protection mode, including:-by-cycle current limit protection (OCP), over-load protection (OLP), VDD over-voltage clamping voltage and low voltage closed (UVLO). Which, in order to better protect the external MOSFET power transistor, the gate drive output voltage is clamped at 18V.

WIS2269 the totem pole gate drive output using a frequency jitter control technology and soft-switching technology, can be very good to improve EMI performance switching power supply system. By optimizing the design, when the chip's operating frequency less than 20KHz circumstances, the audio energy can be reduced to a minimum. Therefore, the audio can get greatly improved noise performance.

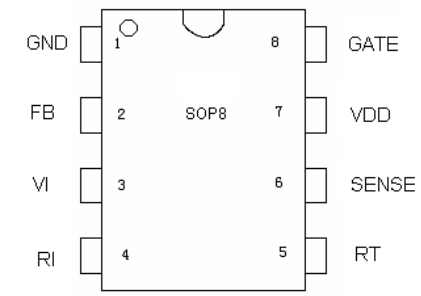
WIS2269-chip can be used as RCC-mode power supply linear power supply or the best alternative to enhance the overall performance of switching power supply system, and effectively reduce the system cost.

TYPICAL APPLICATION



GENERAL INFORMATION

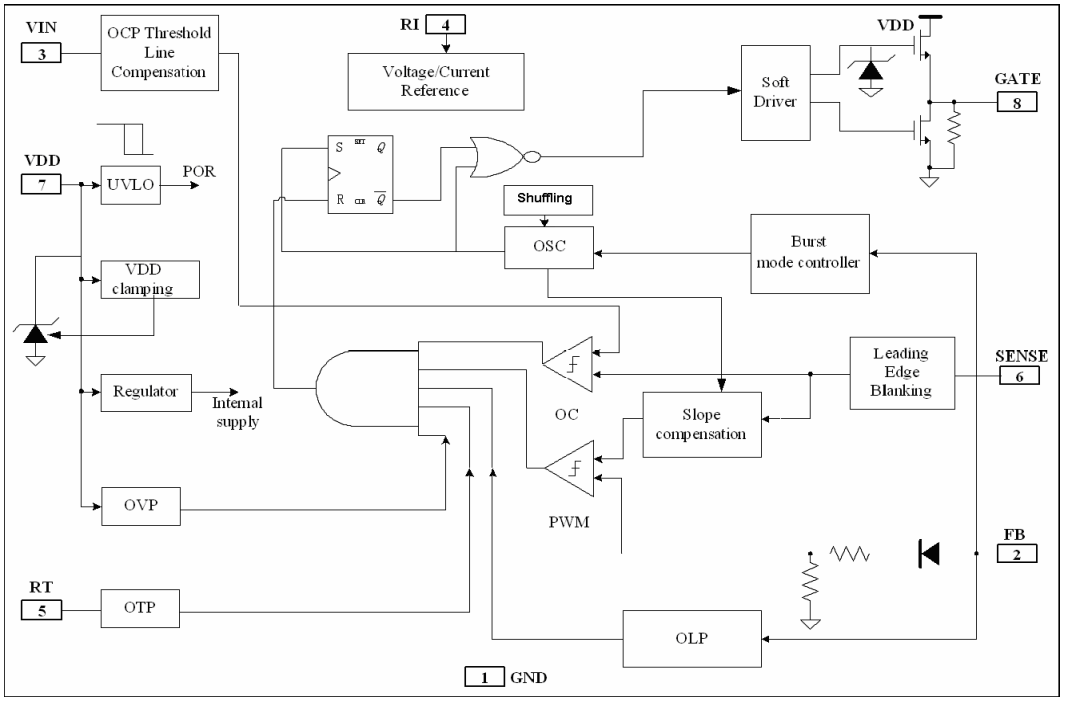
Pin Configuration



TERMINAL ASSIGNMENTS

Pin Name	Pin No.	I/O	Description
GND	1	P	Ground
FB	2	I	Feedback input pin. The input level value and 6-pin to monitor the value of current is indeed common set PWM duty cycle control signal. If the FB terminal of the input voltage is greater than a set set threshold voltage, the internal protection circuit will automatically turn off PWM output.
VI	3	I	Through a high resistance of the resistor connected to the rectifier output, start the device into the working condition; while the voltage is sampled to generate line voltage compensation.
RI	4	I	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
RT	5	I	Temperature monitoring of input pins. By a NTC resistor connected to ground.
SENSE	6	I	Current sense input pin. Connected to MOSFET current sensing resistor node.
VDD	7	P	Chip DC power supply pin
GATE	8	O	Totem-pole gate drive output for the power MOSFET.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min	Max	Unit
V_{DD}	VDD Supply Voltage	12	23	V
RI	RI Resistor Value	24		KΩ
T	Operating Ambient Temperature	-20	85	℃

ABSOLUTE MAXIMUM RATINGS

Pin Name	Parameter	Ratings	Units
V_{DD}	V_{DD} Pin input voltage	30	V
V_{FB}	V_{FB} Pin input voltage	-0.3~7	V
V_{SENSE}	V_{SENSE} Pin input voltage	-0.3~7	V
V_{RI}	V_{RI} Pin input voltage	-0.3~7	V
V_{RT}	V_{RT}Pin input voltage	-0.3~7	V
T_J	Operating Junction Temperature	-20~150	℃
T_S	Storage Temperature	-55~160	℃
Vcv	V_{DD} DC Clamping Voltage	34	V
I_{CC}	V_{DD} DC Clamping Current	10	mA

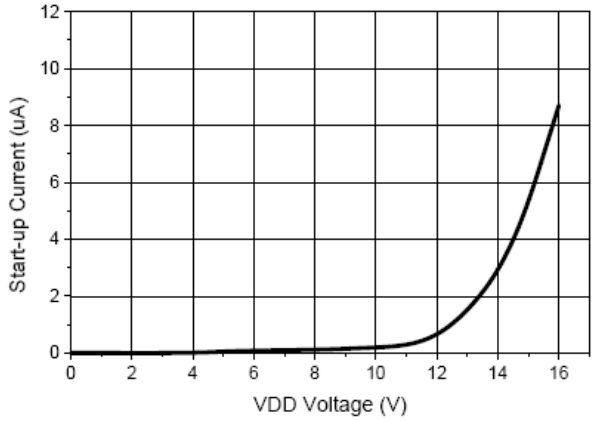
Note: more than the limit specified in the table parameters will result in permanent damage to the device. The device is not recommended in these extreme conditions of work, working conditions in the limit above which may affect device reliability.

Electrical Characteristics (Tc = 25°C, V_{DD}=16V, R_I=25KΩ, Unless otherwise specified)

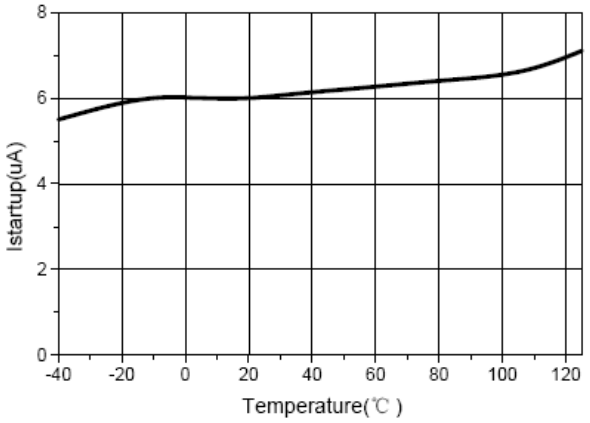
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_VDD_Startup	VDD startup current	VDD=15V, measure current into VDD		6.5	20	uA
I_VDD_Operation	Operation Current	FB=3V		2.3		mA
UVLO(ON)	VDD under voltage lockout enter		9.5	10.5	11.5	V
UVLO(OFF)	VDD under voltage lockout exit		16	17	18	V
OVP(ON)	VDD Over Voltage Protection Enter		23.5	25	26.5	V
OVP(OFF)	VDD Over Voltage Protection Exit		21.5	23.2	24.7	V
TD_OVP	OVP Debounce time			80		us
VDD_Clamp	VDD Clamp voltage	I(V_{DD})=5mA		36		V
Feedback Input Section(FB Pin)						
Avcs	PWM Input Gain,	$\triangle V_{FB}/\triangle V_{CS}$		2.6		V/V
VFB_Open	VFB Open Voltage			6		V
I_{FB}_Short	FB pin short current	Short FB pin to GND		0.8		mA
VTH_0D	Zero Duty Cycle FB Threshold Voltage				0.95	V
VTH_BM	Burst Mode FB Threshold Voltage			1.7		V
VTH_PL	Power Limiting FB Threshold			4.4		V
TD_PL	Power Limiting Debounce Time			80		mSec
ZFB_IN	Input Impedance			7.5		Kohm
Current Sense Input(Sense Pin)						
T_blanking	Sense Input Leading Edge Blanking Time			300		nSec
Zsense_IN	Sense Input Impedance			39		kohm
TD_OC	Over Current Detection and Control Delay	C_L=1nF at GATE		120		nSec
VTH_OC_0	Current Limiting Threshold at No Compensation	I(VIN)=0uA	0.85	0.9	0.95	V
VTH_OC_1	Current Limiting Threshold at Compensation	I(VIN)=150uA		0.81		V

Oscillator						
F_{OSC}	Normal Oscillation Frequency		60	65	70	KHz
Δf_Temp	Frequency Temperature Stability	-20℃ to 100℃		5		%
Δf_VDD	Frequency Voltage Stability	VDD=12 to 24V		5		%
RI_range	Operating RI range		12	24	60	Khom
V_RI_open	RI open voltage			2		V
F_BM	Burst mode Base frequency			22		KHz
DC_max	Maximum Duty Cycle		75	80	85	%
DC_min	Minimum Duty Cycle				0	%
Gate Drive Output						
VOL	Output low level	Io=-20mA			0.3	V
VOH	Output high level	Io=+20mA	11			V
VG_Clamp	Output Clamp Voltage Level	VDD=20V		18		V
T_r	Output rising time	C_{GATE}=1nF		100		ns
T_f	Output falling time	C_{GATE}=1nF		50		ns
Over Temperature Protection						
I_RT	Output Current of RT Pin			70		uA
VTH_OTP	OTP Threshold Voltage		1	1.065	1.13	V
VTH_OTP_off	OTP Recovery Threshold Voltage			1.165		V
TD_OTP	OTP De-bounce Time			100		uSec
V_RT_Open	RT Pin Open Voltage			3.5		V

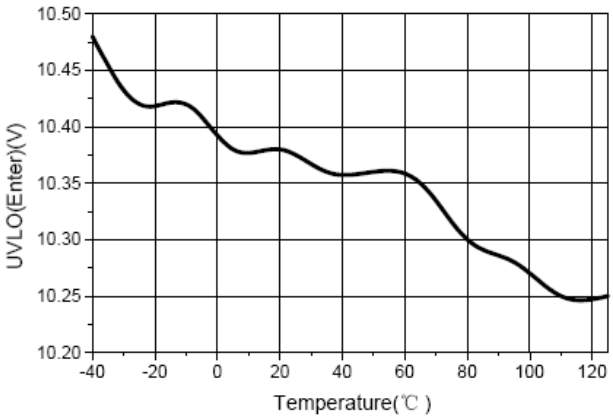
VDD Start-up Current vs Voltage



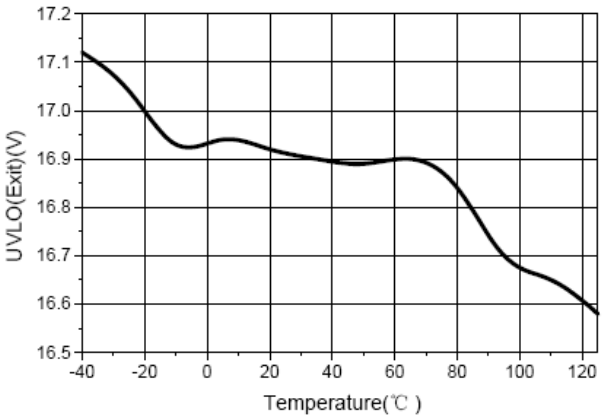
VDD Startup Current vs Temperature



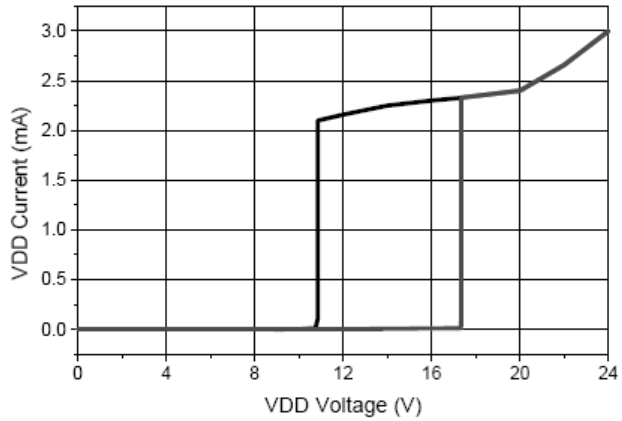
VDD UVLO(Enter) vs Temperature



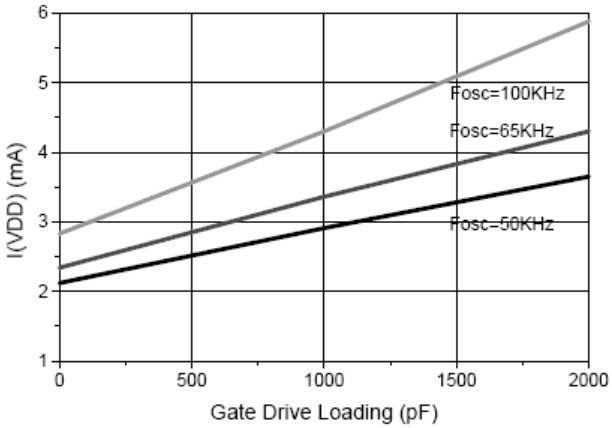
VDD UVLO(Exit) vs Temperature

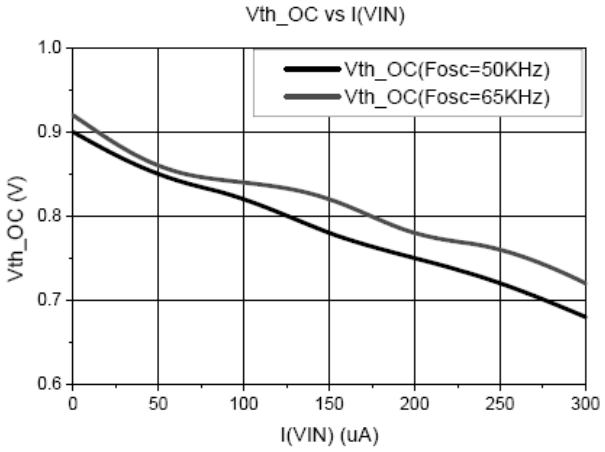


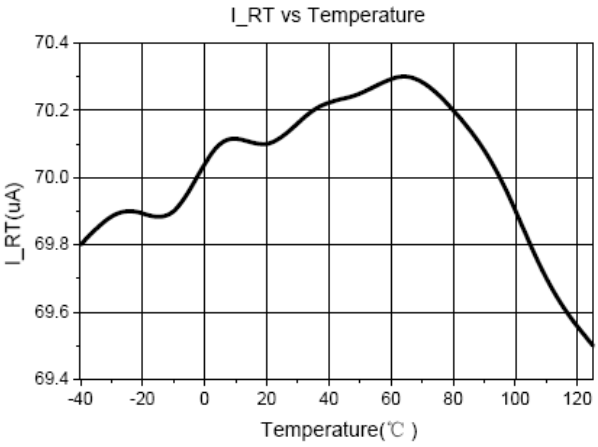
VDD UVLO and Operation Current

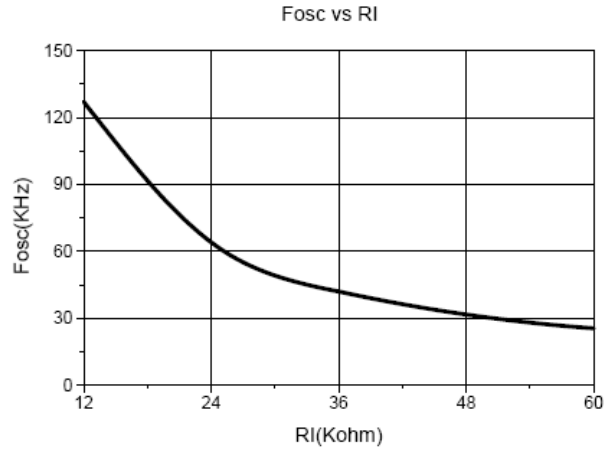


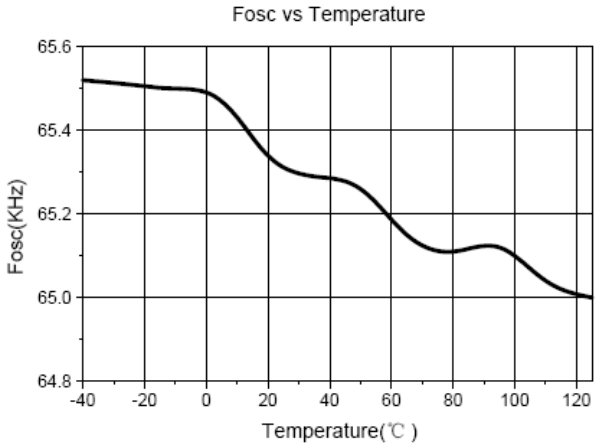
VDD Operation Current vs Load




Vth_OC vs I(VIN)
Vth_OC(Fosc=50KHz)
Vth_OC(Fosc=65KHz)
Vth_OC (V)
I(VIN) (uA)
1.0
0.9
0.8
0.7
0.6
0
50
100
150
200
250
300


I_RT vs Temperature
I_RT(uA)
Temperature(℃)
70.4
70.2
70.0
69.8
69.6
69.4
-40
-20
0
20
40
60
80
100
120


Fosc vs RI
Fosc(KHz)
RI(Kohm)
150
120
90
60
30
0
12
24
36
48
60


Fosc vs Temperature
Fosc(KHz)
Temperature(℃)
65.6
65.4
65.2
65.0
64.8
-40
-20
0
20
40
60
80
100
120

OPERATION DESCRIPTION

The WIS2269 is a highly integrated, high performance current mode PWM controller chip. Applicable to high power notebook power adapter switching power supply and switching power converters. Very low starting current and operating current, and light load or no load situations burstmode function, can effectively reduce the switching power supply system, standby power consumption, improve power conversion efficiency. Built-in synchronized slope compensation of the feedback pin of the leading edge blanking and other functions can not only reduce the number of switching power supply system components, but also increase the stability of the system, to avoid the production of harmonic oscillation. WIS2269 also offers a variety of comprehensive resume protected mode. Features functions described as follows:

Startup Current and Start up Control

Startup current of WIS2269 is designed to be very low(6.5uA) so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet provides reliable startup in application. For AC/DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and low power dissipation solution.

Operating Current

The Operating current of WIS2269 is low at 2.3mA. Good efficiency is achieved with WIS2269 low operating current together with extended burst mode control features.

Burst Mode

At no load or light load conditions, switching power supply in most of the power comes from the MOSFET's switching losses, transformer core losses and the loss of the buffer circuit. The size and power consumption within a certain period of time proportional to the number of MOSFET switches. Reduce the switching frequency also reduces power consumption, saving energy. WIS2269 built-in Burst Mode feature that automatically adjusts according to load switch mode. When the system is in no load or light / medium load, FB terminal voltage at the pulse input mode (BurstMode) threshold voltage (1.8V) below. According to the judge based on the device into the pulse mode control. Gate driver output voltage only when the VDD level below the pre-set value, and the FB input is active cases does the output. Other cases, the gate drive output to maintain the status of long-off to reduce power consumption, which reduces standby power consumption. The characteristics of high-frequency switch also reduced the audio noise at work.

Oscillator Operation

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

$$Fosc = \frac{1560}{RI(K\Omega)}(KHz)$$

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in WIS2269 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to Snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Gate Drive

WIS2269 Gate is connected to an external MOSFET gate for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI. A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

Over-temperature protection

Between RT and GND, and a common thread of a NTC resistor, can provide temperature sensing and protection. NTC resistance with the ambient temperature rises. With a fixed internal current flows through the resistor IRT, RT pin voltage with temperature

The rises. Within the OTP circuit to detect the voltage is less than VTH_OP then triggered off when the MOSFET

Protection Controls

WIS2269 provides comprehensive protection features, the system can obtain the highest reliability. Including by-week limit protection (OCP), over-load protection (OLP), over-temperature protection (OTP), on-chip VDD over-voltage protection (OVP, optional), and low-voltage shutdown (UVLO).

When the ER into the VIN pin large, OCP threshold value is automatically reduced. OCP threshold slope adjustment helps compensate for over-current detection and control of AC voltage delay caused by the increasing of the power limit.

Recommended by WIS2269 OCP compensation circuit can obtain constant output power limit. WIS2269 OCP protection circuitry built-in can detect the duty cycle of PWM control signals, and through the line voltage compensation ensure a continuous AC input voltage range was constant output power limit.

In the case of output overload, FB bias voltage was higher, when FB input exceeds the power limit threshold.

voltage continue to 80ms, the control circuit will turn off MOSFET. Similarly, the control circuitry detects over-temperature in the case will be closed when the MOSFET. WIS2269 hysteresis temperature value at a temperature lower than after the recovery. VDD output from the transformer provide the sub-winding. VDD is clamped at 36V. When VDD below the UVLO threshold time, MOSFET is turned off, the device and then entered on the electronic activation.

SOP-8 Package Dimension