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Intel® 925X Express Chipset

Datasheet

For the Intel® 82925X Memory Controller Hub (MCH)

August 2004

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Revision History

Revision	Description	Date
-001	• Initial Release	June 2004
-002	• Added EM64T Support Information	August 2004

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Intel® 82925X MCH Features

- Processor Interface
  - One Intel® Pentium® 4 processor (supports 775-land package)
  - Supports Pentium 4 processor FSB interrupt delivery
  - 800 MT/s (200 MHz) FSB
  - Supports Hyper-Threading Technology (HT Technology)
  - FSB Dynamic Bus Inversion (DBI)
  - 32-bit host bus addressing for access to 4 GB of memory space
  - 12-deep In-Order Queue
  - 1-deep Defer Queue
  - GTL+ bus driver with integrated GTL termination resistors
  - Supports a Cache Line Size of 64 bytes
  - Supports Intel Pentium® 4 processors with Intel® EM64T
- DMI Interface
  - A chip-to-chip connection interface to Intel® ICH6
  - 2 GB/s point-to-point DMI to ICH6 (1 GB/s each direction)
  - 100 MHz reference clock (shared with PCI Express Graphics Attach).
  - 32-bit downstream addressing
  - Messaging and Error Handling

- System Memory
  - One or two 64-bit wide DDR2 SDRAM data channels
  - Bandwidth up to 8.5 GB/s (DDR2 533) in dual-channel Interleaved mode
  - ECC and Non-ECC memory
  - 256-Mb, 512-Mb and 1-Gb DDR2 technologies
  - Only x8, x16, DDR2 devices with four banks and also supports eight bank, 1-Gbit DDR2 devices.
  - Opportunistic refresh
  - Up to 64 simultaneously open pages (four ranks of eight bank devices* 2 channels)
  - SPD (Serial Presence Detect) scheme for DIMM detection support
  - Suspend-to-RAM support using CKE
  - Supports configurations defined in the JEDEC DDR2 DIMM specification only
- PCI Express Graphics Interface
  - One x16 PCI Express port
  - Compatible with the PCI Express Base Specification Revision 1.0a
- Package
  - 37.5 mm × 37.5 mm., 1210 balls, variable ball pitch

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1 *Introduction*

The Intel® 925X Express chipset is designed for use with the Intel® Pentium® 4 processor in entry-level, uniprocessor workstation platforms. The chipset contains two components: 82925X Memory Controller Hub (MCH) for the host bridge and I/O Controller Hub 6 (ICH6) for the I/O subsystem. The MCH provides the interface to the processor, main memory, PCI Express, and the ICH6. The ICH6 is the sixth generation I/O Controller Hub and provides a multitude of I/O related functions. Figure 1-1 shows an example system block diagram for the 925X Express chipset.

For great workstation application flexibility, the Intel® 925X Express chipset is specifically designed to support Intel® Extended Memory 64 Technology* (Intel® EM64T) enabling 64-bit memory addressability. Select versions of the Pentium 4 processor support Intel® Extended Memory 64 Technology* (Intel® EM64T) as an enhancement to Intel's IA-32 architecture on workstation platforms. This enhancement enables the processor to execute operating systems and applications written to take advantage of Intel® EM64T. Further details on the 64-bit extension architecture and programming model can be found in the Intel(R) Extended Memory 64 Technology Software Developer Guide at http://developer.intel.com/technology/64bitextensions/.

* Intel® Extended Memory 64 Technology (Intel® EM64T) requires a computer system with a processor, chipset, BIOS, OS, device drivers and applications enabled for Intel EM64T. Processor will not operate (including 32-bit operation) without an Intel EM64T-enabled BIOS. Performance will vary depending on your hardware and software configurations. Intel EM64T-enabled OS, BIOS, device drivers and applications may not be available. Check with your vendor for more information.

This document is the datasheet for the Intel® 82925X MCH. Topics covered include; signal description, system memory map, register descriptions, a description of the MCH interfaces and major functional units, electrical characteristics, ballout definitions, and package characteristics.

Note: Unless otherwise specified, ICH6 refers to the Intel® 82801FB ICH6, 82801FR ICHR, 82801FW ICH6W, and 82801FRW ICH6RW I/O Controller Hub components.

Figure 1-1. Intel® 925X Express Chipset System Block Diagram Example

Intel® 82925X MCH Datasheet

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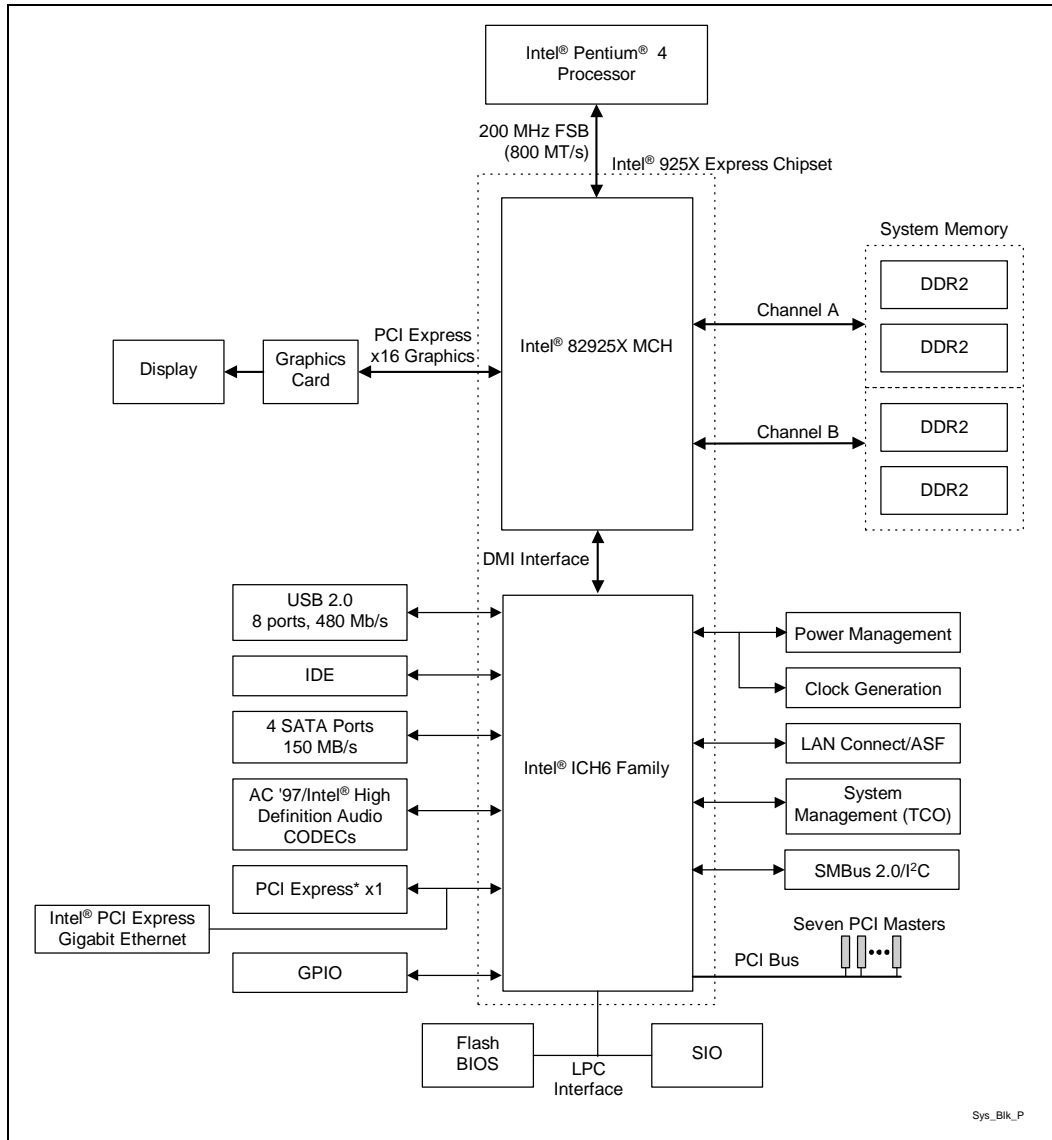
1.1   Terminology

Term	Description
Core	Core refers to the internal base logic in the MCH.
DBI	Dynamic Bus Inversion.
DDR2	A second generation Double Data Rate SDRAM memory technology.
DMI	The Direct Media Interface is the connection between the MCH and the Intel® ICH6.
FSB	Front Side Bus. The FSB is synonymous with Host or processor bus
Full Reset	Full reset is when PWROK is de-asserted. Warm reset is when both RSTIN# and PWROK are asserted.
Host	This term is used synonymously with processor.
INTx	An interrupt request signal where X stands for interrupts A,B,C and D.
Intel® ICH6	Sixth generation I/O Controller Hub component that contains additional functionality compared to previous ICH6s. The Intel® I/O Controller Hub component contains the primary PCI interface, LPC interface, USB2, ATA-100, and other I/O functions. It communicates with the MCH over a proprietary interconnect called DMI.
MCH	The Memory Controller Hub (MCH) component contains the processor interface and DRAM controller. It may also contain an x16 PCI Express port (typically the external graphics interface). It communicates with the I/O controller hub (ICH6*) and other I/O controller hubs over the DMI interconnect.
MSI	Message Signaled Interrupt. A transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.
PCI Express*	Third Generation Input Output (PCI Express) Graphics Attach called PCI Express Graphics. A high-speed serial interface whose configuration is software compatible with the existing PCI specifications. The specific PCI Express implementation intended for connecting the MCH to an external graphics controller is a x16 link and replaces AGP.
Primary PCI	The physical PCI bus that is driven directly by the ICH6 component. Communication between Primary PCI and the MCH occurs over DMI. Note that the Primary PCI bus is **not** PCI Bus 0 from a configuration standpoint.
SCI	System Control Interrupt. SCI is used in ACPI protocol.
SERR	An indication that an unrecoverable error has occurred on an I/O bus.
SMI	System Management Interrupt. SMI is used to indicate any of several system conditions (such as thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity).
Rank	A unit of DRAM corresponding to eight x8 SDRAM devices in parallel or four x16 SDRAM devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DIMM.
TOLM	Top Of Low Memory. The highest address below 4 GB for which a processor-initiated memory read or write transaction will create a corresponding cycle to DRAM on the memory interface.

Term	Description
VCO	Voltage Controlled Oscillator.

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1.2 Reference Documents

Document Title	Document Number/Location
Intel® 925X Express Chipset Thermal Design Guide	http://intel.com/design/chipsets/designex/301466.htm
Intel® I/O Controller Hub 6 (ICH6) Family Datasheet	http://intel.com/design/chipsets/datashts/301473.htm
Advanced Configuration and Power Interface Specification, Version 2.0	http://www.acpi.info/
Advanced Configuration and Power Interface Specification, Version 1.0b	http://www.acpi.info/
The PCI Local Bus Specification, Version 2.3	http://www.pcisig.com/specifications
PCI Express Specification, Version 1.0a*	http://www.pcisig.com/specifications

1.3 MCH Overview

The MCH connects to the processor as shown in Figure 1-1. A major role of the MCH in a system is to manage the flow of information between its interfaces: the processor interface (FSB), the System Memory interface (DRAM controller), the external graphics interface via PCI Express, and the I/O Controller Hub through the DMI interface. This includes arbitrating between the interfaces when each initiates transactions. The processor interface supports the Pentium 4 processor subset of the Extended Mode of the Scalable Bus Protocol.

The MCH supports one or two channels of DDR2 SDRAM. The MCH also supports the new PCI Express based external graphics attach. Thus, the 925X Express chipset is NOT compatible with AGP (1X, 2X, 4X, or 8X).

To increase system performance, the MCH incorporates several queues and a write cache. The MCH also contains advanced desktop power management logic.

1.3.1 Host Interface

The MCH is optimized for the Pentium 4 processors in the LGA775 socket. The MCH supports a FSB frequency of 200 MHz (800 MT/s) using a scalable FSB. The MCH supports the Pentium 4 processor subset of the Extended Mode Scaleable Bus Protocol. The primary enhancements over the Compatible Mode P6 bus protocol are: Source synchronous double-pumped (2) Address and Source synchronous quad-pumped (4x) Data.

The MCH supports 32-bit host addressing, decoding up to 4 GB of the processor's memory address space. Host-initiated I/O cycles are decoded to PCI Express, DMI, or the MCH configuration space. Host-initiated memory cycles are decoded to PCI Express, DMI, or system memory. PCI Express device accesses to non-cacheable system memory are not snooped on the host bus. Memory accesses initiated from PCI Express using PCI semantics and from DMI to system memory will be snooped on the host bus.

1.3.2   System Memory Interface

The MCH integrates a system memory DDR2 controller with two, 64-bit wide interfaces. Only Double Data Rate (DDR2) memory is supported; consequently, the buffers support only SSTL_1.8 V signal interfaces. The memory controller interface is fully configurable through a set of control registers. Features of the MCH memory controller include:

- The MCH System Memory Controller directly supports one or two channels of memory (each channel consisting of 64 data lines).

- Supports two memory addressing organization options:
    — The memory channels are asymmetric: "Stacked" channels are assigned addresses serially. Channel B addresses are assigned after all Channel A addresses.
    — The memory channels are interleaved: Addresses are ping-ponged between the channels after each cache line (64-B boundary).

- Available bandwidth up to:
    — 3.2 GB/s (DDR2 400) for single-channel mode
    — 6.4 GB/s in dual-channel interleaved mode assuming DDR2 400 MHz.
    — 8.5 GB/s in dual-channel interleaved mode assuming DDR2 533 MHz.

- Supports DDR2 memory DIMM frequencies of 400 MHz and 533 MHz. The speed used in all channels is the speed of the slowest DIMM in the system.

- I/O Voltage of 1.8 V for DDR2.

- Supports non-ECC and ECC memory.

- Supports 256-Mb, 512-Mb and 1-Gb DDR2 technologies

- Supports only x8, x16, DDR2 devices with four banks and also supports eight bank, 1-Gbit DDR2 devices.

- Supports opportunistic refresh

- In dual channel mode the MCH supports 64 simultaneously open pages (four ranks of eight bank devices* 2 channels)

- Supports Partial Writes to memory using Data Mask (DM) signals.

- Supports page sizes of 4 KB, 8 KB, and 16 KB.

- Supports a burst length of 8 for single-channel and dual-channel interleaved and asymmetric operating modes.

- Supports unbuffered DIMMs.

- SPD (Serial Presence Detect) scheme for DIMM detection support

- Suspend-to-RAM support using CKE

- Supports configurations defined in the JEDEC DDR2 DIMM specification only

The MCH supports a memory thermal management scheme to selectively manage reads and/or writes. Memory thermal management can be triggered either by on-die thermal sensor, or by preset limits. Management limits are determined by weighted sum of various commands that are scheduled on the memory interface.

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1.3.3   Direct Media Interface (DMI)

Direct Media Interface (DMI) is the chip-to-chip connection between the MCH and ICH6. This high-speed interface integrates advanced priority-based servicing allowing for concurrent traffic and true isochronous transfer capabilities. Base functionality is completely software transparent permitting current and legacy software to operate normally.

To provide for true isochronous transfers and configurable Quality of Service (QoS) transactions, the ICH6 supports two virtual channels on DMI: VC0 and VC1. These two channels provide a fixed arbitration scheme where VC1 is always the highest priority. VC0 is the default conduit of traffic for DMI and is always enabled. VC1 must be specifically enabled and configured at both ends of the DMI link (i.e., the ICH6 and MCH). Features of the DMI include:

- A chip-to-chip connection interface to ICH6
- 2 GB/s point-to-point DMI to ICH6 (1 GB/s each direction)
- 100 MHz reference clock (shared with PCI Express Graphics Attach).
- 32-bit downstream addressing
- APIC and MSI interrupt messaging support. Will send Intel-defined "End Of Interrupt" broadcast message when initiated by the processor.
- Message Signaled Interrupt (MSI) messages
- SMI, SCI and SERR error indication
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive, and LPC bus masters

1.3.4   PCI Express* Graphics Interface

The MCH contains a 16-lane (x16) PCI Express* port intended for an external PCI Express graphics card. The PCI Express port is compatible with the *PCI Express Base Specification* Revision 1.0a. The x16 port operates at a frequency of 2.5 Gb/s on each lane while employing 8b/10b encoding, and supports a maximum theoretical bandwidth of 4 Gb/s each direction.

Features of the PCI Express Interface include:

- One x16 PCI Express port intended for graphics attach, compatible with the PCI Express Base Specification revision 1.0a.

- Theoretical PCI Express transfer rate of 2.5 Gb/s.

- Raw bit-rate on the data pins of 2.5 Gb/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface

- Maximum theoretical realized bandwidth on the interface of 4 GB/s in each direction simultaneously, for an aggregate of 8 GB/s when (1)x16.

- PCI Express Graphics Extended Configuration Space. The first 256 bytes of configuration space alias directly to the PCI Compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.

- PCI Express Enhanced Addressing Mechanism. Accessing the device configuration space in a flat memory mapped fashion.

- Automatic discovery, negotiation, and training of link out of reset

- Supports traditional PCI style traffic (asynchronous snooped, PCI ordering)

- Supports traditional AGP style traffic (asynchronous non-snooped, PCI Express-relaxed ordering)

- Hierarchical PCI-compliant configuration mechanism for downstream devices (i.e., normal PCI 2.3 Configuration space as a PCI-to-PCI bridge)

- Supports "static" lane numbering reversal. This method of lane reversal is controlled by a Hardware Reset strap, and reverses both the receivers and transmitters for all lanes (e.g., TX15->TX0, RX15->RX0). This method is transparent to all external devices and is different than lane reversal as defined in the PCI Express Specification. In particular, link initialization is not affected by static lane reversal.

1.3.5 System Interrupts

The MCH interrupt support includes:

- Supports both 8259 and Pentium 4 processor FSB interrupt delivery mechanisms.

- Supports interrupts signaled as upstream Memory Writes from PCI Express and DMI
  — MSIs routed directly to FSB
  — From I/OxAPICs

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1.3.6   MCH Clocking

The differential FSB clock (HCLKP/HCLKN) is set to 200 MHz. This supports FSB transfer rates of 800 MT/s. The Host PLL generates 2X, 4X, and 8X versions of the host clock for internal optimizations. The MCH core clock is synchronized to the host clock.

The internal and external memory clocks of 133 MHz and 200 MHz are generated from one of two MCH PLLs that use the host clock as a reference. This includes 2X and 4X for internal optimizations.

The PCI Express core clock of 250 MHz is generated from a separate PCI Express PLL. This clock uses the fixed 100 MHz Serial Reference Clock (GCLKP/GCLKN) for reference.

All of the above mentioned clocks are capable of tolerating Spread Spectrum clocking as defined in the Clock Generator specification. Host, Memory, and PCI Express* x16 Graphics PLLs, and all associated internal clocks are disabled until PWROK is asserted.

1.3.7   Power Management

MCH Power Management support includes:

- PC99 suspend to DRAM support ("STR", mapped to ACPI state S3)
- SMRAM space remapping to A0000h (128 KB)
- Supports extended SMRAM space above 256 MB, additional 1-MB TSEG from the Base of graphics stolen memory (BSM) when enabled, and cacheable (cacheability controlled by processor)
- ACPI Rev 1.0 compatible power management
- Supports processor states: C0, C1, C2, C3, and C4
- Supports System states: S0, S1, S3, S4, and S5
- Supports processor Thermal Management 2 (TM2)
- Microsoft Windows NT* Hardware Design Guide v1.0 compliant

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2 *Signal Description*

This chapter provides a detailed description of MCH signals. The signals are arranged in functional groups according to their associated interface. The states of all of the signals during reset are provided in the Section 2.9.

The following notations are used to describe the signal type:

I	Input pin
O	Output pin
I/O	Bi-directional input/output pin
GTL+	Open Drain GTL+ interface signal. Refer to the GTL+ I/O Specification for complete details. The MCH integrates GTL+ termination resistors, and supports VTT of from 0.83 V to 1.65 V (including guardbanding).
PCIE	PCI-Express interface signals. These signals are compatible with PCI Express 1.0 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3 V tolerant. Differential voltage specification $= (|D+ - D-|) * 2 = 1.2$ V maximum Single-ended maximum = 1.5 V. Single-ended minimum = 0 V.
DMI	Direct Media Interface signals. These signals are compatible with PCI Express 1.0 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3 V tolerant. Differential voltage specification $= (|D+ - D-|) * 2 = 1.2$ V maximum. Single-ended maximum = 1.5 V. Single-ended minimum = 0 V.
CMOS	CMOS buffers. 1.5 V tolerant.
COD	CMOS Open Drain buffers. 2.5 V tolerant.
HVCMOS	High Voltage CMOS buffers. 2.5 V tolerant.
HVIN	High Voltage CMOS input-only buffers. 3.3 V tolerant.
SSTL-1.8	Stub Series Termination Logic. These are 1.8 V output capable buffers. 1.8 V tolerant.
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation.

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Figure 2-1. Intel® MCH Signal Interface Diagram
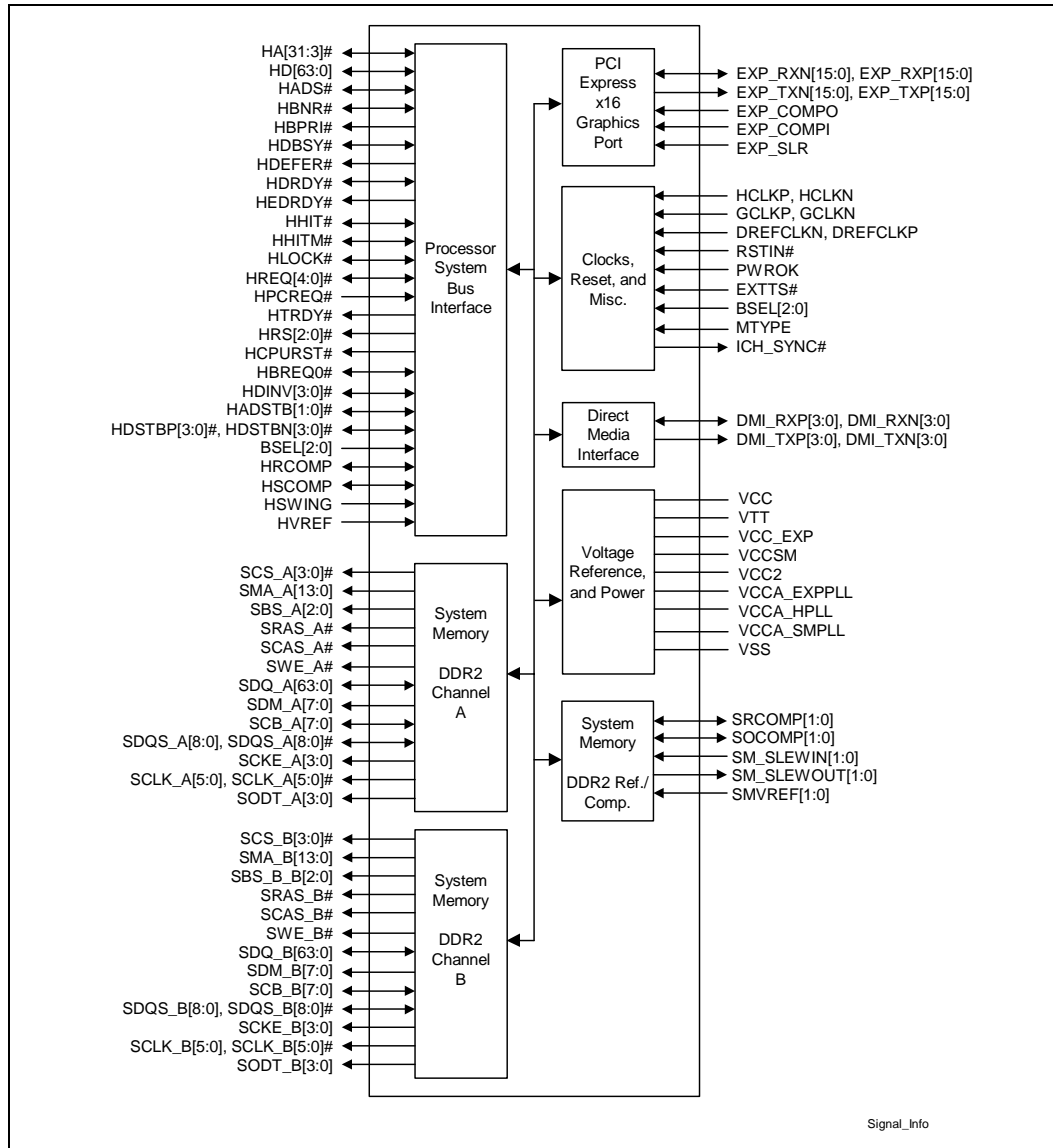
2.1 Host Interface Signals

Note: Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the Host Bus (V_{TT}).

Signal Name	Type	Description
HADS#	I/O GTL+	**Address Strobe:** The processor bus owner asserts HADS# to indicate the first of two cycles of a request phase. The MCH can assert this signal for snoop cycles and interrupt messages.
HBNR#	I/O GTL+	**Block Next Request:** This signal is used to block the current request bus owner from issuing new requests. This signal is used to dynamically control the processor bus pipeline depth.
HBPRI#	O GTL+	**Priority Agent Bus Request:** The MCH is the only Priority Agent on the processor bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
HBREQ0#	I/O GTL+	**Bus Request 0:** The MCH pulls the processor's bus HBREQ0# signal low during HCPURST#. The processor samples this signal on the active-to-inactive transition of HCPURST#. The minimum setup time for this signal is 4 HCLKs. The minimum hold time is 2 clocks and the maximum hold time is 20 HCLKs. HBREQ0# should be tri-stated after the hold time requirement has been satisfied.
HCPURST#	O GTL+	**CPU Reset:** The HCPURST# pin is an output from the MCH. The MCH asserts HCPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is de-asserted. The HCPURST# allows the processors to begin execution in a known state. Note that the Intel® ICH6 must provide processor frequency select strap set-up and hold times around HCPURST#. This requires strict synchronization between MCH HCPURST# de-assertion and the Intel® ICH6 driving the straps.
HDBSY#	I/O GTL+	**Data Bus Busy:** This signal is used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
HDEFER#	O GTL+	**Defer:** Signals that the MCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.
HDINV[3:0]#	I/O GTL+	**Dynamic Bus Inversion:** Driven along with the HD[63:0] signals**.** Indicates if the associated signals are inverted or not. HDINV[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16 bit group never exceeds 8. **HDINVx#** **Data Bits** HDINV3# HD[63:48] HDINV2# HD[47:32] HDINV1# HD[31:16] HDINV0# HD[15:0]

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Signal Name	Type	Description
HDRDY#	I/O GTL+	**Data Ready**: This signal is asserted for each cycle that data is transferred.
HEDRDY#	O GTL+	**Early Data Ready**: This signal indicates that the data phase of a read transaction will start on the bus exactly one common clock after assertion.
HA[31:3]#	I/O GTL+	**Host Address Bus:** HA[31:3]# connect to the processor address bus. During processor cycles, the HA[31:3]# are inputs. The MCH drives HA[31:3]# during snoop cycles on behalf of DMI and PCI Express Graphics initiators. HA[31:3]# are transferred at 2x rate.
HADSTB[1:0]#	I/O GTL+	**Host Address Strobe:** The source synchronous strobes used to transfer HA[31:3]# and HREQ[4:0] at the 2x transfer rate.
HD[63:0]	I/O GTL+	**Host Data:** These signals are connected to the processor data bus. Data on HD[63:0] is transferred at 4x rate. Note that the data signals may be inverted on the processor bus, depending on the HDINV[3:0]# signals.
HDSTBP[3:0]# HDSTBN[3:0]#	I/O GTL+	**Differential Host Data Strobes:** The differential source synchronous strobes are used to transfer HD[63:0]# and HDINV[3:0]# at 4x transfer rate. These signals are named this way because they are not level sensitive. Data is captured on the falling edge of both strobes. Hence, they are pseudo-differential, and not true differential. **Strobes** **Data** **Bits** HDSTBP3#, HDSTBN3# HD[63:48] HDINV3# HDSTBP2#, HDSTBN2# HD[47:32] HDINV2# HDSTBP1#, HDSTBN1# HD[31:16] HDINV1# HDSTBP0#, HDSTBN0# HD[15:0] HDINV0#
HHIT#	I/O GTL+	**Hit:** This signal indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HHITM# by the target to extend the snoop window.
HHITM#	I/O GTL+	**Hit Modified:** This signal indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. This signal is also driven in conjunction with HHIT# to extend the snoop window.
HLOCK#	I/O GTL+	**Host Lock:** All processor bus cycles sampled with the assertion of HLOCK# and HADS#, until the negation of HLOCK# must be atomic (i.e., no DMI or PCI Express Graphics accesses to DRAM are allowed when HLOCK# is asserted by the processor).
HPCREQ#	I GTL+ 2x	**Precharge Request:** The processor provides a "hint" to the MCH that it is OK to close the DRAM page of the memory read request with which the hint is associated. The MCH uses this information to schedule the read request to memory using the special "AutoPrecharge" attribute. This causes the DRAM to immediately close (Precharge) the page after the read data has been returned. This allows subsequent processor requests to more quickly access information on other DRAM pages, since it will no longer be necessary to close an open page prior to opening the proper page. Asserted by the requesting agent during both halves of Request Phase. The same information is provided in both halves of the request phase.

Signal Name	Type	Description
HREQ[4:0]#	I/O GTL+ 2x	**Host Request Command:** These signals define the attributes of the request. HREQ[4:0]# are transferred at 2x rate. They are asserted by the requesting agent during both halves of Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type. The transactions supported by the MCH Host Bridge are defined in the Host Interface section of this document.
HTRDY#	O GTL+	**Host Target Ready:** This signal indicates that the target of the processor transaction is able to enter the data transfer phase.
HRS[2:0]#	O GTL+	**Response Signals:** These signals indicate the type of response as shown below: 000 = Response type 001 = Idle state 010 = Retry response 011 = Deferred response 100 = Reserved (not driven by MCH) 101 = Hard Failure (not driven by MCH) 110 = No data response 111 = Implicit Writeback 111 = Normal data response
BSEL[2:0]	I CMOS	**Bus Speed Select:** At the de-assertion of RSTIN#, the value sampled on these pins determines the expected frequency of the bus.
HRCOMP	I/O CMOS	**Host RCOMP:** Used to calibrate the Host GTL+ I/O buffers. This signal is powered by the Host Interface termination rail (VTT).
HSCOMP	I/O CMOS	**Slew Rate Compensation:** Compensation for the Host Interface.
HSWING	I A	**Host Voltage Swing:** This signal provides the reference voltage used by FSB RCOMP circuits. HSWING is used for the signals handled by HRCOMP.
HVREF	I A	**Host Reference Voltage Reference:** Voltage input for the data, address, and common clock signals of the Host GTL interface.

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2.2 DDR2 DRAM Channel A Interface

Signal Name	Type	Description
SCLK_A[5:0]	O SSTL-1.8	**SDRAM Differential Clock:** (3 per DIMM). SCLK_Ax and its complement SCLK_Ax# signal make a differential clock pair output. The crossing of the positive edge of SCLK_Ax and the negative edge of its complement SCLK_Ax# are used to sample the command and control signals on the SDRAM.
SCLK_A[5:0]#	O SSTL-1.8	**SDRAM Complementary Differential Clock:** (3 per DIMM) These are the complementary differential DDR2 Clock signals.
SCS_A[3:0]#	O SSTL-1.8	**Chip Select:** (1 per Rank) These signals select particular SDRAM components during the active state. There is one chip select for each SDRAM rank.
SMA_A[13:0]	O SSTL-1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM
SBS_A[2:0]	O SSTL-1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank DDR2: 1-Gb technology is 8 banks.
SRAS_A#	O SSTL-1.8	**Row Address Strobe:** This signal is used with SCAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SCAS_A#	O SSTL-1.8	**Column Address Strobe:** This signal is used with SRAS_A# and SWE_A# (along with SCS_A#) to define the SDRAM commands.
SWE_A#	O SSTL-1.8	**Write Enable:** This signal is used with SCAS_A# and SRAS_A# (along with SCS_A#) to define the SDRAM commands.
SDQ_A[63:0]	I/O SSTL-1.8 2x	**Data Lines:** SDQ_A signals interface to the SDRAM data bus.
SDM_A[7:0]	O SSTL-1.8 2X	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_Ax signal for every data byte lane.
SCB_A[7:0]	I/O SSTL-1.8 2X	**ECC Check Byte:** These signals require a 6-layer board to be routed.
SDQS_A[8:0]	I/O SSTL-1.8 2x	**Data Strobes:** For DDR2, SDQS_Ax and its complement SDQS_Ax# signal make up a differential strobe pair. The data is captured at the crossing point of SDQS_Ax and its complement SDQS_Ax# during read and write transactions.
SDQS_A[8:0]#	I/O SSTL-1.8 2x	**Data Strobe Complements:** These signals are the complementary DDR2 strobe signals.
SCKE_A[3:0]	O SSTL-1.8	**Clock Enable:** (1 per Rank) SACKE is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.
SODT_A[3:0]	O SSTL-1.8	**On Die Termination:** Active On-die Termination Control signals for DDR2 devices.

2.3　DDR2 DRAM Channel B Interface

Signal Name	Type	Description
SCLK_B[5:0]	O SSTL-1.8	**SDRAM Differential Clock:** (3 per DIMM) SCLK_Bx and its complement SCLK_Bx# signal make a differential clock pair output. The crossing of the positive edge of SCLK_Bx and the negative edge of its complement SCLK_Bx# are used to sample the command and control signals on the SDRAM.
SCLK_B[5:0]#	O SSTL-1.8	**SDRAM Complementary Differential Clock:** (3 per DIMM) These are the complementary differential DDR2 clock signals.
SCS_B[3:0]#	O SSTL-1.8	**Chip Select:** (1 per Rank) These signals select particular SDRAM components during the active state. There is one chip select for each SDRAM rank
SMA_B[13:0]	O SSTL-1.8	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM
SBS_B[2:0]	O SSTL-1.8	**Bank Select:** These signals define which banks are selected within each SDRAM rank DDR2: 1-Gb technology is 8 banks.
SRAS_B#	O SSTL-1.8	**Row Address Strobe:** This signal is used with SCAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands
SCAS_B#	O SSTL-1.8	**Column Address Strobe:** This signal is used with SRAS_B# and SWE_B# (along with SCS_B#) to define the SDRAM commands.
SWE_B#	O SSTL-1.8	**Write Enable:** This signal is used with SCAS_B# and SRAS_B# (along with SCS_B#) to define the SDRAM commands.
SDQ_B[63:0]	I/O SSTL-1.8 2x	**Data Lines:** SDQ_Bx signals interface to the SDRAM data bus
SDM_B[7:0]	O SSTL-1.8 2x	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SDM_Bx signal for every data byte lane.
SCB_B[7:0]	I/O SSTL-1.8 2X	**ECC Check Byte:** These signals require a 6-layer board to be routed.
SDQS_B[8:0]	I/O SSTL-1.8 2x	**Data Strobes:** For DDR2, SDQS_Bx and its complement SDQS_Bx# make up a differential strobe pair. The data is captured at the crossing point of SDQS_Bx and its complement SDQS_Bx# during read and write transactions.
SDQS_B[8:0]#	I/O SSTL-1.8 2x	**Data Strobe Complements:** These signals are the complementary DDR2 strobe signals.
SCKE_B[3:0]	O SSTL-1.8	**Clock Enable:** (1 per Rank) SCKE_B is used to initialize the SDRAMs during power-up, to power-down SDRAM ranks, and to place all SDRAM ranks into and out of self-refresh during Suspend-to-RAM.
SODT_B[3:0]	O SSTL-1.8	**On Die Termination:** Active On-die Termination Control signals for DDR2 devices.

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2.4 DDR2 DRAM Reference and Compensation

Signal Name	Type	Description
SRCOMP[1:0]	I/O	**System Memory RCOMP**
SOCOMP[1:0]	I/O A	**DDR2 On-Die DRAM Over Current Detection (OCD) driver compensation**
SM_SLEWIN[1:0]	I A	**Buffer Slew Rate Input:** Slew Rate Characterization buffer input for X and Y orientation.
SM_SLEWOUT[1:0]	O A	**Buffer Slew Rate Output:** Slew Rate Characterization buffer output for X and Y orientation
SMVREF[1:0]	I A	**SDRAM Reference Voltage:** Reference voltage inputs for each DQ, DM, DQS, and DQS# input signals.

2.5 PCI Express* x16 Graphics Port Signals

Unless otherwise specified, PCI Express Graphics signals are AC coupled, so the only voltage specified is a maximum 1.2 V differential swing.

Signal Name	Type	Description
EXP_RXN[15:0] EXP_RXP[15:0]	I/O PCIE	**PCI Express Graphics Receive Differential Pair**
EXP_TXN[15:0] EXP_TXP[15:0]	O PCIE	**PCI Express Graphics Transmit Differential Pair**
EXP_COMPO	I A	**PCI Express Graphics Output Current Compensation** Note: EXP_COMP0 is used for DMI current compensation.
EXP_COMPI	I A	**PCI Express Graphics Input Current Compensation** Note: EXP_COMPI is used for DMI current compensation.
EXP_SLR	I CMOS	**PCI Express* Static Lane Reversal:** The MCH's PCI Express lane numbers are reversed. For example, the MCH PCI Express interface signals can be configured as follows: Ball / Normal Operation / Lane Reversed C10 — EXP_TXP0 — EXP_TXP15 A9 — EXP_TXP1 — EXP_TXP14 … — … — … N3 — EXP_TXP14… — EXP_TXP1… P1 — EXP_TXP15 — EXP_TXP0 0 = MCH's PCI Express lane numbers are reversed 1 = Normal operation

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2.6 Clocks, Reset, and Miscellaneous

Signal Name	Type	Description
HCLKP HCLKN	I CMOS	**Differential Host Clock In:** These pins receive a differential host clock from the external clock synthesizer. This clock is used by all of the MCH logic that is in the Host clock domain.
GCLKP GCLKN	I CMOS	**Differential PCI Express Graphics Clock In:** These pins receive a differential 100 MHz serial reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.
DREFCLKN DREFCLKP	I CMOS	**Display PLL Differential Clock In**
RSTIN#	I HVIN	**Reset In:** When asserted, this signal will asynchronously reset the MCH logic. This signal is connected to the PLTRST# output of the Intel® ICH6. All PCI Express Graphics Attach output signals will also tri-state compatible with *PCI Express* Specification* Rev 1.0a. This input should have a Schmitt trigger to avoid spurious resets. This signal is required to be 3.3 V tolerant.
PWROK	I HVIN	**Power OK:** When asserted, PWROK is an indication to the MCH that core power has been stable for at least 10 us.
EXTTS#	I HVCMOS	**External Thermal Sensor Input:** This signal may connect to a precision thermal sensor located on or near the DIMMs. If the system temperature reaches a dangerously high value, then this signal can be used to trigger the start of system thermal management. This signal is activated when an increase in temperature causes a voltage to cross some threshold in the sensor.
MTYPE	I CMOS	**Memory Type Select Strap.** This signal is a strapping option that indicates the type of system memory. This signal should be tied to ground indicating DDR2 memory.
ICH_SYNC#	O HVCMOS	**ICH Sync:** This signal is connected to the MCH_SYNCH# signal on the ICH6.

2.7 Direct Media Interface (DMI)

Signal Name	Type	Description
DMI_RXP[3:0] DMI_RXN[3:0]	I/O DMI	**Direct Media Interface:** These signals are the receive differential pair (Rx).
DMI_TXP[3:0] DMI_TXN[3:0]	O DMI	**Direct Media Interface:** These signals are the transmit differential pair (Tx).

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2.8   Power and Ground

Name	Voltage	Description
VCC	1.5 V	**Core Power.**
VTT	1.2 V	**Processor System Bus Power.**
VCC_EXP	1.5 V	**PCI Express* and DMI Power.**
VCCSM	1.8 V	**System Memory Power.** DDR2: VCCSM = 1.8 V
VCC2	2.5 V	**2.5 V CMOS Power.**
VCCA_EXPPLL	1.5 V	**PCI Express PLL Analog Power.**
VCCA_HPLL	1.5 V	**Host PLL Analog Power.**
VCCA_SMPLL	1.5 V	**System Memory PLL Analog Power.**
VSS	0 V	**Ground.**

2.9   Reset States and Pull-up/Pull-downs

This section describes the expected states of the MCH I/O buffers during and immediately after the assertion of RSTIN#. This table only refers to the contributions on the interface from the MCH and does **not** reflect any external influence (such as external pull-up/pull-down resistors or external drivers).

Legend:

CMCT: Common Mode Center Tapped. Differential signals are weakly driven to the common mode central voltage.

DRIVE: Strong drive (to normal value supplied by core logic if not otherwise stated)

TERM: Normal termination devices are turned on

LV: Low voltage

HV: High voltage

IN: Input buffer enabled

ISO: Isolate input buffer so that it does not oscillate if input left floating

TRI: Tri-state

PU: Weak internal pull-up

PD: Weak internal pull-down

STRAP: Strap input sampled during assertion or on the de-asserting edge of RSTIN#

Table 2-1. Host Interface Reset and S3 States

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
Host I/F	HCPURST#	O	DRIVE LV	TERM HV after approximately 1ms	TRI (No VTT)	
	HADSTB[1:0]#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HA[31:3]#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HD[63:0]	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HDSTBP[3:0]#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HDSTBN[3:0]#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HDINV[3:0]#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HADS#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HBNR#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HBPRI#	O	TERM HV	TERM HV	TRI (No VTT)	
	HDBSY#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HDEFER#	O	TERM HV	TERM HV	TRI (No VTT)	
	HDRDY#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HEDRDY#	O	TERM HV	TERM HV	TRI (No VTT)	
Host I/F	HHIT#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HHITM#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HLOCK#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HREQ[4:0]#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HTRDY#	O	TERM HV	TERM HV	TRI (No VTT)	
	HRS[2:0]#	O	TERM HV	TERM HV	TRI (No VTT)	
	HBREQ0#	I/O	TERM HV	TERM HV	TRI (No VTT)	
	HPCREQ#	I	TERM HV	TERM HV	TRI (No VTT)	
	HVREF	I	IN	IN	TRI	
	HRCOMP	I/O	TRI	TRI after RCOMP	TRI	20 Ω resistor for board with target impedance of 60 Ω
	HSWING	I	IN	IN		
	HSCOMP	I/O	TRI	TRI	TRI	

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Table 2-2. System Memory Reset and S3 States

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
System Memory	**Channel A**					
	SCLK_A[5:0]	O	TRI	TRI	TRI	
	SCLK_A[5:0]#	O	TRI	TRI	TRI	
	SCS_A[3:0]#	O	TRI	TRI	TRI	
	SMA_A[13:0]	O	TRI	TRI	TRI	
	SBS_A[2:0]	O	TRI	TRI	TRI	
	SRAS_A#	O	TRI	TRI	TRI	
	SCAS_A#	O	TRI	TRI	TRI	
	SWE_A#	O	TRI	TRI	TRI	
	SDQ_A[63:0]	I/O	TRI	TRI	TRI	
	SDM_A[7:0]	O	TRI	TRI	TRI	
	SCB_A[7:0]	I/O	TRI	TRI	TRI	
	SDQS_A[8:0]	I/O	TRI	TRI	TRI	
	SDQS_A[8:0]#	I/O	TRI	TRI	TRI	
	SCKE_A[3:0]	O	LV	LV	LV	
	SODT_A[3:0]	O	LV	LV	LV	
System Memory	**Channel B**					
	SCLK_B[5:0]	O	TRI	TRI	TRI	
	SCLK_B[5:0]#	O	TRI	TRI	TRI	
	SCS_B[3:0]#	O	TRI	TRI	TRI	
	SMA_B[13]	O	TRI	TRI	TRI	
	SMA_B[12:11]	O	LV	LV	LV	
	SMA_B[10:8]	O	TRI	TRI	TRI	
	SMA_B[7]	O	LV	LV	LV	
	SMA_B[6:0]	O	TRI	TRI	TRI	
	SBS_B[2]	O	LV	LV	LV	
	SBS_B[1:0]	O	TRI	TRI	TRI	
	SRAS_B#	O	TRI	TRI	TRI	
	SCAS_B#	O	TRI	TRI	TRI	
	SWE_B#	O	TRI	TRI	TRI	
	SDQ_B[63:0]	I/O	TRI	TRI	TRI	
	SDM_B[7:0]	O	TRI	TRI	TRI	
	SCB_B[7:0]	I/O	TRI	TRI	TRI	
	SDQS_B[8:0]	I/O	TRI	TRI	TRI	

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
	SDQS_B[8:0]#	I/O	TRI	TRI	TRI	
	SCKE_B[3:0]	O	LV	LV	LV	
	SODT_B[3:0]	O	LV	LV	LV	
	SRCOMP0	I/O	TRI	TRI (after RCOMP)	TRI	
	SRCOMP1	I/O	TRI	TRI (after RCOMP)	TRI	
	SM_SLEWIN[1:0]	I	IN	IN	IN	
	SM_SLEWOU[1:0]	O	TRI	TRI (after RCOMP)	TRI	
	SMVREF[1:0]	I	IN	IN	IN	
	SOCOMP[1:0]	I/O	TRI	TRI	TRI	DDR2: 40 Ω resistor to ground

Table 2-3. PCI Express* Graphics x16 Port Reset and S3 States

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
PCI Express*-Graphics	EXP_RXN[15:0]	I/O	CMCT	CMCT	CMCT	
	EXP_RXP[15:0]	I/O	CMCT	CMCT	CMCT	
	EXP_TXN[15:0]	O	CMCT 1.0 V	CMCT 1.0 V	CMCT 1.0 V	
	EXP_TXP[15:0]	O	CMCT 1.0 V	CMCT 1.0 V	CMCT 1.0 V	
	EXP_COMPO	I	TRI	TRI (after RCOMP)	TRI	
	EXP_COMPI	I	TRI	TRI (after RCOMP)	TRI	

Table 2-4. DMI Reset and S3 States

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
DMI	DMI_RXN[3:0]	I/O	CMCT	CMCT	CMCT	
	DMI_RXP[3:0]	I/O	CMCT	CMCT	CMCT	
	DMI_TXN[3:0]	O	CMCT 1.0 V	CMCT 1.0 V	CMCT 1.0 V	
	DMI_TXP[3:0]	O	CMCT 1.0 V	CMCT 1.0 V	CMCT 1.0 V	

Table 2-5. Clocking Reset and S3 States

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
Clocks	HCLKN	I	IN	IN	IN	
	HCLKP	I	IN	IN	IN	
	GCLKN	I	IN	IN	IN	
	GCLKP	I	IN	IN	IN	
	DREFCLKN	I	IN	IN	IN	
	DREFCLKP	I	IN	IN	IN	

Table 2-6. Miscellaneous Reset and S3 States

Interface	Signal Name	I/O	State During RSTIN# Assertion	State After RSTIN# De-assertion	S3	Pull-up/ Pull-down
Misc.	RSTIN#	I	IN	IN	IN	
	PWROK	I	HV	HV	HV	
	EXTTS#	I	PU	PU	PU	
	BSEL[2:0]	I	TRI	TRI	TRI	
	MTYPE	I	TERM HV	TERM HV	TERM HV	
	EXP_SLR	I	TERM HV	TERM HV	TERM HV	
	ICH_SYNC#	O	PU	PU	PU	

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3 Register Description

The MCH contains two sets of software accessible registers, accessed via the processor I/O address space: Control registers and internal configuration registers.

- Control registers are I/O mapped into the processor I/O space that control access to PCI and PCI Express configuration space (see Section 3.4).

- Internal configuration registers residing within the MCH are partitioned into two logical device register sets ("logical" since they reside within a single physical device). The first register set is dedicated to Host Bridge functionality (i.e. DRAM configuration, other chip-set operating parameters and optional features). The second register block is dedicated to Host-PCI Express Bridge functions (controls PCI Express interface configurations and operating parameters).

The MCH internal registers (I/O Mapped, Configuration and PCI Express Extended Configuration registers) are accessible by the processor. The registers that reside within the lower 256 bytes of each device can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFIG_ADDRESS that can only be accessed as a DWord. All multi-byte numeric fields use "little-endian" ordering (i.e., lower addresses contain the least significant parts of the field). Registers that reside in bytes 256 through 4095 of each device may only be accessed using memory mapped transactions in DWord (32-bit) quantities.

3.1 Register Terminology

The following table shows the register-related terminology that is used.

Item	Description
RO	Read Only bit(s). Writes to these bits have no effect.
RS/WC	Read Set / Write Clear bit(s). These bits are set to '1' when read and then will continue to remain set until written. A write of '1' clears (sets to '0') the corresponding bit(s) and a write of '0' has no effect.
R/W	Read / Write bit(s). These bits can be read and written.
R/WC	Read / Write Clear bit(s). These bits can be read. Internal events may set this bit. A write of '1' clears (sets to '0') the corresponding bit(s) and a write of '0' has no effect.
R/WC/S	Read / Write Clear / Sticky bit(s). These bits can be read. Internal events may set this bit. A write of '1' clears (sets to '0') the corresponding bit(s) and a write of '0' has no effect. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express* related bits a cold reset is "Power Good Reset" as defined in the *PCI Express* Specification*).
R/W/L	Read / Write / Lockable bit(s). These bits can be read and written. Additionally there is a bit (which may or may not be a bit marked R/W/L) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/W/S	Read / Write / Sticky bit(s). These bits can be read and written. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is "Power Good Reset" as defined in the *PCI Express* Specification*).

Item	Description
R/WSC	Read / Write Self Clear bit(s). These bits can be read and written. When the bit is '1', hardware may clear the bit to '0' based upon internal events, possibly sooner than any subsequent read could retrieve a '1'.
R/WSC/L	Read / Write Self Clear / Lockable bit(s). These bits can be read and written. When the bit is '1', hardware may clear the bit to '0' based upon internal events, possibly sooner than any subsequent read could retrieve a '1'. Additionally there is a bit (which may or may not be a bit marked R/W/L) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/WC	Read Write Clear bit(s). These bits can be read and written. However, a write of '1' clears (sets to '0') the corresponding bit(s) and a write of '0' has no effect.
R/WO	Write Once bit(s). Once written, bits with this attribute become Read Only. These bits can only be cleared by a Reset.
W	Write Only. Whose bits may be written, but will always-return zeros when read. They are used for write side effects. Any data written to these registers cannot be retrieved.
Reserved Bits	Some of the MCH registers described in this section contain reserved bits. These bits are labeled "Reserved". Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions and then written back. Note the software does not need to perform read, merge, and write operation for the configuration address register.
Reserved Registers	In addition to reserved bits within a register, the MCH contains address locations in the configuration space of the Host Bridge entity that are marked either "Reserved" or "Intel Reserved". The MCH responds to accesses to "Reserved" address locations by completing the host cycle. When a "Reserved" register location is read, a zero value is returned. ("Reserved" registers can be 8-, 16-, or 32-bits in size). Writes to "Reserved" registers have no effect on the MCH. Registers that are marked as "Intel Reserved" must not be modified by system software. Writes to "Intel Reserved" registers may cause system failure. Reads from "Intel Reserved" registers may return a non-zero value.
Default Value	Upon a Full Reset, the MCH sets its entire set of internal configuration registers to predetermined default states. Some register values at reset are determined by external strapping options. The default state represents the minimum functionality feature set required to successfully bringing up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program the MCH registers accordingly.

3.2   Platform Configuration

In platforms that support DMI (e.g. this MCH) the configuration structure is significantly different from previous Hub architectures. The DMI physically connects the MCH and the Intel ICH6; so, from a configuration standpoint, the DMI is logically PCI bus 0. As a result, all devices internal to the MCH and the Intel ICH6 appear to be on PCI bus 0.

The ICH6 internal LAN controller does not appear on bus 0; it appears on the external PCI bus (whose number is configurable).

The system's primary PCI expansion bus is physically attached to the Intel ICH6 and, from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge and therefore has a programmable PCI Bus number. The PCI Express Graphics Attach appears to system software to be a real PCI bus behind a PCI-to-PCI bridge that is a device resident on PCI bus 0.

Note: A physical PCI bus 0 does not exist and that DMI and the internal devices in the MCH and Intel ICH6 logically constitute PCI Bus 0 to configuration software. This is shown in Figure 3-1.

Figure 3-1. Conceptual Intel® 925X Express Chipset Platform PCI Configuration Diagram

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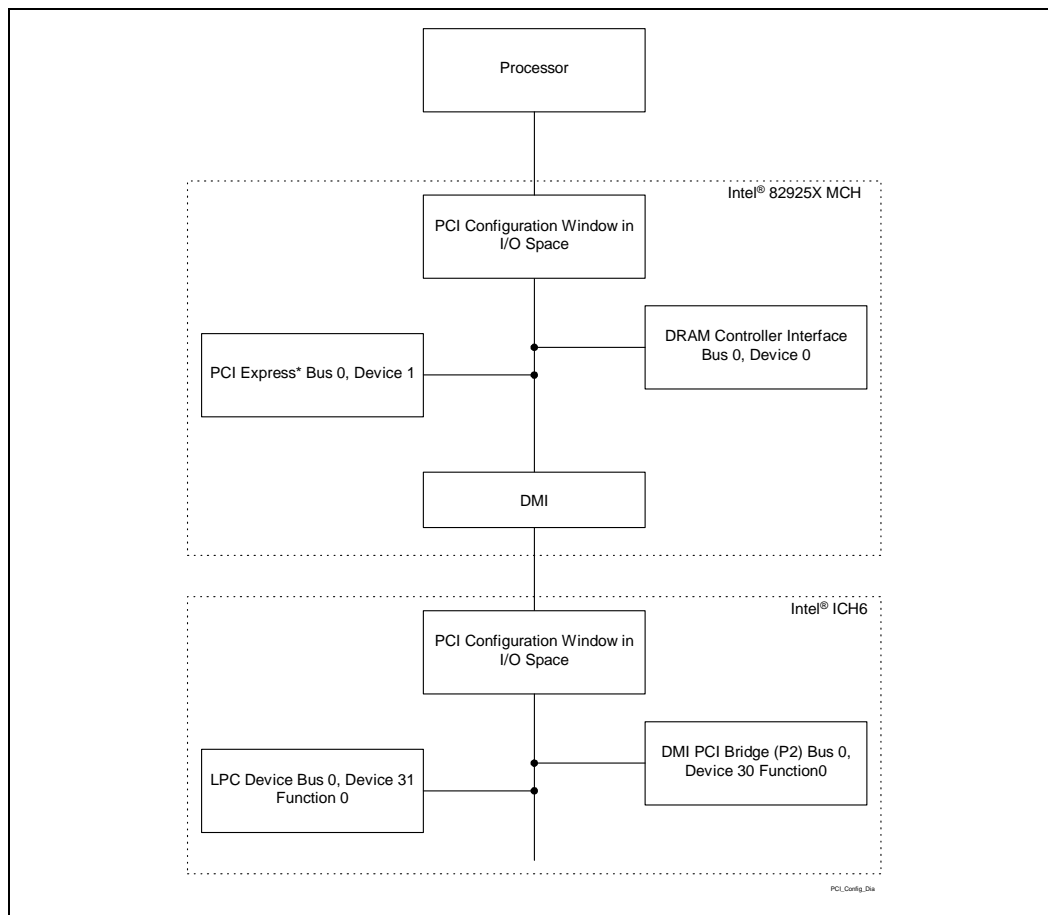
The MCH contains the following PCI devices within a single physical component. The configuration registers for the devices are mapped as devices residing on PCI bus 0.

- **Device 0 – Host Bridge/DRAM Controller**: Logically this appears as a PCI device residing on PCI bus 0. Device 0 contains the standard PCI header registers, PCI Express base address register, DRAM control (including thermal/throttling control), and configuration for the DMI and other MCH specific registers.

- **Device 1– Host-PCI Express Bridge**. Logically this appears as a "virtual" PCI-to-PCI bridge residing on PCI bus 0 and is compliant with *PCI Express* Specification* Revision 1.0a. Device 1 contains the standard PCI-to-PCI bridge registers and the standard PCI Express/PCI configuration registers (including the PCI Express memory address mapping). It also contains Isochronous and Virtual Channel controls in the PCI Express extended configuration space.

Table 3-1. Device Number Assignment for Internal MCH Devices

MCH Function	Device#
Host Bridge / DRAM Controller	Device 0
Host-to-PCI Express* Bridge (virtual P2P)	Device 1

3.3 General Routing Configuration Accesses

The MCH supports two PCI related interfaces: DMI and PCI Express. PCI and PCI Express configuration cycles are selectively routed to one of these interfaces. The MCH is responsible for routing configuration cycles to the proper interface. Configuration cycles to the Intel ICH6 internal devices and Primary PCI (including downstream devices) are routed to the Intel ICH6 via DMI. Configuration cycles to both the PCI Express Graphics PCI compatibility configuration space and the PCI Express Graphics extended configuration space are routed to the PCI Express Graphics port.

A detailed description of the mechanism for translating processor I/O bus cycles to configuration cycles is described below.

3.3.1 Standard PCI Bus Configuration Mechanism

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to 8 functions with each function containing up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the MCH.

The configuration access mechanism makes use of the CONFIG_ADDRESS Register (at I/O address 0CF8h though 0CFBh) and CONFIG_DATA Register (at I/O address 0CFCh though 0CFFh). To reference a configuration register a DW I/O write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFIG_ADDRESS [31] must be 1 to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA will result in the MCH translating the CONFIG_ADDRESS into the appropriate configuration cycle.

The MCH is responsible for translating and routing the processor's I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal MCH configuration registers, DMI, or PCI Express.

3.3.2 Logical PCI Bus 0 Configuration Mechanism

The MCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0 the configuration cycle is targeting a PCI Bus 0 device. The Host-DMI Bridge entity within the MCH is hardwired as Device 0 on PCI Bus 0. The Host-PCI Express Bridge entity within the MCH is hardwired as Device 1 on PCI Bus 0. The Intel ICH6 decodes the Type 0 access and generates a configuration access to the selected internal device.

3.3.3 Primary PCI and Downstream Configuration Mechanism

If the Bus Number in the CONFIG_ADDRESS is non-zero, and falls outside the range claimed by the Host-PCI Express bridge (not between upper bound in device's Subordinate Bus Number register and lower bound in device's Secondary Bus Number register), the MCH would generate a Type 1 DMI configuration cycle. This DMI configuration cycle will be sent over the DMI.

If the cycle is forwarded to the Intel ICH6 via the DMI, the Intel ICH6 compares the non-zero Bus Number with the Secondary Bus Number and Subordinate Bus Number registers of its P2P bridges to determine if the configuration cycle is meant for ICH6 PCI Express ports one of the Intel ICH6's devices, the DMI, or a downstream PCI bus.

Figure 3-2. DMI Type 0 Configuration Address Translation

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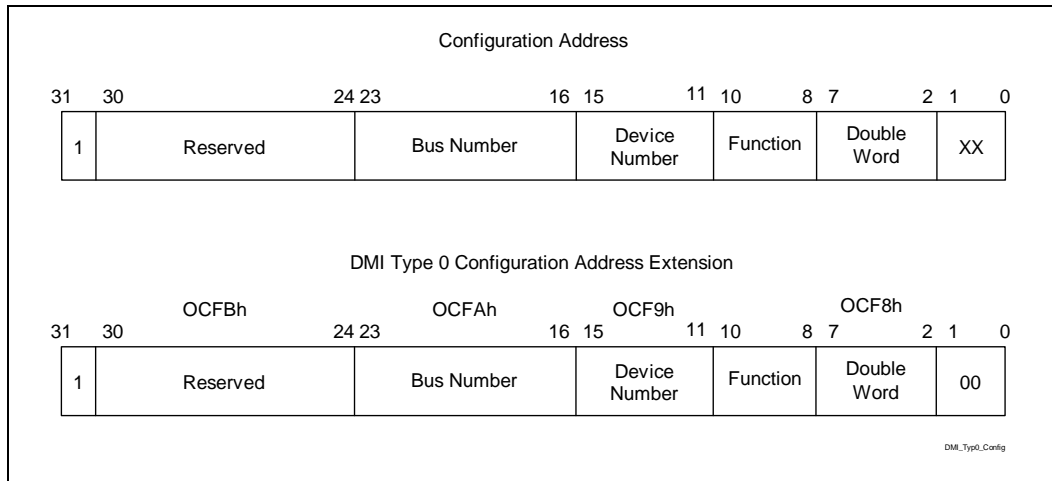
Figure 3-3. DMI Type 1 Configuration Address Translation
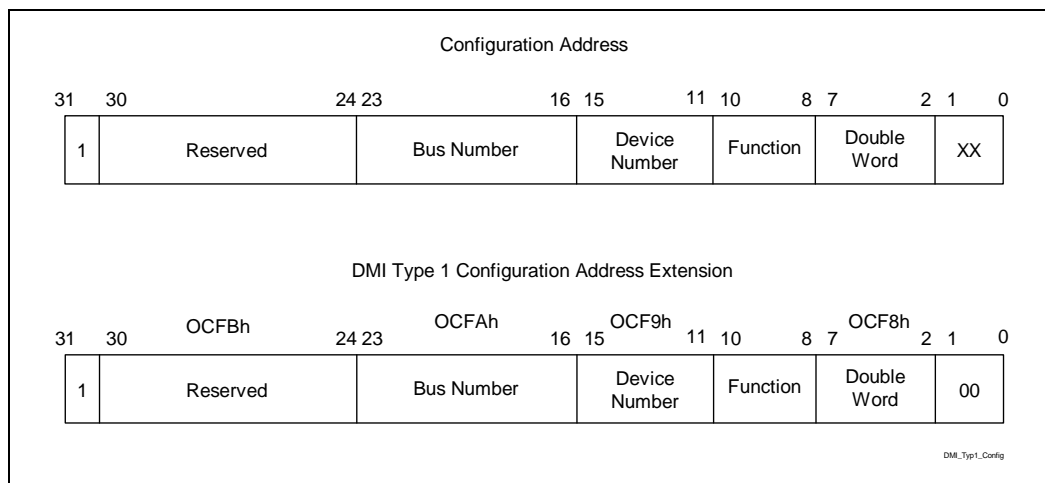
3.3.4 PCI Express* Enhanced Configuration Mechanism

PCI Express extends the configuration space to 4096 bytes per device/function as compared to 256 bytes allowed by PCI Specification, Revision 2.3. PCI Express configuration space is divided into a PCI 2.3 compatible region that consists of the first 256B of a logical device's configuration space and a PCI Express extended region that consists of the remaining configuration space.

The PCI compatible region can be accessed using either the mechanism defined in the previous section or using the enhanced PCI Express configuration access mechanism described in this section. The extended configuration registers may only be accessed using the enhanced PCI Express configuration access mechanism. To maintain compatibility with PCI configuration addressing mechanisms, system software must access the extended configuration space using 32-bit operations (32-bit aligned) only. These 32-bit operations include byte enables allowing only appropriate bytes within the DWord to be accessed. Locked transactions to the PCI Express memory mapped configuration address space are not supported. All changes made using either access mechanism are equivalent. The enhanced PCI Express configuration access mechanism uses a flat memory-mapped address space to access device configuration registers. This address space is reported by the system firmware to the operating system. The PCIEXBAR register defines the base address for the 256-MB block of addresses below top of addressable memory (currently 4 GB) for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. The PCI Express Configuration Transaction Header includes an additional 4 bits (Extended Register Address[3:0]) between the Function Number and Register Address fields to provide indexing into the 4 KB of configuration space allocated to each potential device. For PCI Compatible Configuration Requests, the Extended Register Address field must be all zeros.

![intel logo](int_el)

Figure 3-4. Memory Map to PCI Express* Device Configuration Space
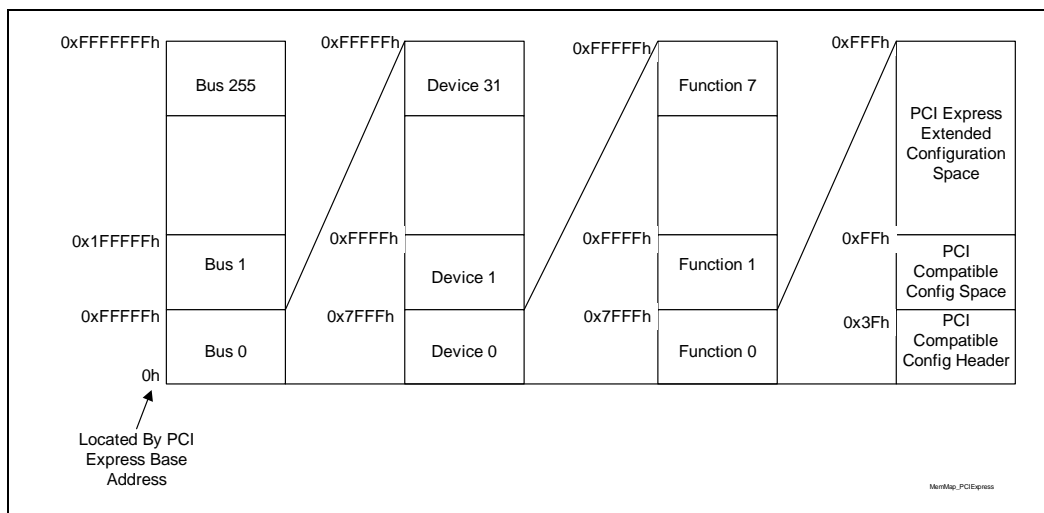
Just the same as with PCI devices, each device is selected based on decoded address information that is provided as a part of the address portion of Configuration Request packets. A PCI Express device will decode all address information fields (bus, device, function, and extended address numbers) to provide access to the correct register.

To access this space (steps 1, 2, 3 are performed only once by BIOS)

1. Use the PCI compatible configuration mechanism to enable the PCI Express enhanced configuration mechanism by writing 1 to bit 31 of the DEVEN register.

2. Use the PCI compatible configuration mechanism to write an appropriate PCI Express base address into the PCIEXBAR register.

3. Calculate the host address of the register you wish to set using (PCI Express base + (bus number * 1 MB) + (device number * 32 KB) + (function number * 4 KB) + (1 B * offset within the function) = host address).

4. Use a memory write or memory read cycle to the calculated host address to write to or read from that register.
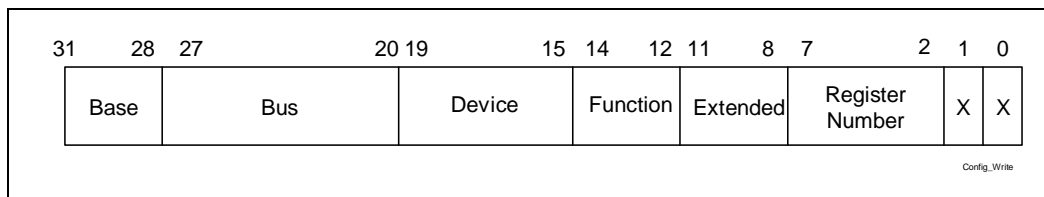
PCI Express Configuration Writes

Internally the host interface unit translates writes to PCI Express extended configuration space to configurations on the backbone. Writes to extended space are posted on the FSB, but non-posted on the PCI Express* x16 Graphics Interface or DMI pins (i.e., translated to configuration writes).

See the *PCI Express Specification* for more information on both the PCI 2.3 compatible and PCI Express enhanced configuration mechanism and transaction rules.

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3.3.5   Intel® 82925X MCH Configuration Cycle Flowchart

Figure 3-5. Intel® 82925X MCH Configuration Cycle Flowchart

Config_Cyc_Flow_915
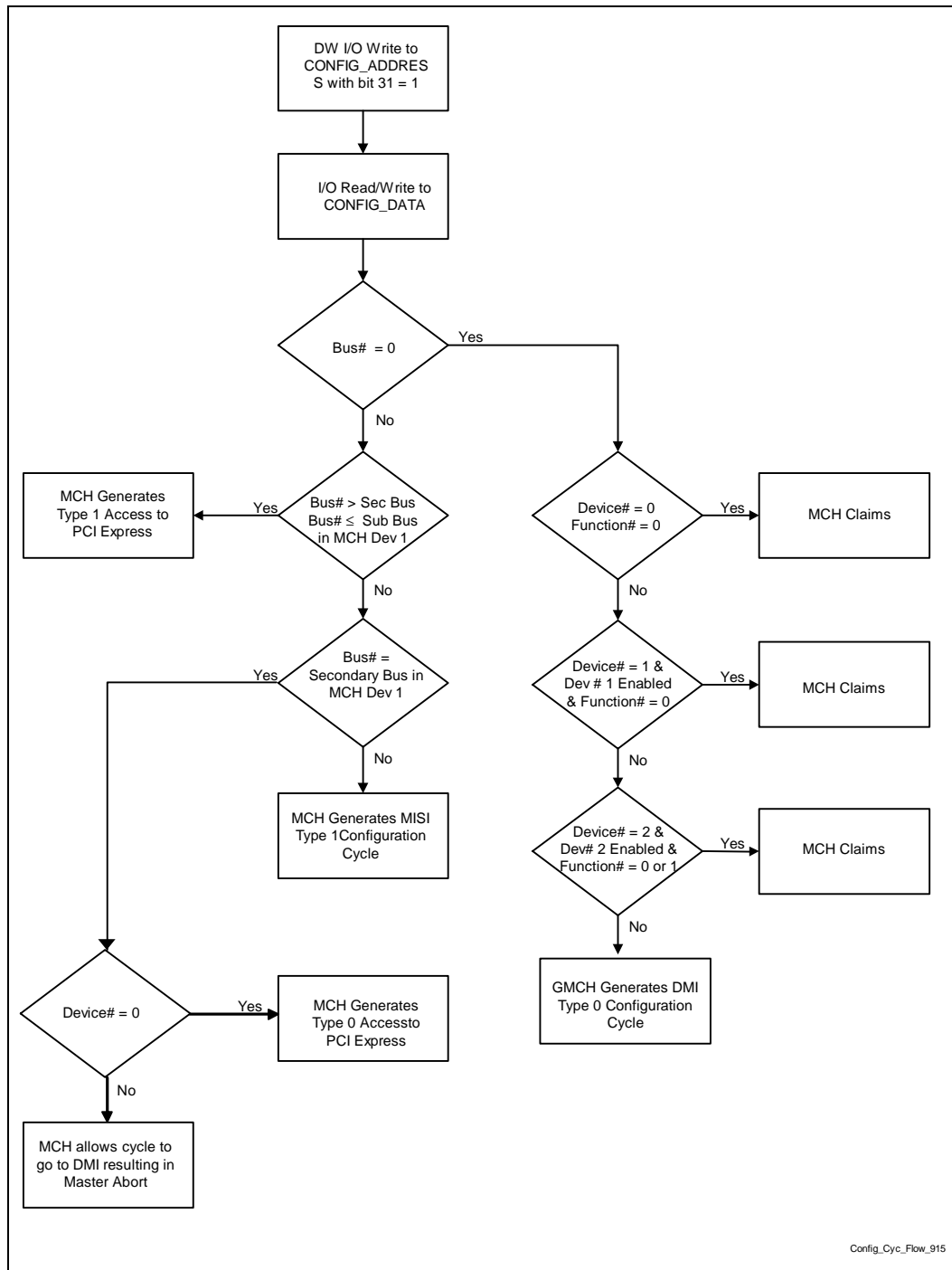
3.4   I/O Mapped Registers

The MCH contains two registers that reside in the processor I/O address space – the Configuration Address (CONFIG_ADDRESS) Register and the Configuration Data (CONFIG_DATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.4.1   CONFIG_ADDRESS—Configuration Address Register

I/O Address: 0CF8h Accessed as a DWord
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_ADDRESS is a 32-bit register that can be accessed only as a DW. A Byte or Word reference will "pass through" the Configuration Address Register and DMI onto the Primary PCI bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Access & Default	Description
31	R/W 0b	**Configuration Enable (CFGE):** 1 = Enable 0 = Disable
30:24		Reserved
23:16	R/W 00h	**Bus Number:** If the Bus Number is programmed to 00h the target of the Configuration Cycle is a PCI Bus #0 agent. If this is the case and the MCH is not the target (i.e., the device number is ≥ 3 and not equal to 7), then a DMI Type 0 Configuration Cycle is generated. If the Bus Number is non-zero, and does not fall within the ranges enumerated by device 1's Secondary Bus Number or Subordinate Bus Number Register, then a DMI Type 1 Configuration Cycle is generated. If the Bus Number is non-zero and matches the value programmed into the Secondary Bus Number Register of device 1, a Type 0 PCI configuration cycle will be generated on PCI Express Graphics. If the Bus Number is non-zero, greater than the value in the Secondary Bus Number register of device 1 and less than or equal to the value programmed into the Subordinate Bus Number Register of device 1 a Type 1 PCI configuration cycle will be generated on PCI Express Graphics. This field is mapped to byte 8 [7:0] of the request header format during PCI Express Configuration cycles and A[23:16] during the DMI Type 1 configuration cycles.
15:11	R/W 00h	**Device Number:** This field selects one agent on the PCI bus selected by the Bus Number. When the Bus Number field is "00", the MCH decodes the Device Number field. The MCH is always Device Number 0 for the Host bridge entity, Device Number 1 for the Host-PCI Express entity. Therefore, when the Bus Number =0 and the Device Number equals 0, 1, or 2 the internal MCH devices are selected. This field is mapped to byte 6 [7:3] of the request header format during PCI Express Configuration cycles and A [15:11] during the DMI configuration cycles.

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Bit	Access & Default	Description
10:8	R/W 000b	**Function Number:** This field allows the configuration registers of a particular function in a multi-function device to be accessed. The MCH ignores configuration cycles to its internal devices if the function number is not equal to 0 or 1. This field is mapped to byte 6 [2:0] of the request header format during PCI Express Configuration cycles and A[10:8] during the DMI configuration cycles.
7:2	R/W 00h	**Register Number:** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to byte 7 [7:2] of the request header format during PCI Express Configuration cycles and A[7:2] during the DMI Configuration cycles.
1:0		Reserved

3.4.2 CONFIG_DATA—Configuration Data Register

I/O Address: 0CFCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

CONFIG_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Bit	Access & Default	Description
31:0	R/W 0000 0000h	**Configuration Data Window (CDW):** If bit 31 of CONFIG_ADDRESS is 1, any I/O access to the CONFIG_DATA register will produce a configuration transaction using the contents of CONFIG_ADDRESS to determine the bus, device, function, and offset of the register to be accessed.

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4 Host Bridge/DRAM Controller Registers (D0:F0)

The DRAM Controller registers are in Device 0 (D0), Function 0 (F0).

Warning: Address locations that are not listed are considered Reserved registers locations. Reads to Reserved registers may return non-zero values. Writes to reserved locations may cause system failures.

All registers that are defined in the PCI 2.3 specification, but are not necessary or implemented in this component are not included in this document. The reserved/unimplemented space in the PCI configuration header space is not documented as such in this summary.

Table 4-1. Device 0 Function 0 Register Address Map Summary

Address Offset	Register Symbol	Register Name	Default Value	Access
00h–01h	VID	Vendor Identification	8086h	RO
02h–03h	DID	Device Identification	2580h	RO
04h–05h	PCICMD	PCI Command	0006h	RO, R/W
06h–07h	PCISTS	PCI Status	0090h	RO, R/W/C
08h	RID	Revision Identification	00h	RO
09h–0Bh	CC	Class Code	060000h	RO
0Ch	—	**Reserved**	—	—
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HDR	Header Type	00h	RO
0Fh–2Bh	—	**Reserved**	—	—
2Ch–2Dh	SVID	Subsystem Vendor Identification	0000h	R/W/O
2Eh–2Fh	SID	Subsystem Identification	0000h	R/W/O
30h–33h	—	**Reserved**	—	—
34h	CAPPTR	Capabilities Pointer	E0h	RO
35h–3Fh	—	**Reserved**	—	—
40h–43h	EPBAR	Egress Port Base Address	00000000h	RO
44h–47h	MCHBAR	MCH Memory Mapped Register Range Base Address	00000000h	R/W
48h–4Bh	PCIEXBAR	PCI Express* Register Range Base Address	E0000000h	R/W
4Ch–4Fh	DMIBAR	Root Complex Register Range Base Address	00000000h	R/W

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Address Offset	Register Symbol	Register Name	Default Value	Access
52h–53h	—	**Reserved**	—	—
54h–57h	DEVEN	Device Enable	00000019h	R/W
58h–5Bh	DEAP	DRAM Error Address Pointer	00000000h	RO/S
5Ch	DERRSYN	DRAM Error Syndrome	00h	RO/S
5Dh	DERRDST	DRAM Error Destination	00h	RO/S
5Fh–8Fh	—	**Reserved**	—	—
90h	PAM0	Programmable Attribute Map 0	00h	R/W
91h	PAM1	Programmable Attribute Map 1	00h	R/W
92h	PAM2	Programmable Attribute Map 2	00h	R/W
93h	PAM3	Programmable Attribute Map 3	00h	R/W
94h	PAM4	Programmable Attribute Map 4	00h	R/W
95h	PAM5	Programmable Attribute Map 5	00h	R/W
96h	PAM6	Programmable Attribute Map 6	00h	R/W
97h	LAC	Legacy Access Control	00h	R/W
98–9Bh	—	**Reserved**	—	—
9Ch	TOLUD	Top of Low Usable DRAM	08h	R/W
9Dh	SMRAM	System Management RAM Control	00h	RO, R/W/L
9Eh	ESMRAMC	Extended System Management RAM Control	00h	RO, R/W/L
9F–C7h	—	**Reserved**	—	—
C8h–C9h	ERRSTS	Error Status	0000h	RO, R/W/L
CAh–CBh	ERRCMD	Error Command	0000h	R/W
CCh—CDh	SMICMD	SMI Command	0000h	R/W
CEh—CFh	SCICMD	SCI Command	0000h	R/W
D0h–DBh	—	**Reserved**	—	—
DCh–DFh	SKPD	Scratchpad Data	00000000h	R/W
E0h–E8h	CAPID0	Capability Identifier	000000000001090009h	RO
E9h–FFh	—	**Reserved**	—	—
100h	C0DRB0	Channel A DRAM Rank Boundary Address 0	00h	R/W
101h	C0DRB1	Channel A DRAM Rank Boundary Address 1	00h	R/W
102h	C0DRB2	Channel A DRAM Rank Boundary Address 2	00h	R/W
103h	C0DRB3	Channel A DRAM Rank Boundary Address 3	00h	R/W
104h–107h	—	**Reserved**	—	—
108h	C0DRA0	Channel A DRAM Rank 0,1 Attribute	00h	R/W
109h	C0DRA2	Channel A DRAM Rank 2,3 Attribute	00h	R/W

Address Offset	Register Symbol	Register Name	Default Value	Access
10Ah–10Bh	—	**Reserved**	—	—
10Ch	C0DCLKDIS	Channel A DRAM Clock Disable	00h	R/W
10Dh	—	**Reserved**	—	—
10E–10F	C0BNKARC	Channel A DRAM Bank Architecture	0000h	R/W
110h–113h	—	**Reserved**	—	—
114h–117h	C0DRT1	Channel A DRAM Timing Register	900122h	R/W
118h–11Fh	—	**Reserved**	—	—
120h–123h	C0DRC0	Channel A DRAM Controller Mode 0	00000000h	R/W, RO
124h–17Fh	—	**Reserved**	—	—
180h	C1DRB0	Channel B DRAM Rank Boundary Address 0	00h	R/W
181h	C1DRB1	Channel B DRAM Rank Boundary Address 1	00h	R/W
182h	C1DRB2	Channel B DRAM Rank Boundary Address 2	00h	R/W
183h	C1DRB3	Channel B DRAM Rank Boundary Address 3	00h	R/W
184h–187h	—	**Reserved**	—	—
188h	C1DRA0	Channel B DRAM Rank 0,1 Attribute	00h	R/W
189h	C1DRA2	Channel B DRAM Rank 2,3 Attribute	00h	R/W
18Ah–18Bh	—	**Reserved**	—	—
18Ch	C1DCLKDIS	Channel B DRAM Clock Disable	00h	R/W
18Dh	—	**Reserved**	—	—
18Eh–18Fh	C1BNKARC	Channel B Bank Architecture	0000h	R/W
190h–193h	—	**Reserved**	—	—
194h	C1DRT1	Channel B DRAM Timing Register 1	900122h	R/W, RO
195h–19Fh	—	**Reserved**	—	—
1A0h–1A3h	C1DRC0	Channel B DRAM Controller Mode 0	00000000h	R/W, RO
1A4h–F0Fh	—	**Reserved**	—	—
F10h–F13h	PMCFG	Power Management Configuration	00000000h	R/W
F14h	PMSTS	Power Management Status	00000000h	R/W/C/S

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4.1 Device 0 Function 0 PCI Configuration Register Details

4.1.1 VID—Vendor Identification (D0:F0)

PCI Device: 0
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

4.1.2 DID—Device Identification (D0:F0)

PCI Device: 0
Address Offset: 02h
Default Value: 2580h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 2580h	**Device Identification Number (DID):** This field is an identifier assigned to the MCH core/primary PCI device.

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4.1.3 PCICMD—PCI Command (D0:F0)

PCI Device: 0
Address Offset: 04h
Default Value: 0006h
Access: RO, R/W
Size: 16 bits

Since MCH Device 0 does not physically reside on Primary PCI bus, many of the bits are not implemented.

Bit	Access & Default	Description
15:10		Reserved
9	RO 0b	**Fast Back-to-Back Enable (FB2B).** This bit controls whether or not the master can do fast back-to-back write. Since device 0 is strictly a target this bit is not implemented and is hardwired to 0.
8	R/W 0b	**SERR Enable (SERRE).** This bit is a global enable bit for Device 0 SERR messaging. The MCH does not have a SERR signal. The MCH communicates the SERR condition by sending an SERR message over DMI to the ICH6. 1 = Enable. The MCH is enabled to generate SERR messages over DMI for specific Device 0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTS, and PCISTS registers. If SERRE is clear, then the SERR message is not generated by the MCH for Device 0. 0 = Disable **Note:** That this bit only controls SERR messaging for the Device 0. Device 1 has its own SERRE bits to control error reporting for error conditions occurring in that device. The control bits are used in a logical OR manner to enable the SERR DMI message mechanism.
7	RO 0b	**Address/Data Stepping Enable (ADSTEP).** Hardwired to 0.
6	RO 0b	**Parity Error Enable (PERRE).** PERR# is not implemented by the MCH and this bit is hardwired to 0.
5	RO 0b	**VGA Palette Snoop Enable (VGASNOOP).** Hardwired to a 0.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE).** The MCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0.
3	RO 0b	Reserved
2	RO 1b	**Bus Master Enable (BME).** The MCH is always enabled as a master. This bit is hardwired to a 1.
1	RO 1b	**Memory Access Enable (MAE).** The MCH always allows access to main memory. This bit is not implemented and is hardwired to 1.
0	RO 0b	**I/O Access Enable (IOAE).** Hardwired to a 0.

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4.1.4 PCISTS—PCI Status (D0:F0)

PCI Device: 0
Address Offset: 06h
Default Value: 0090h
Access: RO, R/W/C
Size: 16 bits

This status register reports the occurrence of error events on Device 0's PCI interface. Since the MCH Device 0 does not physically reside on Primary PCI, many of the bits are not implemented.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Hhardwired to a 0.
14	R/W/C 0b	**Signaled System Error (SSE):** Software clears this bit by writing a 1 to it. 1 = The MCH Device 0 generated an SERR message over DMI for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD, and ERRCMD registers. Device 0 error flags are read/reset from the PCISTS, or ERRSTS registers.
13	R/WC 0b	**Received Master Abort Status (RMAS):** Software clears this bit by writing a 1 to it. 1 = MCH generated a DMI request that receives an Unsupported Request completion packet.
12	R/WC 0b	**Received Target Abort Status (RTAS):** Software clears this bit by writing a 1 to it. 1 = MCH generated a DMI request that receives a Completer Abort completion packet.
11	RO 0b	**Signaled Target Abort Status (STAS):** The MCH will not generate a Target Abort DMI completion packet or Special Cycle. This bit is not implemented in the MCH and is hardwired to a 0.
10:9	RO 00b	**DEVSEL Timing (DEVT):** These bits are hardwired to "00". Device 0 does not physically connect to Primary PCI. These bits are set to "00" (fast decode) so that optimum DEVSEL timing for Primary PCI is not limited by the MCH.
8	RO 0b	**Master Data Parity Error Detected (DPD):** PERR signaling and messaging are not implemented by the MCH; therefore, this bit is hardwired to 0.
7	RO 1b	**Fast Back-to-Back (FB2B):** Hardwired to 1. Device 0 does not physically connect to Primary PCI. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for Primary PCI is not limited by the MCH.
6		Reserved
5	RO 0b	**66 MHz Capable:** Does not apply to PCI Express*. Hardwired to 0.
4	RO 1b	**Capability List (CLIST):** This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the Capability standard register resides.
3:0		Reserved

4.1.5 RID—Revision Identification (D0:F0)

PCI Device:	0
Address Offset:	08h
Default Value:	00h
Access:	RO
Size:	8 bits

This register contains the revision number of the MCH Device 0.

Bit	Access & Default	Description
7:0	RO 00h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the MCH Device 0. 05h = B-2 Stepping

4.1.6 CC—Class Code (D0:F0)

PCI Device:	0
Address Offset:	09h
Default Value:	060000h
Access:	RO
Size:	24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access & Default	Description
23:16	RO 06h	**Base Class Code (BCC):** This is an 8-bit value that indicates the base class code for the MCH. 06h = Bridge device.
15:8	RO 00h	**Sub-Class Code (SUBCC):** This is an 8-bit value that indicates the category of Bridge into which the MCH falls. 00h = Host Bridge.
7:0	RO 00h	**Programming Interface (PI):** This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

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4.1.7   MLT—Master Latency Timer (D0:F0)

PCI Device: 0
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

Device 0 in the MCH is not a PCI master. Therefore this register is not implemented.

Bit	Access & Default	Description
7:0		Reserved

4.1.8   HDR—Header Type (D0:F0)

PCI Device: 0
Address Offset: 0Eh
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access & Default	Description
7:0	RO 00h	**PCI Header (HDR):** This field always returns 0 to indicate that the MCH is a single function device with standard header layout.

4.1.9   SVID—Subsystem Vendor Identification (D0:F0)

PCI Device: 0
Address Offset: 2Ch
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem Vendor ID (SUBVID):** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.

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4.1.10 SID—Subsystem Identification (D0:F0)

PCI Device: 0
Address Offset: 2Eh
Default Value: 0000h
Access: R/W/O
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Access & Default	Description
15:0	R/WO 0000h	**Subsystem ID (SUBID)**: This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

4.1.11 CAPPTR—Capabilities Pointer (D0:F0)

PCI Device: 0
Address Offset: 34h
Default Value: E0h
Access: RO
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Access & Default	Description
7:0	RO E0h	**Pointer to the offset of the first capability ID register block:** In this case the first capability is the product-specific Capability Identifier (CAPID0).

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4.1.12 EPBAR—Egress Port Base Address (D0:F0)

PCI Device: 0
Address Offset: 40h
Default Value: 00000000h
Access: RO
Size: 32 bits

This is the base address for the Egress Port MMIO configuration space. There is no physical memory within this 4-KB window that can be addressed. The 4 KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to EPBAREN[Dev 0, offset 54h, bit 27]

Bit	Access & Default	Description
31:12	R/W 00000h	**Egress Port MMIO Base Address:** This field corresponds to bits 31 to 12 of the base address Egress Port MMIO configuration space. BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB. System software uses this base address to program the MCH MMIO register set.
11:0		Reserved

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4.1.13   MCHBAR—MCH Memory Mapped Register Range Base Address (D0:F0)

PCI Device: 0
Address Offset: 44h
Default Value: 00000000h
Access: R/W
Size: 32 bits

This is the base address for the MCH memory-mapped configuration space. There is no physical memory within this 16-KB window that can be addressed. The 16 KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to MCHBAREN [Dev 0, offset 54h, bit 28]

Bit	Access & Default	Description
31:14	R/W 00000h	**MCH Memory Mapped Base Address:** This field corresponds to bits 31 to 14 of the base address MCH memory-mapped configuration space. BIOS will program this register resulting in a base address for a 16-KB block of contiguous memory address space. This register ensures that a naturally aligned 16-KB space is allocated within total addressable memory space of 4 GB. System software uses this base address to program the MCH Memory-mapped register set.
13:0		Reserved

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4.1.14 PCIEXBAR—PCI Express* Register Range Base Address (D0:F0)

PCI Device: 0
Address Offset: 48h
Default Value: E0000000h
Access: R/W
Size: 32 bits

This is the base address for the PCI Express configuration space. This window of addresses contains the 4 KB of configuration space for each PCI Express device that can potentially be part of the PCI Express hierarchy associated with the MCH. There is not actual physical memory within this 256-MB window that can be addressed. Each PCI Express hierarchies require a PCI Express BASE register. The MCH supports one PCI Express hierarchy.

The 256 MB reserved by this register does not alias to any PCI 2.3 compliant memory-mapped space. For example, MCHBAR reserves a 16-KB space and reserves a 4-KB space both outside of PCIEXBAR space. They cannot be overlaid on the space reserved by PCIEXBAR for devices 0.

On reset, this register is disabled and must be enabled by writing a 1 to PCIEXBAREN [Dev 0, offset 54h, bit 31]

If the PCI Express Base Address [bits 31:28] were set to Fh, an overlap with the High BIOS area, APIC ranges would result. Software must guarantee that these ranges do not overlap. The PCI Express Base Address cannot be less than the maximum address written to the Top of physical memory register (TOLUD). If a system is populated with more than 3.5 GB, either the PCI Express Enhanced Access mechanism must be disabled or the value in TOLUD must be reduced to report that only 3.5 GB are present in the system to allow a value of Eh for the PCI Express Base Address (assuming that all PCI 2.3 compatible configuration space fits above 3.75 GB).

Bit	Access & Default	Description
31:28	R/W Eh	**PCI Express* Base Address:** This field corresponds to bits 31 to 28 of the base address for PCI Express enhanced configuration space. BIOS will program this register resulting in a base address for a 256-MB block of contiguous memory address space. Having control of those particular 4 bits insures that this base address will be on a 256-MB boundary, above the lowest 256 MB and still within total addressable memory space, currently 4 GB. The address used to access the PCI Express configuration space for a specific device can be determined as follows: PCI Express Base Address + Bus Number * 1 MB + Device Number * 32 KB + Function Number * 4 KB The address used to access the PCI Express configuration space for **Device 1** in this component would be PCI Express Base Address + 0 * 1 MB + 1 * 32 KB + 0 * 4 KB = **PCI Express Base Address + 32 KB**. Remember that this address is the beginning of the 4-KB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space.
27:0		Reserved

4.1.15   DMIBAR—Root Complex Register Range Base Address (D0:F0)

PCI Device: 0
Address Offset: 4Ch
Default Value: 00000000h
Access: R/W
Size: 32 bits

This is the base address for the Root Complex configuration space. This window of addresses contains the Root Complex Register set for the PCI Express hierarchy associated with the MCH. There is no physical memory within this 4-KB window that can be addressed. The 4 KB that is reserved by this register does not alias to any PCI 2.3 compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to the DMIBAREN [Dev 0, offset 54h, bit 29].

Bit	Access & Default	Description
31:12	R/W 0000 0h	**DMI Base Address:** This field corresponds to bits 31 to 12 of the base address DMI configuration space. BIOS will program this register resulting in a base address for a 4-KB block of contiguous memory address space. This register ensures that a naturally aligned 4-KB space is allocated within total addressable memory space of 4 GB. System software uses this base address to program the DMI register set.
11:0		Reserved

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4.1.16 DEVEN—Device Enable (D0:F0)

PCI Device: 0
Address Offset: 54h
Default Value: 00000019h
Access: R/W
Size: 32 bits

This register allows for enabling/disabling of PCI devices and functions that are within the MCH.

Bit	Access & Default	Description
31	R/W 0b	**PCIEXBAR Enable (PCIEXBAREN):** 0 = The PCIEXBAR register is disabled. Memory read and write transactions proceed as if there were no PCIEXBAR register. PCIEXBAR bits 31:28 are R/W with no functionality behind them. 1 = The PCIEXBAR register is enabled. Memory read and write transactions whose address bits 31:28 match PCIEXBAR 31:28 will be translated to configuration reads and writes within the MCH. These translated cycles are routed as shown in the table above.
30		Reserved
29	R/W 0b	**DMIBAR Enable (DMIBAREN):** 0 = DMIBAR is disabled and does not claim any memory. 1 = DMIBAR memory mapped accesses are claimed and decoded appropriately.
28	R/W 0b	**MCHBAR Enable (MCHBAREN):** 0 = MCHBAR is disabled and does not claim any memory. 1 = MCHBAR memory mapped accesses are claimed and decoded appropriately.
27	R/W 0b	**EPBAR Enable (EPBAREN):** 0 = EPBAR is disabled and does not claim any memory. 1 = EPBAR memory mapped accesses are claimed and decoded appropriately.
26:2		Reserved
1	R/W 1b Strap dependent	**PCI Express* Port (D1EN):** 0 = Bus 0 Device 1 Function 0 is disabled and hidden. This also gates PCI Express internal clock (lgclk) and asserts PCI Express internal reset (lgrstb). 1 = Bus 0 Device 1 Function 0 is enabled and visible.
0	RO 1b	**Host Bridge:** Bus 0 Device 0 Function 0 can not be disabled and is therefore hardwired to 1.

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4.1.17 DEAP—DRAM Error Address Pointer (D0:F0)

PCI Device: 0
Address Offset: 58h
Default Value: 00000000h
Access: RO/S
Size: 32 bits

This register contains the address of detected DRAM ECC error(s).

Bit	Access & Default	Description
31:7	RO/S 0000000h	**Error Address Pointer (EAP):** This field is used to store the 128B (Two Cache Line) address of main memory for which an error (single bit or multi-bit error) has occurred. Note that the value of this bit field represents the address of the first single or the first multiple bit error occurrence after the error flag bits in the ERRSTS register have been cleared by software. A multiple bit error will overwrite a single bit error. Once the error flag bits are set as a result of an error, this bit field is locked and does not change as a result of a new error. These bits are reset on PWROK.
6:1		**Reserved**
0	RO/S 0b	**Channel Indicator:** This bit indicates which memory channel had the error. 0 = Channel A 1 = Channel B

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4.1.18   DERRSYN—DRAM Error Syndrome (D0:F0)

PCI Device: 0
Address Offset: 5Ch
Default Value: 00h
Access: RO/S
Size: 8 bits

This register is used to report the ECC syndromes for each quad word of a 32B-aligned data quantity read from the DRAM array.

Bit	Access & Default	Description
7:0	RO/S 00h	**DRAM ECC Syndrome (DECCSYN):** After a DRAM ECC error on any QW of the data chunk resulting from a read command, hardware loads this field with a syndrome that describes the set of bits associated with the first QW containing an error. Note that this field is locked from the time that it is loaded up to the time when the error flag is cleared by software. If the first error was a single bit, correctable error, then a subsequent multiple bit error on any of the QWs in this read transaction or any subsequent read transaction will cause the field to be rerecorded. When a multiple bit error is recorded, the field is locked until the error flag is cleared by software. In all other cases, an error that occurs after the first error, and before the error flag, has been cleared by software, will escape recording. These bits are reset on PWROK.

4.1.19   DERRDST—DRAM Error Destination (D0:F0)

PCI Device: 0
Address Offset: 5Dh
Default Value: 00h
Access: RO/S
Size: 8 bits

This register is used to report the destination of the data containing an ECC error whose address is recorded in DEAP register.

Bit	Access & Default	Description
7:6		Reserved
5:0	RO/S 00h	**Error Source Code:** This field is updated concurrently with DERRSYN. 00h = Processor to memory reads 01h–07h = Reserved 08h–09h = DMI VC0 initiated and targeting cycles/data 0Ah–0Bh = DMI VC1 initiated and targeting cycles/data 0Ch–0Dh = DMI VCp initiated and targeting cycles/data 0Eh–0Fh = Reserved 10h = PCI Express* initiated and targeting cycles/data 11h = Reserved 12h = PCI Express* initiated and targeting cycles/data 13h = Reserved 14h–16h = PCI Express* initiated and targeting cycles/data 17h = Reserved 18h–1Ah: = Reserved 1Bh–3Eh = Reserved 3Fh = Used for broadcast messages with data targeting multiple units. (e.g., EOI). These bits are reset on PWROK.

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4.1.20   PAM0—Programmable Attribute Map 0 (D0:F0)

PCI Device: 0
Address Offset: 90h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS area from 0F0000h–0FFFFFh

The MCH allows programmable memory attributes on 13 Legacy memory segments of various sizes in the 768-KB to 1-MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cache ability of these areas is controlled via the MTRR registers in the P6 processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

- RE (Read Enable). When RE = 1, the processor read accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to Primary PCI.

- WE (Write Enable). When WE = 1, the host write accesses to the corresponding memory segment are claimed by the MCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to Primary PCI.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM Register controls two regions, typically 16 KB in size.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0F0000-0FFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that addresses the BIOS area from 0F0000h to 0FFFFFh. 00 = DRAM Disabled: All accesses are directed to the DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:0		Reserved

Warning: The MCH may hang if a PCI Express graphics attach or DMI originated access to Read Disabled or Write Disabled PAM segments occurs (due to a possible IWB to non-DRAM). For these reasons the following critical restriction is placed on the programming of the PAM regions:

At the time that a DMI or PCI Express graphics attach accesses to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writeable.

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4.1.21 PAM1—Programmable Attribute Map 1 (D0:F0)

PCI Device:	0
Address Offset:	91h
Default Value:	00h
Access:	R/W
Size:	8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C0000h–0C7FFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0C4000-0C7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C4000h to 0C7FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0C0000-0C3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C0000h to 0C3FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

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4.1.22   PAM2—Programmable Attribute Map 2 (D0:F0)

PCI Device: 0
Address Offset: 92h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C8000h–
0CFFFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0CC000h–0CFFFFh Attribute (HIENABLE):** 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0C8000h–0CBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C8000h to 0CBFFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.23 PAM3—Programmable Attribute Map 3 (D0:F0)

PCI Device:	0
Address Offset:	93h
Default Value:	00h
Access:	R/W
Size:	8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D0000h–0D7FFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0D4000h–0D7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D4000h to 0D7FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0D0000h–0D3FFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D0000h to 0D3FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

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4.1.24   PAM4—Programmable Attribute Map 4 (D0:F0)

PCI Device: 0
Address Offset: 94h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D8000h-0DFFFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0DC000h–0DFFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0DC000h to 0DFFFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0D8000h–0DBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D8000h to 0DBFFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.25 PAM5—Programmable Attribute Map 5 (D0:F0)

PCI Device:	0
Address Offset:	95h
Default Value:	00h
Access:	R/W
Size:	8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E0000h-0E7FFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0E4000h–0E7FFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0E0000h–0E3FFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

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4.1.26   PAM6—Programmable Attribute Map 6 (D0:F0)

PCI Device: 0
Address Offset: 96h
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E8000h–0EFFFFh.

Bit	Access & Default	Description
7:6		Reserved
5:4	R/W 00b	**0EC000h–0EFFFFh Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		Reserved
1:0	R/W 00b	**0E8000h–0EBFFFh Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. 00 = DRAM Disabled: Accesses are directed to the DMI. 01 = Read Only: All reads are serviced by DRAM. All writes are forwarded to the DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.27　LAC—Legacy Access Control (D0:F0)

PCI Device:　　　　　　　　　　　0
Address Offset:　　　　　　　　　97h
Default Value:　　　　　　　　　　00h
Access:　　　　　　　　　　　　　R/W
Size:　　　　　　　　　　　　　　8 bits

This 8-bit register controls a fixed DRAM hole from 15–16 MB.

Bit	Access & Default	Description
7	R/W 0b	**Hole Enable (HEN):** This field enables a memory hole in DRAM space. The DRAM that lies "behind" this space is not remapped. 0 = No memory hole. 1 = Memory hole from 15 MB to 16 MB.
6:1		Reserved
0	R/W 0b	**MDA Present (MDAP):** This bit works with the VGA Enable bits in the BCTRL register of Device 1 to control the routing of processor initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1's VGA Enable bit is not set. If device 1's VGA enable bit is not set, then accesses to I/O address range x3BCh–x3BFh are forwarded to the DMI. If the VGA enable bit is set and MDA is not present, then accesses to I/O address range x3BCh–x3BFh are forwarded to PCI Express* if the address is within the corresponding IOBASE and IOLIMIT, otherwise they are forwarded to the DMI. MDA resources are defined as the following: Memory:　　0B0000h – 0B7FFFh I/O:　　　　3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, 　　　　　　(Including ISA address aliases, A [15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to the DMI even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA: <table><tr><th>VGAEN</th><th>MDAP</th><th>Description</th></tr><tr><td>0</td><td>0</td><td>All References to MDA and VGA space are routed to the DMI</td></tr><tr><td>0</td><td>1</td><td>Illegal combination</td></tr><tr><td>1</td><td>0</td><td>All VGA and MDA references are routed to PCI Express Graphics Attach.</td></tr><tr><td>1</td><td>1</td><td>All VGA references are routed to PCI Express Graphics Attach. MDA references are routed to the DMI</td></tr></table>

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4.1.28   TOLUD—Top of Low Usable DRAM (D0:F0)

PCI Device: 0
Address Offset: 9Ch
Default Value: 08h
Access: R/W
Size: 8 bits

This 8-bit register defines the Top of Low Usable DRAM. TSEG and Graphics Stolen Memory are within the DRAM space defined.

Bit	Access & Default	Description
7:3	R/W 01h	**Top of Low Usable DRAM (TOLUD):** This register contains bits 31 to 27 of an address one byte above the maximum DRAM memory that is usable by the operating system. Address bits 31 down to 27 programmed to 01h implies a minimum memory size of 128 MBs. Configuration software must set this value to the smaller of the following 2 choices: • Maximum amount memory in the system plus one byte or the minimum address allocated for PCI memory. Address bits 26:0 are assumed to be 000_0000h for the purposes of address comparison. The host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register. If this register is set to 0000 0b, it implies 128 MBs of system memory.
2:0		Reserved

4.1.29 SMRAM—System Management RAM Control (D0:F0)

PCI Device: 0
Address Offset: 9Dh
Default Value: 00h
Access: R/W/L, RO
Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G_SMRAME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

Bit	Access & Default	Description
7		Reserved
6	R/W/L 0b	**SMM Space Open (D_OPEN):** When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
5	R/W/L 0b	**SMM Space Closed (D_CLS):** When D_CLS = 1 SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference through SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. Note that the D_CLS bit only applies to Compatible SMM space.
4	R/W/L 0b	**SMM Space Locked (D_LCK):** When D_LCK is set to 1, D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMRAM_EN, TSEG_SZ and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	R/W/L 0b	**Global SMRAM Enable (G_SMRAME):** If set to a 1, Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADSB with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details. Once D_LCK is set, this bit becomes read only.
2:0	RO 010b	**Compatible SMM Space Base Segment (C_BASE_SEG):** This field indicates the location of SMM space. SMM DRAM is not remapped. It is simply made visible if the conditions are right to access SMM space, otherwise the access is forwarded to DMI. Since the MCH supports only the SMM space between A0000h and BFFFFh, this field is hardwired to 010.

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4.1.30 ESMRAMC—Extended System Management RAM Control (D0:F0)

PCI Device: 0
Address Offset: 9Eh
Default Value: 00h
Access: R/W/L, RO
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

Bit	Access & Default	Description
7	R/W/L 0b	**Enable High SMRAM (H_SMRAME):** This bit controls the SMM memory space location (i.e., above 1 MB or below 1 MB) When G_SMRAME is 1 and H_SMRAME is 1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA0000h to 0FEDBFFFFh are remapped to DRAM addresses within the range 000A0000h to 000BFFFFh. Once D_LCK has been set, this bit becomes read only.
6	R/W/C 0b	**Invalid SMRAM Access (E_SMERR):** This bit is set when the processor has accessed the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	RO 1b	**SMRAM Cacheable (SM_CACHE):** This bit is forced to 1 by the MCH .
4	RO 1b	**L1 Cache Enable for SMRAM (SM_L1):** This bit is forced to 1 by the MCH.
3	RO 1b	**L2 Cache Enable for SMRAM (SM_L2):** This bit is forced to 1 by the MCH.
2:1		Reserved
0	R/W/L 0b	**TSEG Enable (T_EN):** This bit Enables SMRAM memory for Extended SMRAM space only. When G_SMRAME =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Note that once D_LCK is set, this bit becomes read only.

4.1.31 ERRSTS—Error Status (D0:F0)

PCI Device: 0
Address Offset: C8h
Default Value: 0000h
Access: R/WC/S, RO
Size: 16 bits

This register is used to report various error conditions via the SERR DMI messaging mechanism. An SERR DMI message is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD and PCICMD registers). These bits are set regardless of whether or not the SERR is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a 1 to it.

0Bit	Access & Default	Description
15:13		Reserved
12	R/WC/S 0b	**MCH Software Generated Event for SMI:** 1 = This bit indicates the source of the SMI was a Device 2 Software Event.
11	R/WC/S 0b	**MCH Thermal Sensor Event for SMI/SCI/SERR:** This bit indicates that a MCH Thermal Sensor trip has occurred and an SMI, SCI, or SERR has been generated. The status bit is set only if a message is sent based on Thermal event enables in Error command, SMI command, and SCI command registers. A trip point can generate one of SMI, SCI, or SERR interrupts (two or more per event is illegal). Multiple trip points can generate the same interrupt, if software chooses this mode, subsequent trips may be lost. If this bit is already set, an interrupt message will not be sent on a new thermal sensor event.
10		Reserved
9	R/WC/S 0b	**LOCK to non-DRAM Memory Flag (LCKF):** 1 = MCH detected a lock operation to memory space that did not map into DRAM.
8	R/WC/S 0b	**Received Refresh Timeout Flag(RRTOF):** 1 = 1024 memory core refreshes are enqueued.
7	R/WC/S 0b	**DRAM Throttle Flag (DTF):** 1 = Indicates that a DRAM Throttling condition occurred. 0 = Software has cleared this flag since the most recent throttling event
6:2		Reserved
1	R/WC/S 0b	**Multiple-bit DRAM ECC Error Flag (DMERR):** If this bit is set to 1, a memory read data transfer had an uncorrectable multiple-bit error. When this bit is set, the address, channel number, and device number that caused the error are logged in the EAP register. Once this bit is set, the EAP, CN, DN, and ES fields are locked until the processor clears this bit by writing a 1. Software uses bits [1:0] to detect whether the logged error address is for Single or Multiple-bit error. This bit is reset on PWROK.
0	R/WC/S 0b	**Single-bit DRAM ECC Error Flag (DSERR):** If this bit is set to 1, a memory read data transfer had a single-bit correctable error and the corrected data was sent for the access. When this bit is set the address and device number that caused the error are logged in the EAP register. Once this bit is set the EAP, CN, DN, and ES fields are locked to further single bit error updates until the processor clears this bit by writing a 1. A multiple bit error that occurs after this bit is set will overwrite the EAP, CN, and DN fields with the multiple-bit error signature and the MEF bit will also be set. This bit is reset on PWROK.

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4.1.32   ERRCMD—Error Command (D0:F0)

PCI Device: 0
Address Offset: CAh
Default Value: 0000h
Access: R/W
Size: 16 bits

This register controls the MCH responses to various system errors. Since the MCH does not have an SERR# signal, SERR messages are passed from the MCH to the Intel ICH6 over DMI. When a bit in this register is set, a SERR message will be generated on DMI when the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device 0 via the PCI Command register.

Bit	Access & Default	Description
15:12		Reserved
11	R/W 0b	**SERR on MCH Thermal Sensor Event (TSESERR)** 1 = The MCH generates a DMI SERR special cycle when bit 11 of the ERRSTS is set. The SERR must not be enabled at the same time as the SMI for the same thermal sensor event. 0 = Reporting of this condition via SERR messaging is disabled.
10		Reserved
9	R/W 0b	**SERR on LOCK to non-DRAM Memory (LCKERR)** 1 = The MCH will generate a DMI SERR special cycle whenever a processor lock cycle is detected that does not hit DRAM. 0 = Reporting of this condition via SERR messaging is disabled.
8	R/W 0b	**SERR on DRAM Refresh Timeout (DRTOERR)** 1 = The MCH generates a DMI SERR special cycle when a DRAM Refresh timeout occurs. 0 = Reporting of this condition via SERR messaging is disabled.
7:2		Reserved
1	R/W 0b	**SERR Multiple-Bit DRAM ECC Error (DMERR)** 1 = The MCH generates a SERR message over DMI when it detects a multiple-bit error reported by the DRAM controller. 0 = Reporting of this condition via SERR messaging is disabled. For systems not supporting ECC, this bit must be disabled.
0	R/W 0b	**SERR on Single-bit ECC Error (DSERR)** 1 = The MCH generates a SERR special cycle over DMI when the DRAM controller detects a single bit error. 0 = Reporting of this condition via SERR messaging is disabled. For systems that do not support ECC, this bit must be disabled.

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4.1.33   SMICMD—SMI Command (D0:F0)

PCI Device: 0
Address Offset: CCh
Default Value: 0000h
Access: R/W
Size: 16 bits

This register enables various errors to generate an SMI DMI special cycle. When an error flag is set in the ERRSTS register, it can generate an SERR, SMI, or SCI DMI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively. Note that one and only one message type can be enabled.

Bit	Access & Default	Description
15:2		Reserved
1	R/W 0b	**SMI on Multiple-Bit DRAM ECC Error (DMESMI):** 1 = The MCH generates an SMI DMI message when it detects a multiple-bit error reported by the DRAM controller. 0 = Reporting of this condition via SMI messaging is disabled. For systems not supporting ECC, this bit must be disabled.
0	R/W 0b	**SMI on Single-bit ECC Error (DSESMI):** 1 = The MCH generates an SMI DMI special cycle when the DRAM controller detects a single bit error. 0 = Reporting of this condition via SMI messaging is disabled. For systems that do not support ECC, this bit must be disabled.

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4.1.34 SCICMD—SCI Command (D0:F0)

PCI Device: 0
Address Offset: CEh
Default Value: 0000h
Access: R/W
Size: 16 bits

This register enables various errors to generate an SMI DMI special cycle. When an error flag is set in the ERRSTS register, it can generate an SERR, SMI, or SCI DMI special cycle when enabled in the ERRCMD, SMICMD, or SCICMD registers, respectively. Note that one and only one message type can be enabled.

Bit	Access & Default	Description
15:2		Reserved
1	R/W 0b	**SCI on Multiple-Bit DRAM ECC Error (DMESCI):** 1 = The MCH generates an SCI DMI message when it detects a multiple-bit error reported by the DRAM controller. 0 = Reporting of this condition via SCI messaging is disabled. For systems not supporting ECC this bit must be disabled.
0	R/W 0b	**SCI on Single-bit ECC Error (DSESCI):** 1 = The MCH generates an SCI DMI special cycle when the DRAM controller detects a single bit error. 0 = Reporting of this condition via SCI messaging is disabled. For systems that do not support ECC this bit must be disabled.

4.1.35 SKPD—Scratchpad Data (D0:F0)

PCI Device: 0
Address Offset: DCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers.

Bit	Access & Default	Description
31:0	R/W 00000000 h	**Scratchpad Data:** 1 DWord of data storage.

4.1.36   CAPID0—Capability Identifier (D0:F0)

PCI Device: 0
Address Offset: E0h
Default Value: 000000000001090009h
Access: RO
Size: 72 bits

Bit	Access & Default	Description
71:28		Reserved
27:24	RO 1h	**CAPID Version:** This field has the value 0001b to identify the first revision of the CAPID register definition.
23:16	RO 09h	**CAPID Length:** This field has the value 09h to indicate the structure length (9 bytes).
15:8	RO 00h	**Next Capability Pointer:** This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO 09h	**CAP_ID:** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

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5 MCHBAR Registers

These registers are offset from the MCHBAR base address.

Address Offset	Register Symbol	Register Name	Default Value	Access
100h	C0DRB0	Channel A DRAM Rank Boundary Address 0	00h	R/W
101h	C0DRB1	Channel A DRAM Rank Boundary Address 1	00h	R/W
102h	C0DRB2	Channel A DRAM Rank Boundary Address 2	00h	R/W
103h	C0DRB3	Channel A DRAM Rank Boundary Address 3	00h	R/W
104–107h	—	Reserved	—	—
108h	C0DRA0	Channel A DRAM Rank 0,1 Attribute	00h	R/W
109h	C0DRA2	Channel A DRAM Rank 2,3 Attribute	00h	R/W
10A–10Bh	—	Reserved	—	—
10Ch	C0DCLKDIS	Channel A DRAM Clock Disable	00h	R/W
10Dh	—	Reserved	—	—
10E–10F	C0BNKARC	Channel A DRAM Bank Architecture	0000h	R/W
110–113h	—	Reserved	—	—
114–117h	C0DRT1	Channel A DRAM Timing Register	900122h	R/W
118–11Fh	—	Reserved	—	—
120–123h	C0DRC0	Channel A DRAM Controller Mode 0	00000000h	R/W, RO
124–17Fh	—	Reserved	—	—
180h	C1DRB0	Channel B DRAM Rank Boundary Address 0	00h	R/W
181h	C1DRB1	Channel B DRAM Rank Boundary Address 1	00h	R/W
182h	C1DRB2	Channel B DRAM Rank Boundary Address 2	00h	R/W
183h	C1DRB3	Channel B DRAM Rank Boundary Address 3	00h	R/W
184–187h	—	Reserved	—	—
188h	C1DRA0	Channel B DRAM Rank 0,1 Attribute	00h	R/W
189h	C1DRA2	Channel B DRAM Rank 2,3 Attribute	00h	R/W
18A–18Bh	—	Reserved	—	—
18Ch	C1DCLKDIS	Channel B DRAM Clock Disable	00h	R/W

Address Offset	Register Symbol	Register Name	Default Value	Access
18Dh	—	Reserved	—	—
18E–18Fh	C1BNKARC	Channel B Bank Architecture	0000h	R/W
190–193h	—	Reserved	—	—
194h	C1DRT1	Channel B DRAM Timing Register 1	900122h	R/W, RO
195–19Fh	—	Reserved	—	—
1A0–1A3h	C1DRC0	Channel B DRAM Controller Mode 0	00000000h	R/W, RO
1A4–F0Fh	—	Reserved	—	—
F10–F13h	PMCFG	Power Management Configuration	00000000h	R/W
F14h	PMSTS	Power Management Status	00000000h	R/W/C/S

5.1 MCHBAR Register Details

5.1.1 C0DRB0—Channel A DRAM Rank Boundary Address 0

MMIO Range: MCHBAR
Address Offset: 100h
Default Value: 00h
Access: R/W
Size: 8 bits

The **DRAM Rank Boundary Register** defines the upper boundary address of each DRAM rank with a granularity of 32 MB. Each rank has its own single-byte **DRB** register. These registers are used to determine which chip select will be active for a given address.

Channel and Rank Map:

Channel A Rank 0:   100h
Channel A Rank 1:   101h
Channel A Rank 2:   102h
Channel A Rank 3:   103h
Channel B Rank 0:   180h
Channel B Rank 1:   181h
Channel B Rank 2:   182h
Channel B Rank 3:   183h

Single Channel or Asymmetric Channels Example

If the channels are independent, addresses in Channel B should begin where addresses in Channel A left off, and the address of the first rank of Channel A can be calculated from the technology (256 Mbit, 512 Mbit, or 1 Gbit) and the x8 or x16 configuration. With independent channels, a value of 01h in **C0DRB0** indicates that 32 MB of DRAM has been populated in the first rank, and the top address in that rank is 32 MB.

Programming guide

If Channel A is empty, all of the C0DRBs are programmed with 00h.

C0DRB0 = Total memory in chA rank0 (in 32-MB increments)

C0DRB1 = Total memory in chA rank0 + chA rank1 (in 32-MB increments)

_____

C1DRB0 = Total memory in chA rank0 + chA rank1 + chA rank2 + chA rank3 + chB rank0
(in 32-MB increments)

If Channel B is empty, all of the C1DRBs are programmed with the same value as C0DRB3.

Interleaved Channels Example

If channels are interleaved, corresponding ranks in opposing channels will contain the same value, and the value programmed takes into account the fact that twice as many addresses are spanned by this rank compared to the single channel case. With interleaved channels, a value of 01h in **C0DRB0** and a value of 01h in **C1DRB0** indicate that 32 MB of DRAM has been populated in the first rank of each channel and the top address in that rank of either channel is 64 MB.

Programming guide:

C0DRB0 = C1DRB0 = Total memory in chA rank0 (in 32-MB increments)

C0DRB1 = C1DRB1 = Total memory in chA rank0 + chA rank1 (in 32-MB increments)

_____

C0DRB3 = C1DRB3 = Total memory in chA rank0 + chA rank1+ chA rank2 + chA rank3
(in 32-MB increments)

Note: Channel A DRB3 and Channel B DRB3 must be equal for this mode, but the other DRBs may be different.

In all modes, if a DIMM is single sided, it appears as a populated rank and an empty rank. A DRB must be programmed appropriately for each.

Each Rank is represented by a byte. Each byte has the following format.

Bit	Access & Default	Description
7:0	R/W 00h	**Channel A DRAM Rank Boundary Address:** This 8 bit value defines the upper and lower addresses for each DRAM rank. Bits 6:2 are compared against Address 31:27 to determine the upper address limit of a particular rank. Bits 1:0 must be 0s. Bit 7 may be programmed to a 1 in the highest DRB (DRB3) if 4 GBs of memory is present.

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5.1.2 C0DRB1—Channel A DRAM Rank Boundary Address 1

MMIO Range: MCHBAR
Address Offset: 101h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.3 C0DRB2—Channel A DRAM Rank Boundary Address 2

MMIO Range: MCHBAR
Address Offset: 102h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.4 C0DRB3—Channel A DRAM Rank Boundary Address 3

MMIO Range: MCHBAR
Address Offset: 103h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

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5.1.5   C0DRA0—Channel A DRAM Rank 0,1 Attribute

MMIO Range: MCHBAR
Address Offset: 108h
Default Value: 00h
Access: R/W
Size: 8 bits

The **DRAM Rank Attribute Registers** define the page sizes to be used when accessing different ranks. These registers should be left with their default value (all zeros) for any rank that is unpopulated, as determined by the corresponding CxDRB registers. Each byte of information in the **CxDRA** registers describes the page size of a pair of ranks.

Channel and Rank Map:

Channel A Rank 0, 1:   108h
Channel A Rank 2, 3:   109h
Channel B Rank 0, 1:   188h
Channel B Rank 2, 3:   189h

Bit	Access & Default	Description
7		Reserved
6:4	R/W 000b	**Channel A DRAM odd Rank Attribute:** This 3 bit field defines the page size of the corresponding rank. 000 = Unpopulated 001 = Reserved 010 = 4 KB 011 = 8 KB 100 = 16 KB Others = Reserved
3		Reserved
2:0	R/W 000b	**Channel A DRAM even Rank Attribute:** This 3 bit field defines the page size of the corresponding rank. 000 = Unpopulated 001 = Reserved 010 = 4 KB 011 = 8 KB 100 = 16 KB Others = Reserved

5.1.6   C0DRA2—Channel A DRAM Rank 2,3 Attribute

MMIO Range: MCHBAR
Address Offset: 109h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRA0.

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5.1.7 C0DCLKDIS—Channel A DRAM Clock Disable

MMIO Range: MCHBAR
Address Offset: 10Ch
Default Value: 00h
Access: R/W
Size: 8 bits

This register can be used to disable the system memory clock signals to each DIMM slot. This can significantly reduce EMI and Power concerns for clocks that go to unpopulated DIMMs. Clocks should be enabled based on whether a slot is populated, and what kind of DIMM is present.

Bit	Access & Default	Description
7:6		Reserved
5	R/W 0b	**DIMM Clock Gate Enable Pair 5** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
4	R/W 0b	**DIMM Clock Gate Enable Pair 4** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
3	R/W 0b	**DIMM Clock Gate Enable Pair 3** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
2	R/W 0b	**DIMM Clock Gate Enable Pair 2** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
1	R/W 0b	**DIMM Clock Gate Enable Pair 1** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.
0	R/W 0b	**DIMM Clock Gate Enable Pair 0** 0 = Tri-state the corresponding clock pair. 1 = Enable the corresponding clock pair.

Note: Since there are multiple clock signals assigned to each Rank of a DIMM, it is important to clarify exactly which Rank width field affects which clock signal:

Channel	Rank	Clocks Affected
0	0 or 1	SCLK_A[2:0]/ SCLK_A[2:0]#
0	2 or 3	SCLK_A[5:3]/ SCLK_A[5:3]#
1	0 or 1	SCLK_B[2:0]/ SCLK_B[2:0]#
1	2 or 3	SCLK_B[5:3]/ SCLK_B[5:3]#

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5.1.8 C0BNKARC—Channel A DRAM Bank Architecture

MMIO Range: MCHBAR
Address Offset: 10Eh
Default Value: 0000h
Access: R/W
Size: 16 bits

This register is used to program the bank architecture for each Rank.

Bit	Access & Default	Description
15:8		Reserved
7:6	R/W 00b	Rank 3 Bank Architecture 00 = 4 Bank. 01 = 8 Bank. 1X = Reserved
5:4	R/W 00b	Rank 2 Bank Architecture 00 = 4 Bank. 01 = 8 Bank. 1X = Reserved
3:2	R/W 00b	Rank 1 Bank Architecture 00 = 4 Bank. 01 = 8 Bank. 1X = Reserved
1:0	R/W 00b	Rank 0 Bank Architecture 00 = 4 Bank. 01 = 8 Bank. 1X = Reserved

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5.1.9 C0DRT1—Channel A DRAM Timing Register

MMIO Range: MCHBAR
Address Offset: 114h
Default Value: 900122hh
Access: R/W, RO
Size: 32 bits

Bit	Access & Default	Description
31:24		Reserved
23:20	R/W 9h	**Activate to Precharge delay (t_{RAS}).** This bit controls the number of DRAM clocks for t_{RAS}. Minimum recommendations are beside their corresponding encodings. 0h – 3h = Reserved 4h – Fh = Four to Fifteen Clocks respectively.
19	RO 0b	**Reserved for Activate to Precharge Delay (t_{RAS}) MAX:** It is required that the Panic Refresh timer be set to a value less than the t_{RAS} maximum. Based on this setting, a Panic Refresh occurs before T_{RAS} maximum expiration and closes all the banks. This bit controls the maximum number of clocks that a DRAM bank can remain open. After this time period, the DRAM controller will guarantee to pre-charge the bank. This time period may or may not be set to overlap with time period that requires a refresh to happen. The DRAM controller includes a separate $t_{RAS-MAX}$ counter for every supported bank. With a maximum of four ranks, and four banks per rank, there are 16 counters per channel. 0 = 120 microseconds 1 = Reserved **Note:** This register will become Read Only with a value of 0 if the design does not implement these counters. $t_{RAS-MAX}$ is not required because a panic refresh will close all banks in a rank before $t_{RAS-MAX}$ expires.
18:10		Reserved
9:8	R/W 01b	**CASB Latency (tCL).** This value is programmable on DDR2 DIMMs. The value programmed here must match the CAS Latency of every DDR2 DIMM in the system. **Encoding DDR2 CL** 00 5 01 4 10 3 11 Reserved
7		Reserved

Bit	Access & Default	Description
6:4	R/W 010b	**DRAM RAS to CAS Delay (t_{RCD}).** This bit controls the number of clocks inserted between a row activate command and a read or write command to that row. 000 = 2 DRAM clocks 001 = Reserved 010 = 4 DRAM clocks 011 = 5 DRAM clocks 100 – 111 = Reserved
3		Reserved
2:0	R/W 010b	**DRAM RAS Precharge (t_{RP}).** This bit controls the number of clocks that are inserted between a row precharge command and an activate command to the same rank. 000 = 2 DRAM clocks 001 = Reserved 010 = 4 DRAM clocks 011 = 5 DRAM clocks 100 – 111 = Reserved

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5.1.10   C0DRC0—Channel A DRAM Controller Mode 0

MMIO Range: MCHBAR
Address Offset: 120h
Default Value: 00000000h
Access: R/W
Size: 32 bits

Bit	Access & Default	Description
31:30		Reserved
29	R/W 0b	**Initialization Complete (IC):** This bit is used for communication of software state between the memory controller and the BIOS. BIOS sets this bit to 1 after initialization of the DRAM memory array is complete.
28:11		Reserved
10:8	R/W 000b	**Refresh Mode Select (RMS):** This field determines whether refresh is enabled and, if so, at what rate refreshes will be executed. 000 = Refresh disabled 001 = Refresh enabled. Refresh interval 15.6 usec 010 = Refresh enabled. Refresh interval 7.8 usec 011 = Refresh enabled. Refresh interval 3.9 usec 100 = Refresh enabled. Refresh interval 1.95 usec 111 = Refresh enabled. Refresh interval 64 clocks (fast refresh mode) Other = Reserved
7	RO 0b	Reserved

Bit	Access & Default	Description
6:4	R/W 000 b	**Mode Select (SMS).** These bits select the special operational mode of the DRAM interface. The special modes are intended for initialization at power up. 000 = Post Reset state – When the MCH exits reset (power-up or otherwise), the mode select field is cleared to "000". During any reset sequence, while power is applied and reset is active, the MCH de-asserts all CKE signals. After internal reset is de-asserted, CKE signals remain de-asserted until this field is written to a value different than "000". On this event, all CKE signals are asserted. During suspend, MCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. As part of resume sequence, MCH will be reset – which will clear this bit field to "000" and maintain CKE signals de-asserted. After internal reset is de-asserted, CKE signals remain de-asserted until this field is written to a value different than "000". On this event, all CKE signals are asserted. During entry to other low power states (C3, S1), MCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. During exit to normal mode, MCH signal triggers DRAM controller to exit Self-Refresh and resume normal operation without S/W involvement. 001 = NOP Command Enable – All processor cycles to DRAM result in a NOP command on the DRAM interface. 010 = All Banks Pre-charge Enable – All processor cycles to DRAM result in an "all banks precharge" command on the DRAM interface. 011 = Mode Register Set Enable – All processor cycles to DRAM result in a "mode register" set command on the DRAM interface. Host address lines are mapped to DRAM address lines in order to specify the command sent. Host address lines [12:3] are mapped to MA[9:0], and HA[13] is mapped to MA[11]. 101 = Reserved 110 = CBR Refresh Enable – In this mode all processor cycles to DRAM result in a CBR cycle on the DRAM interface 111 = Normal operation
3:2		Reserved
1:0	RO	**DRAM Type (DT).** This field is used to select between supported SDRAM types. This bit is controlled by the MTYPE strap signal. 00 = Reserved 01 = Reserved 10 = Second Revision Dual Data Rate (DDR2) SDRAM 11 = Reserved

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5.1.11 C1DRB0—Channel B DRAM Rank Boundary Address 0

MMIO Range: MCHBAR
Address Offset: 180h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.12 C1DRB1—Channel B DRAM Rank Boundary Address 1

MMIO Range: MCHBAR
Address Offset: 181h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.13 C1DRB2—Channel B DRAM Rank Boundary Address 2

MMIO Range: MCHBAR
Address Offset: 182h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.14 C1DRB3—Channel B DRAM Rank Boundary Address 3

MMIO Range: MCHBAR
Address Offset: 183h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.1.15 C1DRA0—Channel B DRAM Rank 0,1 Attribute

MMIO Range: MCHBAR
Address Offset: 188h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRA0.

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5.1.16 C1DRA2—Channel B DRAM Rank 2,3 Attribute

MMIO Range: MCHBAR
Address Offset: 189h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRA0.

5.1.17 C1DCLKDIS—Channel B DRAM Clock Disable

MMIO Range: MCHBAR
Address Offset: 18Ch
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DCLKDIS.

5.1.18 C1BNKARC—Channel B Bank Architecture

MMIO Range: MCHBAR
Address Offset: 18Eh
Default Value: 0000h
Access: R/W
Size: 16 bits

The operation of this register is detailed in the description for register C0BNKARC.

5.1.19 C1DRT1—Channel B DRAM Timing Register 1

MMIO Range: MCHBAR
Address Offset: 194h
Default Value: 900122h
Access: R/W
Size: 32 bits

The operation of this register is detailed in the description for register C0DRT1.

5.1.20 C1DRC0—Channel B DRAM Controller Mode 0

MMIO Range: MCHBAR
Address Offset: 1A0h
Default Value: 00000000h
Access: R/W
Size: 32 bits

The operation of this register is detailed in the description for register C0DRC0.

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5.1.21   PMCFG—Power Management Configuration

MMIO Range: MCHBAR
Address Offset: F10h
Default Value: 00000000h
Access: R/W
Size: 32 bits

Bit	Access & Default	Description
31:5		Reserved
4	R/W 0b	**Enhanced Power Management Features Enable** 0 = Legacy power management mode 1 = Reserved.
3:0		Reserved

5.1.22   PMSTS—Power Management Status

MMIO Range: MCHBAR
Address Offset: F14h
Default Value: 00000000h
Access: R/W
Size: 32 bits

This register is Reset by PWROK only.

Bit	Access & Default	Description
31:2		Reserved
1	R/WC/S 0b	**Channel B in self-refresh.** This bit is set by power management hardware after Channel B is placed in self refresh as a result of a Power State or a Reset Warn sequence. It is cleared by power management hardware before starting Channel B self refresh exit sequence initiated by a power management exit. It is cleared by BIOS in a warm reset (Reset# asserted while pwrok is asserted) exit sequence. 0 = Channel B not guaranteed to be in self-refresh. 1 = Channel B in Self-Refresh.
0	R/WC/S 0b	**Channel A in Self-refresh.** Set by power management hardware after Channel A is placed in self refresh as a result of a Power State or a Reset Warn sequence. It is cleared by power management hardware before starting Channel A self refresh exit sequence initiated by a power management exit. It is cleared by the BIOS in a warm reset (Reset# asserted while PWOK is asserted) exit sequence. 0 = Channel A not guaranteed to be in self-refresh. 1 = Channel A in Self-Refresh.

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6 EPBAR Registers—Egress Port Register Summary

These registers are offset from the EPBAR base address.

Table 6-1. Egress Port Register Address Map

Address Offset	Register Symbol	Register Name	Default Value	Access
044h–047h	EPESD	EP Element Self Description	0000h	R/WO, RO
050h–053h	EPLE1D	EP Link Entry 1 Description	0100h	R/WO, RO
058h–05Fh	EPLE1A	EP Link Entry 1 Address	0000000000000000h	R/WO, RO
060h–063h	EPLE2D	EP Link Entry 2 Description	02000002h	R/WO, RO
068h–06Fh	EPLE2A	EP Link Entry 2 Address	0000000000008000h	RO

6.1 EP RCRB Configuration Register Details

Figure 6-1. Link Declaration Topology

Intel® 82925X MCH Datasheet

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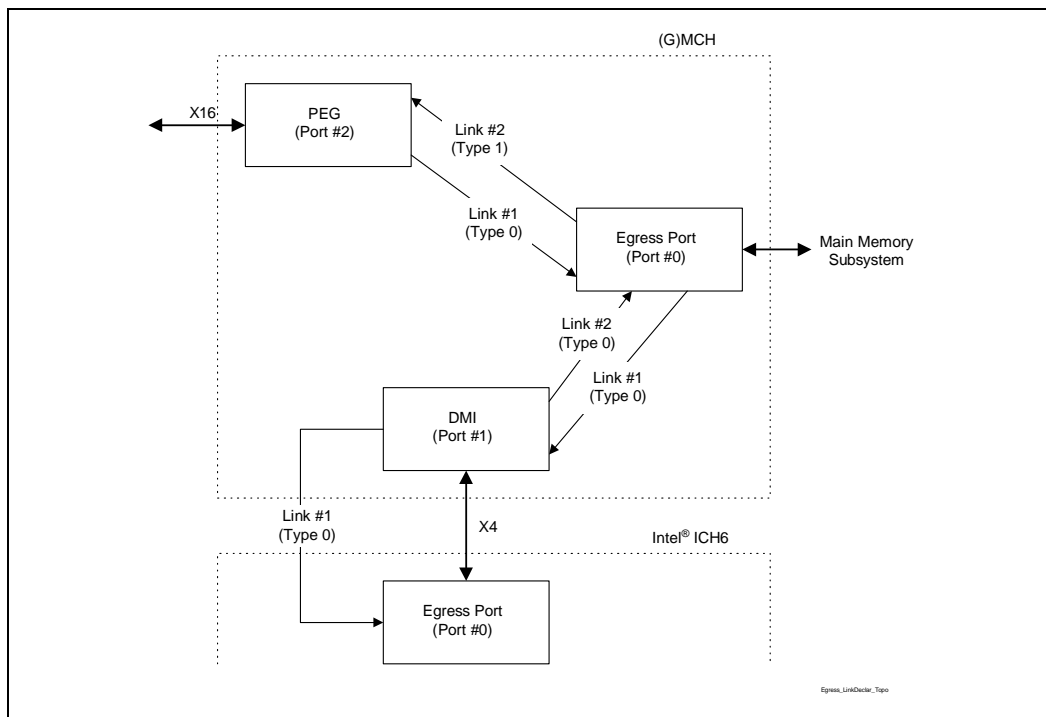
6.1.1 EPESD—EP Element Self Description

MMIO Range: EPBAR
Address Offset: 044h
Default Value: 00000201h
Access: R/WO, RO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration capability.

Bit	Access & Default	Description
31:24	RO 00h	**Port Number:** This field specifies the port number associated with this element with respect to the component that contains this element. A value of 00h indicates to configuration software that this is the default egress port.
23:16	R/WO 00h	**Component ID:** This field identifies the physical component that contains this Root Complex Element. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:8	RO 02h	**Number of Link Entries:** This field indicates the number of link entries following the Element Self Description. This field reports 2 (one each for PCI Express* x16 Graphics Interface and DMI).
7:4		Reserved
3:0	RO 1h	**Element Type:** This field Indicates the type of the Root Complex Element. 1h = Port to system memory

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6.1.2   EPLE1D—EP Link Entry 1 Description

MMIO Range: EPBAR
Address Offset: 050h
Default Value: 0100h
Access: R/WO, RO
Size: 32 bits

This register provides the First part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 01h	**Target Port Number:** This field specifies the port number associated with the element targeted by this link entry (DMI). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00h	**Target Component ID:** This field identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved; Component IDs start at 1.
		This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2		Reserved
1	RO 0b	**Link Type:** This bit indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO 0b	**Link Valid**
		0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

6.1.3   EPLE1A—EP Link Entry 1 Address

MMIO Range: EPBAR
Address Offset: 058h
Default Value: 0000000000000000h
Access: R/WO
Size: 64 bits

This register provides the second part of a Link Entry, which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:32		Reserved
31:12	R/WO 0 0000h	**Link Address:** This field provides the memory-mapped base address of the RCRB that is the target element (DMI) for this link entry.
11:0		Reserved

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6.1.4 EPLE2D—EP Link Entry 2 Description

MMIO Range: EPBAR
Address Offset: 060h
Default Value: 02000002h
Access: R/WO, RO
Size: 32 bits

This register provides the First part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 02h	**Target Port Number:** This field specifies the port number associated with the element targeted by this link entry (PCI Express* x16 Graphics Interface). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00h	**Target Component ID:** This field identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved; Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2		Reserved
1	RO 1b	**Link Type:** 1 = Link points to configuration space of the integrated device that controls the x16 root port. The link address specifies the configuration address (segment, bus, device, function) of the target root port.
0	R/WO 0b	**Link Valid** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

6.1.5 EPLE2A—EP Link Entry 2 Address

MMIO Range: EPBAR
Address Offset: 068h
Default Value: 0000000000008000h
Access: RO
Size: 64 bits

This register provides the second part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:28		Reserved
27:20	RO 00h	**Bus Number**
19:15	RO 0 0001b	**Device Number:** Target for this link is PCI Express* x16 port (Device 1).
14:12	RO 000b	**Function Number**
11:0		Reserved

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7 DMIBAR Registers—Direct Media Interface (DMI) RCRB

This Root Complex Register Block (RCRB) controls the MCH-Intel ICH6 serial interconnect. The base address of this space is programmed in DMIBAR in device 0 configuration space. These registers are offset from the DMIBAR base address

Table 7-1. DMI Register Address Map Summary

Address offset	Register Symbol	Register Name	PCI Dev #
000–003h	DMIVCECH	DMI Virtual Channel Enhanced Capability Header	DMIBAR
004–007h	DMIPVCCAP1	DMI Port VC Capability Register 1	DMIBAR
008–00Bh	DMIPVCCAP2	DMI Port VC Capability Register 2	DMIBAR
00C–00Dh	DMIPVCCTL	DMI Port VC Control	DMIBAR
00E–00Fh	—	**Reserved**	DMIBAR
010–013h	DMIVC0RCAP	DMI VC0 Resource Capability	DMIBAR
014–017h	DMIVC0RCTL	DMI VC0 Resource Control	DMIBAR
018–019h	—	**Reserved**	DMIBAR
01A–01Bh	DMIVC0RSTS	DMI VC0 Resource Status	DMIBAR
01C–01Fh	DMIVC1RCAP	DMI VC1 Resource Capability	DMIBAR
020–023h	DMIVC1RCTL	DMI VC1 Resource Control	DMIBAR
024–025h	—	**Reserved**	DMIBAR
026–027h	DMIVC1RSTS	DMI VC1 Resource Status	DMIBAR
028–083h	—	**Reserved**	DMIBAR
084–087h	DMILCAP	DMI Link Capabilities	DMIBAR
088–089h	DMILCTL	DMI Link Control	DMIBAR
08A–08Bh	DMILSTS	DMI Link Status	DMIBAR
08C–FFFh	—	**Reserved**	DMIBAR

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7.1 Direct Media Interface (DMI) RCRB Register Details

7.1.1 DMIVCECH—DMI Virtual Channel Enhanced Capability Header

MMIO Range: DMIBAR
Address Offset: 000h
Default Value: 04010002h
Access: RO
Size: 32 bits

This register indicates DMI Virtual Channel capabilities.

Bit	Access & Default	Description
31:20	RO 040h	**Pointer to Next Capability:** This field indicates the next item in the list.
19:16	RO 1h	**Capability Version:** This field indicates support as a version 1 capability structure.
15:0	RO 0002h	**Capability ID:** This field indicates this is the Virtual Channel capability item.

7.1.2 DMIPVCCAP1—DMI Port VC Capability Register 1

MMIO Range: DMIBAR
Address Offset: 004h
Default Value: 00000001h
Access: R/WO, RO
Size: 32 bits

This register describes the configuration of Virtual Channels associated with this port.

Bit	Access & Default	Description
31:12		Reserved
11:10	RO 00b	**Port Arbitration Table Entry Size (PATS):** This field indicates the size of the port arbitration table is 4 bits (to allow up to 8 ports).
9:8	RO 00b	**Reference Clock (RC)** Fixed at 100 ns.
7		Reserved
6:4	RO 000b	**Low Priority Extended VC Count (LPEVC):** This field indicates that there are no additional VCs of low priority with extended capabilities.
3		Reserved
2:0	R/WO 001b	**Extended VC Count:** This field indicates that there is one additional VC (VC1) that exists with extended capabilities.

7.1.3 DMIPVCCAP2—DMI Port VC Capability Register 2

MMIO Range:	DMIBAR
Address Offset:	008h
Default Value:	00000001h
Access:	RO
Size:	32 bits

This register describes the configuration of Virtual Channels associated with this port.

Bit	Access & Default	Description
31:24	RO 00h	**VC Arbitration Table Offset (ATO):** This field indicates that no table is present for VC arbitration since it is fixed.
23:8		Reserved
7:0	RO 01h	**VC Arbitration Capability:** This field indicates that the VC arbitration is fixed in the root complex. VC1 is highest priority and VC0 is lowest priority.

7.1.4 DMIPVCCTL—DMI Port VC Control

MMIO Range:	DMIBAR
Address Offset:	00Ch
Default Value:	00000000h
Access:	R/W, RO
Size:	16 bits

Bit	Access & Default	Description
15:4		Reserved
3:1	R/W 000b	**VC Arbitration Select:** This field indicates which VC should be programmed in the VC arbitration table. The root complex takes no action on the setting of this field since there is no arbitration table.
0	RO 0b	**Load VC Arbitration Table (LAT):** This field indicates that the table programmed should be loaded into the VC arbitration table. This bit is defined as read/write with always returning 0 on reads.

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7.1.5 DMIVC0RCAP—DMI VC0 Resource Capability

MMIO Range: DMIBAR
Address Offset: 010h
Default Value: 00000001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:24	RO 00h	**Port Arbitration Table Offset (AT):** This VC implements no port arbitration table since the arbitration is fixed.
23		Reserved
22:16	RO 00h	**Maximum Time Slots (MTS):** This VC implements fixed arbitration, and therefore this field is not used.
15	RO 0b	**Reject Snoop Transactions (RTS):** This VC must be able to take snoopable transactions.
14	RO 0b	**Advanced Packet Switching (APS):** This VC is capable of all transactions, not just advanced packet switching transactions.
13:8		Reserved
7:0	RO 01h	**Port Arbitration Capability (PAC):** This field indicates that this VC uses fixed port arbitration.

7.1.6 DMIVC0RCTL0—DMI VC0 Resource Control

MMIO Range: DMIBAR
Address Offset: 014h
Default Value: 8000007Fh
Access: R/W, RO
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access & Default	Description
31	RO 1b	**Virtual Channel Enable (EN):** Enables the VC when set. Disables the VC when cleared.
30:27		Reserved
26:24	RO 000b	**Virtual Channel Identifier (ID):** Indicates the ID to use for this virtual channel.
23:20		Reserved
19:17	R/W 0h	**Port Arbitration Select (PAS):** Indicates which port table is being programmed. The root complex takes no action on this setting since the arbitration is fixed and there is no arbitration table.
16	RO 0b	**Load Port Arbitration Table (LAT):** The root complex does not implement an arbitration table for this virtual channel.
15:8		Reserved
7:1	R/W 7Fh	**Transaction Class / Virtual Channel Map (TVM):** This field indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel.
0		Reserved

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7.1.7　DMIVC0RSTS—DMI VC0 Resource Status

MMIO Range:　　　　　　　　DMIBAR
Address Offset:　　　　　　　01Ah
Default Value:　　　　　　　　00000002h
Access:　　　　　　　　　　　RO
Size:　　　　　　　　　　　　16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 1b	**VC Negotiation Pending (NP):** 0 = Virtual channel is Not being negotiated with ingress ports. 1 = Virtual channel is still being negotiated with ingress ports.
0	RO 0b	**Port Arbitration Tables Status (ATS):** There is no port arbitration table for this VC, so this bit is reserved at 0.

7.1.8　DMIVC1RCAP—DMI VC1 Resource Capability

MMIO Range:　　　　　　　　DMIBAR
Address Offset:　　　　　　　01Ch
Default Value:　　　　　　　　00008001h
Access:　　　　　　　　　　　RO
Size:　　　　　　　　　　　　32 bits

Bit	Access & Default	Description
31:24	RO 00h	**Port Arbitration Table Offset (AT):** This field indicates the location of the port arbitration table in the root complex. A value of 3h indicates the table is at offset 30h.
23		Reserved
22:16	RO 00h	**Maximum Time Slots (MTS):** This value is updated by platform BIOS based upon the determination of the number of time slots available in the platform.
15	RO 1b	**Reject Snoop Transactions (RTS):** All snoopable transactions on VC1 are rejected. This VC is for isochronous transfers only.
14	RO 0b	**Advanced Packet Switching (APS):** This VC is capable of all transactions, not just advanced packet switching transactions.
13:8		Reserved
7:0	RO 01h	**Port Arbitration Capability (PAC):** This field indicates the port arbitration capability is time-based WRR of 128 phases.

7.1.9 DMIVC1RCTL1—DMI VC1 Resource Control

MMIO Range: DMIBAR
Address Offset: 020h
Default Value: 00100000h
Access: R/W, RO
Size: 32 bits

This register controls the resources associated with Virtual Channel 1.

Bit	Access & Default	Description
31	R/W 0b	**Virtual Channel Enable (EN):** 0 = Disable. 1 = Enable.
30:27	RO 0h	Reserved
26:24	R/W 001b	**Virtual Channel Identifier (ID):** This field indicates the ID to use for this virtual channel.
23:20		Reserved
19:17	R/W 0h	**Port Arbitration Select (PAS):** This field indicates which port table is being programmed. The only permissible value of this field is 4h for the time-based WRR entries.
16	RO 0b	**Load Port Arbitration Table (LAT):** When set, the port arbitration table is loaded based upon the PAS field in this register. This bit always returns 0 when read.
15:8		Reserved
7:1	R/W 00h	**Transaction Class / Virtual Channel Map (TVM):** This field indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel.
0		Reserved

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7.1.10 DMIVC1RSTS—DMI VC1 Resource Status

MMIO Range: DMIBAR
Address Offset: 026h
Default Value: 0000h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 0b	**VC Negotiation Pending (NP):** 0 = Virtual channel is Not being negotiated with ingress ports. 1 = Virtual channel is still being negotiated with ingress ports.
0	RO 0b	**Port Arbitration Tables Status (ATS):** This bit indicates the coherency status of the port arbitration table. 1 = LAT (offset 000Ch:bit 0) is written with value 1 and PAS (offset 0014h:bits19:17) has value of 4h. 0 = This bit is cleared after the table has been updated.

7.1.11 DMILCAP—DMI Link Capabilities

MMIO Range: DMIBAR
Address Offset: 084h
Default Value: 00012C41h
Access: R/WO, RO
Size: 32 bits

This register indicates DMI specific capabilities.

Bit	Access & Default	Description
31:18		Reserved
17:15	R/WO 010b	**L1 Exit Latency (EL1).** L1 not supported on DMI.
14:12	R/WO 010b	**L0s Exit Latency (EL0):** This field indicates that exit latency is 128 ns to less than 256 ns.
11:10	RO 11b	**Active State Link PM Support (APMS):** This field indicates that L0s is supported on DMI.
9:4	RO 4h	**Maximum Link Width (MLW):** This field indicates the maximum link width is 4 ports.
3:0	RO 1h	**Maximum Link Speed (MLS):** This field indicates the link speed is 2.5 Gb/s.

7.1.12   DMILCTL—DMI Link Control

MMIO Range: DMIBAR
Address Offset: 088h
Default Value: 0000h
Access: R/W
Size: 16 bits

This register allows control of DMI.

Bit	Access & Default	Description
15:8		Reserved
7	R/W 0h	**Extended Synch (ES):** 1 = Forces extended transmission of FTS ordered sets when exiting L0s prior to entering L0 and extra TS1 sequences at exit from L1 prior to entering L0.
6:2		Reserved
1:0	R/W 00b	**Active State Link PM Control (APMC):** Indicates whether DMI should enter L0s. 00 = Disabled 01 = L0s entry enabled 10 = Reserved 11 = Reserved

7.1.13   DMILSTS—DMI Link Status

MMIO Range: DMIBAR
Address Offset: 08Ah
Default Value: 0001h
Access: RO
Size: 16 bits

This register indicates DMI status.

Bit	Access & Default	Description
15:10		Reserved
9:4	RO 00h	**Negotiated Link Width (NLW):** This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed). Negotiated link width is x4 (000100b). All other encodings are reserved.
3:0	RO 1h	**Link Speed (LS)** Link is 2.5 Gb/s.

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8 Host-PCI Express* Graphics Bridge Registers (D1:F0)

Device 1contains the controls associated with the PCI Express x16 root port that is the intended to attach as the point for external graphics. It is typically referred to as PCI Express* x16 Graphics Interface port. In addition, it also functions as the virtual PCI-to-PCI bridge.

Warning: When reading the PCI Express "conceptual" registers such as this, you may not get a valid value unless the register value is stable.

The *PCI Express* Specification* defines two types of reserved bits: Reserved and Preserved:

- Reserved for future R/W implementations; software must preserve value read for writes to bits.

- Reserved and Zero: Reserved for future R/WC/S implementations; software must use 0 for writes to bits.

Unless explicitly documented as Reserved and Zero, all bits marked as reserved are part of the Reserved and Preserved type that have historically been the typical definition for Reserved.

It is important to note that most (if not all) control bits in this device cannot be modified unless the link is down. Software is required to first Disable the link, then program the registers, and then re-enable the link (which will cause a full-retrain with the new settings).

Table 8-1. Host-PCI Express* Graphics Bridge Register Address Map (D1:F0)

Address Offset	Register Symbol	Register Name	Default Value	Access
00–01h	VID1	Vendor Identification	8086h	RO
02–03h	DID1	Device Identification	2581h	RO
04–05h	PCICMD1	PCI Command	0000h	RO, R/W
06–07h	PCISTS1	PCI Status	0000h	RO, R/W
08h	RID1	Revision Identification	00h	RO
09–0Bh	CC1	Class Code	060400h	RO
0Ch	CL1	Cache Line Size	00h	R/W
0Dh	—	**Reserved**	—	—
0Eh	HDR1	Header Type	01h	RO
0F–17h	—	Reserved	—	—
18h	PBUSN1	Primary Bus Number	00h	RO
19h	SBUSN1	Secondary Bus Number	00h	RO
1Ah	SUBUSN1	Subordinate Bus Number	00h	R/W
1Bh	—	**Reserved**	—	—

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Address Offset	Register Symbol	Register Name	Default Value	Access
1Ch	IOBASE1	I/O Base Address	F0h	RO
1Dh	IOLIMIT1	I/O Limit Address	00h	R/W
1Eh–1Fh	SSTS1	Secondary Status	00h	RO, R/W/C
20–21h	MBASE1	Memory Base Address	FFF0h	R/W
22–23h	MLIMIT1	Memory Limit Address	0000h	R/W
24–25h	PMBASE1	Prefetchable Memory Base Address	FFF0h	RO, R/W
26–27h	PMLIMIT1	Prefetchable Memory Limit Address	0000h	RO, R/W
28–33h	—	**Reserved**	—	—
34h	CAPPTR1	Capabilities Pointer	88h	RO
35–3Bh	—	Reserved	—	—
3Ch	INTRLINE1	Interrupt Line	00h	R/W
3Dh	INTRPIN1	Interrupt Pin	00h	RO
3E–3Fh	BCTRL1	Bridge Control	0000h	RO, R/W
40–7Fh	—	**Reserved**	—	—
80–83h	PM_CAPID1	Power Management Capabilities	19029001h or 1902A001h	RO
84–87h	PM_CS1	Power Management Control/Status	00000000h	RO, R/W/S
88–8Bh	SS_CAPID	Subsystem ID and Vendor ID Capabilities	0000800Dh	RO
8C–8Fh	SS	Subsystem ID and Subsystem Vendor ID	00008086h	RO
90–91h	MSI_CAPID	Message Signaled Interrupts Capability ID	A005h	RO
92–93h	MC	Message Control	0000h	RO, R/W
94–97h	MA	Message Address	00000000h	RO, R/W
98–99h	MD	Message Data	0000h	R/W
9A–9Fh	—	**Reserved**	—	—
A0–A1h	PEG_CAPL	PCI Express* Capability List	0010h	RO
A2–A3h	PEG_CAP	PCI Express Capabilities	0141h	RO
A4–A7h	DCAP	Device Capabilities	00000000h	RO
A8–A9h	DCTL	Device Control	0000h	R/W
AA–ABh	DSTS	Device Status	0000h	RO
AC–AFh	LCAP	Link Capabilities	02012E01h	R/WO
B0–B1h	LCTL	Link Control	0000h	RO, R/W
B2–B3h	LSTS	Link Status	1001h	RO
B4–B7h	SLOTCAP	Slot Capabilities	00000000h	R/WO
B8–B9h	SLOTCTL	Slot Control	01C0h	R/W
BA–BBh	SLOTSTS	Slot Status	0X00h	RO, R/W/C
BC–BDh	RCTL	Root Control	0000h	R/W
BE–BFh	—	**Reserved**	—	—

Address Offset	Register Symbol	Register Name	Default Value	Access
C0–C3h	RSTS	Root Status	00000000h	RO, R/W/C
C4–EBh	—	Reserved	—	—
EC–EFh	PEGLC	PCI Express*-Graphics Legacy Control	00000000h	R/W, RO
F0–FFh	—	**Reserved**	—	—
100–103h	VCECH	Virtual Channel Enhanced Capability Header	14010002h	RO
104–107h	PVCCAP1	Port VC Capability Register 1	00000001h	RO, R/WO
108–10Bh	PVCCAP2	Port VC Capability Register 2	00000001h	RO
10C–10Dh	PVCCTL	Port VC Control	0000h	R/W
10E–10Fh	—	**Reserved**	—	—
110–113h	VC0RCAP	VC0 Resource Capability	00000000h	RO
114–117h	VC0RCTL	VC0 Resource Control	8000007Fh	RO, R/W
118–119h	—	**Reserved**	—	—
11A–11Bh	VC0RSTS	VC0 Resource Status	0000h	RO
11C–11Fh	VC1RCAP	VC1 Resource Capability	00008000h	RO
120–123h	VC1RCTL	VC1 Resource Control	01000000h	RO, R/W
124–125h	—	**Reserved**	—	—
126–127h	VC1RSTS	VC1 Resource Status	0000h	RO
128–13Fh	—	**Reserved**	—	—
140–143h	RCLDECH	Root Complex Link Declaration Enhanced Capability Header	00010005h	RO
144–147h	ESD	Element Self Description	02000100h	RO, R/WO
148–14Fh	—	**Reserved**	—	—
150–153h	LE1D	Link Entry 1 Description	00000000h	RO, R/WO
154–157h	—	**Reserved**	—	—
158–15Fh	LE1A	Link Entry 1 Address	0000000000000000h	R/WO
160–217h	—	**Reserved**	—	—
218–21Fh	PEGSSTS	PCI Express*-Graphics Sequence Status	0000000000000FFFh	RO
220–FFFh	—	**Reserved**	—	—

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8.1 Device 1 Configuration Register Details

8.1.1 VID1—Vendor Identification (D1:F0)

PCI Device: 1
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086h	**Vendor Identification (VID1):** PCI standard identification for Intel.

8.1.2 DID1—Device Identification (D1:F0)

PCI Device: 1
Address Offset: 02h
Default Value: 2581h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 2581h	**Device Identification Number (DID1):** This field is an identifier assigned to the MCH device 1 (virtual PCI-to-PCI bridge, PCI Express* Graphics port).

8.1.3   PCICMD1—PCI Command (D1:F0)

PCI Device: 1
Address Offset: 04h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:11		Reserved
10	R/W 0b	**INTA Assertion Disable:** 0 = This device is permitted to generate INTA interrupt messages. 1 = This device is prevented from generating interrupt messages. Any INTA emulation interrupts already asserted must be de-asserted when this bit is set. Only affects interrupts generated by the device (PCI INTA from a PME or Hot Plug event) controlled by this command register. It does not affect upstream MSIs, upstream PCI INTA-INTD asserts and de-assert messages.
9	RO 0b	**Fast Back-to-Back Enable (FB2B):** Not Applicable or Implemented. Hardwired to 0.
8	R/W 0b	**SERR Message Enable (SERRE1):** This bit is an enable bit for Device 1 SERR messaging. The MCH communicates the SERRB condition by sending an SERR message to the Intel® ICH6. This bit, when set, enables reporting of non-fatal and fatal errors to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI Express* specific bits in the Device Control Register 0 = The SERR message is generated by the MCH for Device 1 only under conditions enabled individually through the Device Control Register. 1 = The MCH is enabled to generate SERR messages which will be sent to the ICH6 for specific Device 1 error conditions that are individually enabled in the BCTRL1 register and for all non-fatal and fatal errors generated on the primary side of the virtual PCI to PCI Express bridge (not those received by the secondary side). The error status is reported in the PCISTS1 register.
7		Reserved
6	R/WO 0b	**Parity Error Enable (PERRE):** This bit controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set. 0 = Master Data Parity Error bit in PCI Status register **cannot** be set. 1 = Master Data Parity Error bit in PCI Status register **can** be set.
5	RO 0b	**VGA Palette Snoop:** Hardwired to 0.
4	RO 0b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0.
3	RO 0b	**Special Cycle Enable (SCE):** Hardwired to 0.

Bit	Access & Default	Description
2	R/W 0b	**Bus Master Enable (BME):** This bit does not affect forwarding of completions from the primary interface to the secondary interface. 0 = This device is prevented from making memory or I/O requests to its primary bus. Note that according to the PCI specification, as MSI interrupt messages are in-band memory writes, disabling the bus master enable bit prevents this device from generating MSI interrupt messages or passing them from its secondary bus to its primary bus. Upstream memory writes/reads, I/O writes/reads, peer writes/reads, and MSIs will all be treated as illegal cycles. Writes are forwarded to memory address 0h with byte enables de-asserted. Reads will be forwarded to memory address 0h and will return Unsupported Request status (or Master abort) in its completion packet. 1 = This device is allowed to issue requests to its primary bus. Completions for previously issued memory read requests on the primary bus will be issued when the data is available.
1	R/W 0b	**Memory Access Enable (MAE)** 0 = All of device 1's memory space is disabled. 1 = Enable the Memory and Pre-fetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers.
0	R/W 0b	**IO Access Enable (IOAE)** 0 = All of device 1's I/O space is disabled. 1 = Enable the I/O address range defined in the IOBASE1 and IOLIMIT1 registers.

8.1.4 PCISTS1—PCI Status (D1:F0)

PCI Device: 1
Address Offset: 06h
Default Value: 0000h
Access: RO, R/W/C
Size: 16 bits

This register reports the occurrence of error conditions associated with primary side of the "virtual" Host-PCI Express bridge in the MCH.

Bit	Access & Default	Description
15	RO 0b	**Detected Parity Error (DPE):** Hardwired to 0. Parity (generating poisoned TLPs) is not supported on the primary side of this device.
14	R/WC 0b	**Signaled System Error (SSE):** 1 = This bit is set when this Device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition and the SERR Enable bit in the Command register is '1'. Both received (if enabled by BCTRL1[1]) and internally detected error messages do not affect this field.
13	RO 0b	**Received Master Abort Status (RMAS):** Not Applicable or Implemented. Hardwired to 0. The concept of a master abort does not exist on primary side of this device.

Bit	Access & Default	Description
12	RO 0b	**Received Target Abort Status (RTAS):** Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
11	RO 0b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	RO 00b	**DEVSELB Timing (DEVT):** This device is not the subtractive decoded device on bus 0. This bit field is therefore hardwired to 00 to indicate that the device uses the fastest possible decode.
8	RO 0b	**Master Data Parity Error (PMDPE):** Because the primary side of the PCI Express* x16 Graphics Interface's virtual PCI-to-PCI bridge is integrated with the MCH functionality, there is no scenario where this bit will get set. Because hardware will never set this bit, it is impossible for software to have an opportunity to clear this bit or otherwise test that it is implemented. The PCI specification defines it as a R/WC; however, for this implementation, an RO definition behaves the same way and will meet all Microsoft testing requirements. This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.
7	RO 0b	**Fast Back-to-Back (FB2B):** Hardwired to 0.
6		Reserved
5	RO 0b	**66/60MHz capability (CAP66):** Hardwired to 0.
4	RO 1b	**Capabilities List:** This bit indicates that a capabilities list is present. Hardwired to 1.
3	RO 0b	**INTA Status:** This field indicates that an interrupt message is pending internally to the device. Only PME and Hot Plug sources feed into this status bit (not PCI INTA-INTD assert and de-assert messages). The INTA Assertion Disable bit, PCICMD1[10], has no effect on this bit.
2:0		Reserved

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8.1.5 RID1—Revision Identification (D1:F0)

PCI Device: 1
Address Offset: 08h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number of the MCH device 1.

Bit	Access & Default	Description
7:0	RO 00h	**Revision Identification Number (RID1):** This field indicates the number of times that this device in this component has been "stepped" through the manufacturing process. It is always the same as the RID values in all other devices in this component. 05h = B-2 Stepping

8.1.6 CC1—Class Code (D1:F0)

PCI Device: 1
Address Offset: 09h
Default Value: 060400h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access & Default	Description
23:16	RO 06h	**Base Class Code (BCC):** This field indicates the base class code for this device. 06h = Bridge device.
15:8	RO 04h	**Sub-Class Code (SUBCC):** This field indicates the sub-class code for this device. 04h = PCI-to-PCI Bridge.
7:0	RO 00h	**Programming Interface (PI):** This field indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

8.1.7 CL1—Cache Line Size (D1:F0)

PCI Device: 1
Address Offset: 0Ch
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Access & Default	Description
7:0	R/W 00h	**Cache Line Size (Scratch pad):** This field is implemented by PCI Express* devices as a read/write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

8.1.8 HDR1—Header Type (D1:F0)

PCI Device: 1
Address Offset: 0Eh
Default Value: 01h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access & Default	Description
7:0	RO 01h	**Header Type Register (HDR):** This field returns 01h to indicate that this is a single function device with bridge header layout.

8.1.9 PBUSN1—Primary Bus Number (D1:F0)

PCI Device: 1
Address Offset: 18h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies that this "virtual" Host-PCI Express bridge is connected to PCI bus 0.

Bit	Access & Default	Description
7:0	RO 00h	**Primary Bus Number (BUSN):** Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since device 1 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 0.

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8.1.10   SBUSN1—Secondary Bus Number (D1:F0)

PCI Device: 1
Address Offset: 19h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the "virtual" bridge i.e. to PCI Express Graphics. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express Graphics.

Bit	Access & Default	Description
7:0	R/W 00h	**Secondary Bus Number (BUSN):** This field is programmed by configuration software with the bus number assigned to PCI Express*-G.

8.1.11   SUBUSN1—Subordinate Bus Number (D1:F0)

PCI Device: 1
Address Offset: 1Ah
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI Express Graphics. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express Graphics.

Bit	Access & Default	Description
7:0	R/W 00h	**Subordinate Bus Number (BUSN):** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the device 1 bridge. When only a single PCI device resides on the PCI Express*-G segment, this register will contain the same value as the SBUSN1 register.

8.1.12 IOBASE1—I/O Base Address (D1:F0)

PCI Device: 1
Address Offset: 1Ch
Default Value: F0h
Access: RO
Size: 8 bits

This register controls the processor-to-PCI Express Graphics I/O access routing based on the following formula:

 $IO\_BASE \leq address \leq IO\_LIMIT$

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are treated as 0. Thus, the bottom of the defined I/O address range will be aligned to a 4-KB boundary.

Bit	Access & Default	Description
7:4	R/W Fh	**I/O Address Base (IOBASE):** This field corresponds to A[15:12] of the I/O addresses passed by bridge 1 to PCI Express*-G. BIOS must not set this register to 00h; otherwise, 0CF8h/0CFCh accesses will be forwarded to the PCI Express hierarchy associated with this device.
3:0		Reserved

8.1.13 IOLIMIT1—I/O Limit Address (D1:F0)

PCI Device: 1
Address Offset: 1Dh
Default Value: 00h
Access: R/W
Size: 8 bits

This register controls the processor-to-PCI Express Graphics I/O access routing based on the following formula:

 $IO\_BASE \leq address \leq IO\_LIMIT$

Only the upper 4 bits are programmable. For the purposes of address decode, address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4-KB aligned address block.

Bit	Access & Default	Description
7:4	R/W 0h	**I/O Address Limit (IOLIMIT):** This field corresponds to A[15:12] of the I/O address limit of device 1. Devices between this upper limit and IOBASE1 will be passed to the PCI Express* hierarchy associated with this device.
3:0		Reserved

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8.1.14   SSTS1—Secondary Status (D1:F0)

PCI Device: 1
Address Offset: 1Eh
Default Value: 00h
Access: RO, R/W/C
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e., PCI Express Graphics side) of the "virtual" PCI-PCI Bridge in the MCH.

Bit	Access & Default	Description
15	R/WC 0b	**Detected Parity Error (DPE):** 1 = The MCH received across the link (upstream) a Posted Write Data Poisoned TLP (EP=1).
14	R/WC 0b	**Received System Error (RSE):** 1 = Secondary side sends an ERR_FATAL or ERR_NONFATAL message due to an error detected by the secondary side, and the SERR Enable bit in the Bridge Control register is 1.
13	R/WC 0b	**Received Master Abort (RMA):** 1 = Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a completion with **Unsupported Request** Completion Status.
12	R/WC 0b	**Received Target Abort (RTA):** 1 = Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a completion with **Completer Abort** Completion Status.
11	RO 0b	**Signaled Target Abort (STA):** Hardwired to 0. The MCH does not generate Target Aborts (the MCH will never complete a request using the Completer Abort Completion status).
10:9	RO 00b	**DEVSELB Timing (DEVT):** Hardwired to 0.
8	R/WC 0b	**Master Data Parity Error (SMDPE):** 1 = The MCH received across the link (upstream) a Read Data Completion Poisoned TLP (EP=1). Note: This bit can only be set when the Parity Error Enable bit in the Bridge Control register is set.
7	RO 0b	**Fast Back-to-Back (FB2B):** Hardwired to 0.
6		Reserved
5	RO 0b	**66/60 MHz capability (CAP66):** Hardwired to 0.
4:0		Reserved

8.1.15 MBASE1—Memory Base Address (D1:F0)

PCI Device: 1
Address Offset: 20h
Default Value: FFF0h
Access: R/W
Size: 16 bits

This register controls the processor to PCI Express Graphics non-prefetchable memory access routing based on the following formula:

$$MEMORY\_BASE \leq address \leq MEMORY\_LIMIT$$

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access & Default	Description
15:4	R/W FFFh	**Memory Address Base (MBASE):** This field corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express*.
3:0		Reserved

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8.1.16   MLIMIT1—Memory Limit Address (D1:F0)

PCI Device: 1
Address Offset: 22h
Default Value: 0000h
Access: R/W
Size: 16 bits

This register controls the processor-to-PCI Express Graphics non-prefetchable memory access routing based on the following formula:

    MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return zeroes when read. Configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Note: Memory range covered by MBASE and MLIMIT registers are used to map non-pre-fetchable PCI Express Graphics address ranges (typically, where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map pre-fetchable address ranges (typically, graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the pre-fetchable address range for improved processor-PCI Express memory access performance.

Note: Configuration software is responsible for programming all address range registers (pre-fetchable, non-prefetchable) with the values that provide exclusive address ranges (i.e., prevent overlap with each other and/or with the ranges covered with the main memory). There is no provision in the MCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not guaranteed.

Bit	Access & Default	Description
15:4	R/W 000h	**Memory Address Limit (MLIMIT):** This field corresponds to A[31:20] of the upper limit of the address range passed to PCI Express*.
3:0		Reserved

8.1.17   PMBASE1—Prefetchable Memory Base Address (D1:F0)

PCI Device:	1
Address Offset:	24h
Default Value:	FFF0h
Access:	RO, R/W
Size:	16 bits

This register, in conjunction with the corresponding Upper Base Address register, controls the processor-to-PCI Express Graphics prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE ≤ address ≤ PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access & Default	Description
15:4	R/W FFFh	**Prefetchable Memory Base Address (MBASE):** This field corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express*.
3:0	RO 0h	**64-bit Address Support:** This field indicates that the bridge supports only 32 bit addresses.

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8.1.18 PMLIMIT1—Prefetchable Memory Limit Address (D1:F0)

PCI Device:	1
Address Offset:	26h
Default Value:	0000h
Access:	RO, R/W
Size:	16 bits

This register, in conjunction with the corresponding Upper Limit Address register, controls the processor-to-PCI Express Graphics prefetchable memory access routing based on the following formula:

$$PREFETCHABLE\_MEMORY\_BASE \leq address \leq PREFETCHABLE\_MEMORY\_LIMIT$$

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. The configuration software must initialize this register. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e., prefetchable) from the processor perspective.

Bit	Access & Default	Description
15:4	R/W 000h	**Prefetchable Memory Address Limit (PMLIMIT):** This field corresponds to A[31:20] of the upper limit of the address range passed to PCI Express*.
3:0	RO 0h	**64-bit Address Support:** This field indicates the bridge supports only 32 bit addresses.

8.1.19 CAPPTR1—Capabilities Pointer (D1:F0)

PCI Device:	1
Address Offset:	34h
Default Value:	88h
Access:	RO
Size:	8 bits

The capabilities pointer provides the address offset to the location of the first entry in this device's linked list of capabilities.

Bit	Access & Default	Description
7:0	RO 88h	**First Capability (CAPPTR1):** The first capability in the list is the Subsystem ID and Subsystem Vendor ID Capability.

8.1.20 INTRLINE1—Interrupt Line (D1:F0)

PCI Device: 1
Address Offset: 3Ch
Default Value: 00h
Access: R/W
Size: 8 bits

This register contains interrupt line routing information. The device itself does not use this value; rather device drivers and operating systems use it to determine priority and vector information.

Bit	Access & Default	Description
7:0	R/W 00h	**Interrupt Connection:** This field is used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the system interrupt controller this device's interrupt pin is connected to.

8.1.21 INTRPIN1—Interrupt Pin (D1:F0)

PCI Device: 1
Address Offset: 3Dh
Default Value: 00h
Access: RO
Size: 8 bits

This register specifies which interrupt pin this device uses.

Bit	Access & Default	Description
7:0	RO 01h	**Interrupt Pin:** As a single function device, the PCI Express* device specifies INTA as its interrupt pin. 01h = INTA

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8.1.22   BCTRL1—Bridge Control (D1:F0)

PCI Device: 1
Address Offset: 3Eh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e., PCI Express) as well as some bits that affect the overall behavior of the "virtual" Host-PCI Express bridge embedded within MCH (e.g., VGA compatible address ranges mapping).

Bit	Access & Default	Description
15:12		Reserved
11	RO 0b	**Discard Timer SERR Enable:** Hardwired to 0.
10	RO 0b	**Discard Timer Status:** Hardwired to 0.
9	RO 0b	**Secondary Discard Timer:** Hardwired to 0.
8	RO 0b	**Primary Discard Timer:** Hardwired to 0.
7	RO 0b	**Fast Back-to-Back Enable (FB2BEN):** Hardwired to 0.
6	R/W 0b	**Secondary Bus Reset (SRESET):** Setting this bit triggers a hot reset on the corresponding PCI Express* Port.
5	RO 0b	**Master Abort Mode (MAMODE):** When acting as a master, unclaimed reads that experience a master abort returns all 1s and any writes that experience a master abort completes normally and the data is thrown away. Hardwired to 0.
4	R/W 0b	**VGA 16-bit Decode:** This bit enables the PCI-to-PCI bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit only has meaning if bit 3 (VGA Enable) of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. 0 = Execute 10-bit address decodes on VGA I/O accesses. 1 = Execute 16-bit address decodes on VGA I/O accesses.
3	R/W 0b	**VGA Enable (VGAEN):** This bit controls the routing of processor-initiated transactions targeting VGA compatible I/O and memory address ranges. See the VGAEN/MDAP table in Device 0, offset 97h[0].

Bit	Access & Default	Description
2	R/W 0b	**ISA Enable (ISAEN):** This bit is needed to exclude legacy resource decode to route ISA resources to legacy decode path. This bit modifies the response by the MCH to an I/O access issued by the processor that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0 = All addresses defined by the IOBASE and IOLIMIT for processor I/O transactions will be mapped to PCI Express Graphics. 1 = MCH will not forward to PCI Express Graphics any I/O transactions addressing the last 768 bytes in each 1-KB block, even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to PCI Express Graphics, these cycles are forwarded to DMI where they can be subtractively or positively claimed by the ISA bridge.
1	R/W 0b	**SERR Enable (SERREN)** 0 = No forwarding of error messages from secondary side to primary side that could result in an SERR. 1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages result in SERR message when individually enabled by the Root Control register.
0	RO 0b	**Parity Error Response Enable (PEREN):** This bit controls whether or not the Master Data Parity Error bit in the Secondary Status register is set when the MCH receives across the link (upstream) a Read Data Completion Poisoned TLP. 0 = Master Data Parity Error bit in Secondary Status register **cannot** be set. 1 = Master Data Parity Error bit in Secondary Status register **can** be set..

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8.1.23   PM_CAPID1—Power Management Capabilities (D1:F0)

PCI Device: 1
Address Offset: 80h
Default Value: 1902 9001h or 1902 A001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:27	RO 19h	**PME Support:** This field indicates the power states in which this device may indicate PME wake via PCI Express messaging. D0, D3hot, and D3cold. This device is not required to do anything to support D3hot and D3cold; it simply must report that those states are supported. Refer to the PCI Power Management 1.1 specification for encoding explanation and other power management details.
26	RO 0b	**D2:** Hardwired to 0 to indicate that the D2 power management state is NOT supported.
25	RO 0b	**D1:** Hardwired to 0 to indicate that the D1 power management state is NOT supported.
24:22	RO 000b	**Auxiliary Current:** Hardwired to 0 to indicate that there are no 3.3Vaux auxiliary current requirements.
21	RO 0 b	**Device Specific Initialization (DSI):** Hardwired to 0 to indicate that special initialization of this device is NOT required before generic class device driver is to use it.
20	RO 0b	**Auxiliary Power Source (APS):** Hardwired to 0.
19	RO 0b	**PME Clock:** Hardwired to 0 to indicate this device does NOT support PME# generation.
18:16	RO 010b	**PCI PM CAP Version:** Hardwired to 02h to indicate there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the *PCI Power Management Interface Specification*.
15:8	RO 90h or A0h	**Pointer to Next Capability:** This field contains a pointer to the next item in the capabilities list. If MSICH (CAPL[0] @ 7Fh) is 0, then the next item in the capabilities list is the Message Signaled Interrupts (MSI) capability at 90h. If MSICH (CAPL[0] @ 7Fh) is 1, then the next item in the capabilities list is the PCI Express* capability at A0h.
7:0	RO 01h	**Capability ID:** Value of 01h identifies this linked list item (capability structure) as being for PCI Power Management registers.

8.1.24 PM_CS1—Power Management Control/Status (D1:F0)

PCI Device: 1
Address Offset: 84h
Default Value: 00000000h
Access: RO, R/W/S
Size: 32 bits

Bit	Access & Default	Description
31:16		Reserved
15	RO 0b	**PME Status:** This bit indicates that this device does not support PME# generation from $D3_{cold}$.
14:13	RO 00b	**Data Scale:** This field indicates that this device does not support the power management data register.
12:9	RO 0h	**Data Select:** This field indicates that this device does not support the power management data register.
8	R/W/S 0b	**PME Enable:** This bit indicates that this device does not generate PMEB assertion from any D-state. 0 = PMEB generation not possible from any D State 1 = PMEB generation enabled from any D State The setting of this bit has no effect on hardware. See PM_CAP[15:11]
7:2		Reserved
1:0	R/W 00b	**Power State:** This field indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00 = D0 01 = D1 (Not supported in this device.) 10 = D2 (Not supported in this device.) 11 = D3 Support of D3cold does not require any special action. While in the D3hot state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state to be fully functional. There is no hardware functionality required to support these power states.

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8.1.25 SS_CAPID—Subsystem ID and Vendor ID Capabilities (D1:F0)

PCI Device: 1
Address Offset: 88h
Default Value: 0000800Dh
Access: RO
Size: 32 bits

This capability is used to uniquely identify the subsystem where the PCI device resides. Because this device is an integrated part of the system and not an add-in device, it is anticipated that this capability will never be used. However, it is necessary because Microsoft will test for its presence.

Bit	Access & Default	Description
31:16		Reserved
15:8	RO 80h	**Pointer to Next Capability:** This field contains a pointer to the next item in the capabilities list which is the PCI Power Management capability.
7:0	RO 0D h	**Capability ID:** A value of 0Dh identifies this linked list item (capability structure) as being for SSID/SSVID registers in a PCI-to-PCI Bridge.

8.1.26 SS—Subsystem ID and Subsystem Vendor ID (D1:F0)

PCI Device: 1
Address Offset: 8Ch
Default Value: 00008086h
Access: RO
Size: 32 bits

System BIOS can be used as the mechanism for loading the SSID/SVID values. These values must be preserved through power management transitions and hardware reset.

Bit	Access & Default	Description
31:16	R/WO 0000h	**Subsystem ID (SSID):** This field identifies the particular subsystem and is assigned by the vendor.
15:0	R/WO 8086h	**Subsystem Vendor ID (SSVID):** This field identifies the manufacturer of the subsystem and is the same as the vendor ID that is assigned by the PCI Special Interest Group.

8.1.27 MSI_CAPID—Message Signaled Interrupts Capability ID (D1:F0)

PCI Device: 1
Address Offset: 90h
Default Value: A005h
Access: RO
Size: 16 bits

When a device supports MSI, it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

The reporting of the existence of this capability can be disabled by setting MSICH (CAPL [0] @ 7Fh). In that case walking this linked list will skip this capability and, instead, go directly from the PCI PM capability to the PCI Express capability.

Bit	Access & Default	Description
15:8	RO A0h	**Pointer to Next Capability:** This field contains a pointer to the next item in the capabilities list that is the PCI Express* capability.
7:0	RO 05h	**Capability ID:** 05h = Identifies this linked list item (capability structure) as being for MSI registers.

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8.1.28   MC—Message Control (D1:F0)

PCI Device: 1
Address Offset: 92h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so.

If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access & Default	Description
15:8		Reserved
7	RO 0b	**64-bit Address Capable:** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address.
6:4	R/W 000b	**Multiple Message Enable (MME):** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. 000 = 1 message allocated 001–111 = Reserved
3:1	RO 000b	**Multiple Message Capable (MMC):** System software reads this field to determine the number of messages being requested by this device. 000 = 1 message requested 001–111 = Reserved
0	R/W 0b	**MSI Enable (MSIEN)** Controls the ability of this device to generate MSIs. 0 = MSI will not be generated. 1 = MSI will be generated when we receive PME or HotPlug messages. INTA will not be generated and INTA Status (PCISTS1[3]) will not be set.

8.1.29   MA—Message Address (D1:F0)

PCI Device: 1
Address Offset: 94h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

Bit	Access & Default	Description
31:2	R/W 00000000 h	**Message Address:** This field is used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO 00b	**Force DWord Align:** Hardwired to 0 so that addresses assigned by system software are always aligned on a DWord address boundary.

8.1.30   MD—Message Data (D1:F0)

PCI Device: 1
Address Offset: 98h
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access & Default	Description
15:0	R/W 0000h	**Message Data:** This field provides a base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. This register supplies the lower 16 bits.

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8.1.31 PEG_CAPL—PCI Express* Capability List (D1:F0)

PCI Device: 1
Address Offset: A0h
Default Value: 0010h
Access: RO
Size: 16 bits

This register enumerates the PCI Express capability structure.

Bit	Access & Default	Description
15:8	RO 00h	**Pointer to Next Capability:** This value terminates the capabilities list. The Virtual Channel capability and any other PCI Express* specific capabilities that are reported via this mechanism are in a separate capabilities list located entirely within PCI Express extended configuration space.
7:0	RO 10h	**Capability ID:** This field identifies this linked list item (capability structure) as being for PCI Express registers.

8.1.32 PEG_CAP—PCI Express*-G Capabilities (D1:F0)

PCI Device: 1
Address Offset: A2h
Default Value: 0141h
Access: RO
Size: 16 bits

Indicates PCI Express device capabilities.

Bit	Access & Default	Description
15:14		Reserved
13:9	RO 00h	**Interrupt Message Number:** Hardwired to 0.
8	R/WO 1b	**Slot Implemented** 0 = The PCI Express* Link associated with this port is connected to an integrated component or is disabled. 1 = The PCI Express Link associated with this port is connected to a slot. BIOS must initialize this field appropriately if a slot connection is not implemented.
7:4	RO 4h	**Device/Port Type:** Hardwired to 0100 to indicate root port of PCI Express Root Complex.
3:0	RO 1h	**PCI Express Capability Version:** Hardwired to 1 as it is the first version.

8.1.33   DCAP—Device Capabilities (D1:F0)

PCI Device: 1
Address Offset: A4h
Default Value: 00000000h
Access: RO
Size: 32 bits

This register indicates PCI Express link capabilities.

Bit	Access & Default	Description
31:6		Reserved
5	RO 0b	**Extended Tag Field Supported:** Hardwired to indicate support for 5-bit Tags as a Requestor.
4:3	RO 00b	**Phantom Functions Supported:** Hardwired to 0.
2:0	RO 000b	**Max Payload Size:** Hardwired to indicate 128B maximum supported payload for Transaction Layer Packets (TLP).

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8.1.34   DCTL—Device Control (D1:F0)

PCI Device: 1
Address Offset: A8h
Default Value: 0000h
Access: R/W
Size: 16 bits

This register provides control for PCI Express device specific capabilities.

The error reporting enable bits are in reference to errors detected by this device, not error messages received across the link. The reporting of error messages (ERR_CORR, ERR_NONFATAL, ERR_FATAL) received by Root Port is controlled exclusively by Root Port Command Register.

Bit	Access & Default	Description
15:8		Reserved
7:5	R/W 000b	**Max Payload Size** 000 = 128B maximum supported payload for Transaction Layer Packets (TLP). As a receiver, the device must handle TLPs as large as the set value; as transmitter, the device must not generate TLPs exceeding the set value. **Note:** All other encodings are reserved.
4		Reserved
3	R/W 0b	**Unsupported Request Reporting Enable:** 0 = Disable. 1 = Enable. Unsupported Requests will be reported. Note that reporting of error messages received by Root Port is controlled exclusively by Root Control register.
2	R/W 0b	**Fatal Error Reporting Enable:** 0 = Disable. 1 = Enable. Fatal errors will be reported. For a Root Port, the reporting of fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	R/W 0b	**Non-Fatal Error Reporting Enable:** 0 = Disable. 1 = Enable. Non-fatal errors will be reported. For a Root Port, the reporting of non-fatal errors is internal to the root. No external ERR_NONFATAL message is generated. Uncorrectable errors can result in degraded performance.
0	R/W 0b	**Correctable Error Reporting Enable:** 0 = Disable. 1 = Enable. Correctable errors will be reported. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_CORR message is generated.

8.1.35   DSTS—Device Status (D1:F0)

PCI Device: 1
Address Offset: AAh
Default Value: 0000h
Access: RO
Size: 16 bits

This register reflects status corresponding to controls in the Device Control register.

Note: The error reporting bits are in reference to errors detected by this device, not errors messages received across the link.

Bit	Access & Default	Description
15:6		Reserved
5	RO 0b	**Transactions Pending** 0 = All pending transactions (including completions for any outstanding non-posted requests on any used virtual channel) have been completed. 1 = Device has transaction(s) pending (including completions for any outstanding non-posted requests for all used Traffic Classes).
4		Reserved
3	R/WC 0b	**Unsupported Request Detected:** 1 = Device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register.
2	R/WC 0b	**Fatal Error Detected:** 1 = Fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.
1	R/WC 0b	**Non-Fatal Error Detected:** 1 = Non-fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.
0	R/WC 0b	**Correctable Error Detected:** 1 = Correctable error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. **Note:** The MCH may report a false 8B/10B Receiver Error when exiting L0s. This is reported thru the Correctable Error Detected bit CESTS device 1, offset 1D0h, Bit [0]. This will reduce the value of Receiver Error detection when L0s is enabled. Disable L0s for accurate Receiver Error reporting.

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8.1.36 LCAP—Link Capabilities (D1:F0)

PCI Device: 1
Address Offset: ACh
Default Value: 02012E01h
Access: R/WO
Size: 16 bits

This register indicates PCI Express device specific capabilities.

Bit	Access & Default	Description
31:24	RO 02h	**Port Number:** This field indicates the PCI Express* port number for the given PCI Express link. This field matches the value in Element Self Description [31:24].
23:18		Reserved
17:15	R/WO 010b	**L1 Exit Latency:** This field indicates the length of time this Port requires to complete the transition from L1 to L0. The value 010 b indicates the range of 2 µs to less than 4 µs. If this field is required to be any value other than the default, BIOS must initialize it accordingly. Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.
14:12	R/WO 010b	**L0s Exit Latency:** This field indicates the length of time this Port requires to complete the transition from L0s to L0. The value 010 b indicates the range of 128 ns to less than 256 ns. If this field is required to be any value other than the default, BIOS must initialize it accordingly. **Note:** When PCI Express* is operating with separate reference clocks, L0s exit latency may be greater than the setting in the L0s Exit Latency Register. Expect longer exit latency then setting in L0s Exit Latency Register. The link may enter Recovery state before reaching L0. System BIOS can program the appropriate Exit Latency and advertised N_FTS value if it detects that the downstream device is not using the common reference clock (indicated in the Slot Clock Configuration bit 12 of the device's Link Status Register)
11:10	R/WO 11b	**Active State Link PM Support:** L0s and L1 entry supported.
9:4	RO 10h	**Max Link Width:** Hardwired to indicate X16. When Force X1 mode is enabled on this PCI Express* x16 Graphics Interface device, this field reflects X1 (01h).
3:0	RO 1h	**Max Link Speed:** Hardwired to indicate 2.5 Gb/s.

8.1.37 LCTL—Link Control (D1:F0)

PCI Device: 1
Address Offset: B0h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register allows control of PCI Express link.

Bit	Access & Default	Description
15:8		Reserved
7		Reserved. Must be 0 when writing this register.
6	R/W 0b	**Common Clock Configuration** 0 = This component and the component at the opposite end of this Link are operating with asynchronous reference clock. 1 = This component and the component at the opposite end of this Link are operating with a distributed common reference clock. Components use this common clock configuration information to report the correct L0s and L1 Exit Latencies.
5	R/W 0b	**Retrain Link** 0 = Normal operation 1 = Full Link retraining is initiated by directing the Physical Layer LTSSM from L0, L0s, or L1 states to the Recovery state. This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0).
4	R/W 0b	**Link Disable** 0 = Normal operation 1 = Link is disabled. Forces the LTSSM to transition to the Disabled state (via Recovery) from L0, L0s, or L1 states. Link retraining happens automatically on 0 to 0 transition, just like when coming out of reset. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.
3	RO 0b	**Read Completion Boundary (RCB):** Hardwired to 0 to indicate 64 byte.
2		Reserved
1:0	R/W 00b	**Active State PM:** This field controls the level of active state power management supported on the given link. 00 = Disabled 01 = L0s Entry Supported 10 = Reserved 11 = L0s and L1 Entry Supported

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8.1.38 LSTS—Link Status (D1:F0)

PCI Device: 1
Address Offset: B2h
Default Value: 1001h
Access: RO
Size: 16 bits

This register indicates PCI Express link status.

Bit	Access & Default	Description
15:13		Reserved
12	RO 1b	**Slot Clock Configuration** 0 = The device uses an independent clock irrespective of the presence of a reference on the connector. 1 = The device uses the same physical reference clock that the platform provides on the connector.
11	RO 0b	**Link Training:** 1 = Link training is in progress. Hardware clears this bit once Link training is complete.
10	RO 0b	**Training Error:** 1 = This bit is set by hardware upon detection of unsuccessful training of the Link to the L0 Link state.
9:4	RO 00h	**Negotiated Width:** This field indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed). 00h = Reserved 01h = X1 04h = Reserved 08h = Reserved 10h = X16 All other encodings are reserved.
3:0	RO 1h	**Negotiated Speed:** This field indicates negotiated link speed. 1h = 2.5 Gb/s All other encodings are reserved.

8.1.39 SLOTCAP—Slot Capabilities (D1:F0)

PCI Device: 1
Address Offset: B4h
Default Value: 00000000h
Access: R/WO
Size: 32 bits

PCI Express slot-related registers allow for the support of Hot-Plug.

Bit	Access & Default	Description
31:19	R/WO 0000h	**Physical Slot Number:** This field indicates the physical slot number attached to this Port. This field must be initialized by BIOS to a value that assigns a slot number that is globally unique within the chassis.
18:17		Reserved
16:15	R/WO 00b	**Slot Power Limit Scale:** This field specifies the scale used for the Slot Power Limit Value. 00 = 1.0x 01 = 0.1x 10 = 0.01x 11 = 0.001x If this field is written, the link sends a Set_Slot_Power_Limit message.
14:7	R/WO 00h	**Slot Power Limit Value:** In combination with the Slot Power Limit Scale value, this field specifies the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. If this field is written, the link sends a Set_Slot_Power_Limit message.
6	R/WO 0b	**Hot-plug Capable:** This field indicates that this slot is capable of supporting Hot-plug operations.
5	R/WO 0b	**Hot-plug Surprise:** This field indicates that a device present in this slot might be removed from the system without any prior notification.
4	R/WO 0b	**Power Indicator Present:** This field indicates that a Power Indicator is implemented on the chassis for this slot.
3	R/WO 0b	**Attention Indicator Present:** This field indicates that an Attention Indicator is implemented on the chassis for this slot.
2:1		Reserved
0	R/WO 0b	**Attention Button Present:** This field indicates that an Attention Button is implemented on the chassis for this slot. The Attention Button allows the user to request hot-plug operations.

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8.1.40   SLOTCTL—Slot Control (D1:F0)

PCI Device: 1
Address Offset: B8h
Default Value: 01C0h
Access: R/W
Size: 16 bits

PCI Express slot related registers allow for the support of Hot-Plug.

Bit	Access & Default	Description
15:10		Reserved
9:8	R/W 01b	**Power Indicator Control:** Reads to this register return the current state of the Power Indicator. Writes to this register set the Power Indicator and cause the Port to send the appropriate POWER_INDICATOR_* messages. 00 = Reserved 01 = On 10 = Blink 11 = Off
7:6	R/W 11b	**Attention Indicator Control:** Reads to this register return the current state of the Attention Indicator. Writes to this register set the Attention Indicator and cause the Port to send the appropriate ATTENTION_INDICATOR_* messages. 00 = Reserved 01 = On 10 = Blink 11 = Off
5	R/W 0b	**Hot plug Interrupt Enable:** 0 = Disable. 1 = Enables generation of hot plug interrupt on enabled hot plug events.
4	R/W 0b	**Command Completed Interrupt Enable:** 0 = Disable. 1 = Enables the generation of hot plug interrupt when the Hot plug controller completes a command.
3	R/W 0b	**Presence Detect Changed Enable:** 0 = Disable. 1 = Enables the generation of hot plug interrupt or wake message on a presence detect changed event.
2:1		Reserved
0	R/W 0b	**Attention Button Pressed Enable:** 0 = Disable. 1 = Enables the generation of hot plug interrupt or wake message on an attention button pressed event.

8.1.41 SLOTSTS—Slot Status (D1:F0)

PCI Device: 1
Address Offset: BAh
Default Value: 0X00h
Access: RO, R/W/C
Size: 16 bits

PCI Express slot-related registers allow for the support of Hot-Plug.

Bit	Access & Default	Description
15:7		Reserved
6	RO Xb	**Presence Detect State:** This bit indicates the presence of a card in the slot. 0 = Slot Empty 1 = Card Present in slot.
5		Reserved
4	R/WC 0b	**Command Completed:** 1 = Hot plug controller completed an issued command.
3	R/WC 0b	**Presence Detect Changed:** 1 = Presence Detect change is detected. This corresponds to an edge on the signal that corresponds to bit 6 of this register (Presence Detect State).
2:1		Reserved
0	R/WC 0b	**Attention Button Pressed:** 1 = Attention Button is pressed.

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8.1.42   RCTL—Root Control (D1:F0)

PCI Device: 1
Address Offset: BCh
Default Value: 0000h
Access: R/W
Size: 16 bits

This register allows control of PCI Express Root Complex specific parameters. The system error control bits in this register determine if corresponding SERRs are generated when our device detects an error (reported in this device's Device Status register) or when an error message is received across the link. Reporting of SERR as controlled by these bits takes precedence over the SERR Enable in the PCI Command Register.

Bit	Access & Default	Description
15:4		Reserved
3	R/W 0b	**PME Interrupt Enable** 0 = No interrupts are generated as a result of receiving PME messages. 1 = Enables interrupt generation upon receipt of a PME message as reflected in the PME Status bit of the Root Status Register. A PME interrupt is also generated if the PME Status bit of the Root Status Register is set when this bit is set from a cleared state.
2	R/W 0b	**System Error on Fatal Error Enable:** This bit controls the Root Complex's response to fatal errors. 0 = No SERR generated on receipt of fatal error. 1 = Indicates that an SERR should be generated if a fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
1	R/W 0b	**System Error on Non-Fatal Uncorrectable Error Enable:** This bit controls the Root Complex's response to non-fatal errors. 0 = No SERR generated on receipt of non-fatal error. 1 = Indicates that an SERR should be generated if a non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
0	R/W 0b	**System Error on Correctable Error Enable:** This bit controls the Root Complex's response to correctable errors. 0 = No SERR generated on receipt of correctable error. 1 = Indicates that an SERR should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.

8.1.43   RSTS—Root Status (D1:F0)

PCI Device: 1
Address Offset: C0h
Default Value: 00000000h
Access: RO, R/W/C
Size: 32 bits

This register provides information about PCI Express Root Complex specific parameters.

Bit	Access & Default	Description
31:18		Reserved
17	RO 0b	**PME Pending:** This bit indicates that another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.
16	R/W/C 0b	**PME Status:** This bit indicates that the requestor ID indicated in the PME Requestor ID field asserted PME. Subsequent PMEs are kept pending until the status register is cleared by writing a 1 to this field.
15:0	RO 0000h	**PME Requestor ID:** This field indicates the PCI requestor ID of the last PME requestor.

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8.1.44   PEGLC—PCI Express*-G Legacy Control

PCI Device: 1
Address Offset: ECh
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register controls functionality that is needed by Legacy (non-PCI Express aware) OS's during run time.

Bit	Access & Default	Description
31:3	RO 0000 0000h	Reserved
2	R/W 0b	**PME GPE Enable (PMEGPE):** 0 = Do not generate GPE PME message when PME is received. 1 = Enable. Generate a GPE PME message when PME is received (Assert_PMEGPE and Deassert_PMEGPE messages on DMI). This enables the MCH to support PMEs on the PCI Express* x16 Graphics Interface port under legacy OSs.
1	R/W 0b	**Hot-Plug GPE Enable (HPGPE)** 0 = Do not generate GPE Hot-Plug message when Hot-Plug event is received. 1 = Enable. Generate a GPE Hot-Plug message when Hot-Plug Event is received (Assert_HPGPE and Deassert_HPGPE messages on DMI). This enables the MCH to support Hot-Plug on the PCI Express* x16 Graphics Interface port under legacy OSs.
0	R/W 0b	**General Message GPE Enable (GENGPE)** 0 = Do not forward received GPE assert/deassert messages. 1 = Enable. Forward received GPE assert/deassert messages. These general GPE message can be received via the PCI Express* x16 Graphics Interface port from an external Intel device and will be subsequently forwarded to the Intel® ICH6 (via Assert_GPE and Deassert_GPE messages on DMI).

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8.1.45   VCECH—Virtual Channel Enhanced Capability Header (D1:F0)

PCI Device: 1
Address Offset: 100h
Default Value: 14010002h
Access: RO
Size: 32 bits

This register indicates PCI Express device Virtual Channel capabilities.

Note: Extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definitions than standard PCI capability structures.

Bit	Access & Default	Description
31:20	RO 140h	**Pointer to Next Capability:** The Link Declaration Capability is the next in the PCI Express* extended capabilities list.
19:16	RO 1h	**PCI Express Virtual Channel Capability Version:** Hardwired to 1 to indicate compliances with the 1.0a version of the PCI Express specification.
15:0	RO 0002h	**Extended Capability ID:** Value of 0002 h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

8.1.46   PVCCAP1—Port VC Capability Register 1 (D1:F0)

PCI Device: 1
Address Offset: 104h
Default Value: 00000001h
Access: RO, R/WO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:7		Reserved
6:4	RO 000b	**Low Priority Extended VC Count:** This field indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3		Reserved
2:0	R/WO 001b	**Extended VC Count:** This field indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.

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8.1.47 PVCCAP2—Port VC Capability Register 2 (D1:F0)

PCI Device: 1
Address Offset: 108h
Default Value: 00000001h
Access: RO
Size: 32 bits

This register describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:24	RO 00h	**VC Arbitration Table Offset:** This field indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel Capability Structure. A value of 0 indicates that the table is not present (due to fixed VC priority).
23:8		Reserved
7:0	RO 01h	**VC Arbitration Capability:** This field indicates that the only possible VC arbitration scheme is hardware fixed (in the root complex). VC1 is the highest priority, VC0 is the lowest priority.

8.1.48 PVCCTL—Port VC Control (D1:F0)

PCI Device: 1
Address Offset: 10Ch
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access & Default	Description
15:4		Reserved
3:1	R/W 000b	**VC Arbitration Select:** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. The value 001b when written to this field will indicate the VC arbitration scheme is hardware fixed (in the root complex). This field can not be modified when more than one VC in the LPVC group is enabled.
0		Reserved

8.1.49 VC0RCAP—VC0 Resource Capability (D1:F0)

PCI Device: 1
Address Offset: 110h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16		Reserved
15	RO 0b	**Reject Snoop Transactions** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:0		Reserved

8.1.50 VC0RCTL—VC0 Resource Control (D1:F0)

PCI Device: 1
Address Offset: 114h
Default Value: 8000007Fh
Access: RO, R/W
Size: 32 bits

This register controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access & Default	Description
31	RO 1b	**VC0 Enable:** For VC0 this is hardwired to 1 and read only as VC0 can never be disabled.
30:27		Reserved
26:24	RO 000b	**VC0 ID:** This field assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:8		Reserved
7:1	R/W 7Fh	**TC/VC0 Map:** This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 1b	**TC0/VC0 Map:** Traffic Class 0 is always routed to VC0.

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8.1.51 VC0RSTS—VC0 Resource Status (D1:F0)

PCI Device: 1
Address Offset: 11Ah
Default Value: 0000h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 1b	**VC0 Negotiation Pending** 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0		Reserved

8.1.52 VC1RCAP—VC1 Resource Capability (D1:F0)

PCI Device: 1
Address Offset: 11Ch
Default Value: 00008000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16		Reserved
15	RO 1b	**Reject Snoop Transactions** 0 = Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1 = Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:0		Reserved

8.1.53   VC1RCTL—VC1 Resource Control (D1:F0)

PCI Device: 1
Address Offset: 120h
Default Value: 01000000h
Access: RO, R/W
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 1.

Bit	Access & Default	Description
31	R/W 0b	**VC1 Enable** 0 = Virtual Channel is disabled. 1 = Virtual Channel is enabled. See exceptions in note below. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express* port); a 0 read from this bit indicates that the Virtual Channel is currently disabled. **Notes:** • To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both Components on a Link. • To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both Components on a Link. • Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. • Software must fully disable a Virtual Channel in both Components on a Link before re-enabling the Virtual Channel.
30:27		Reserved
26:24	R/W 001b	**VC1 ID:** Assigns a VC ID to the VC resource. Assigned value must be non-zero. This field cannot be modified when the VC is already enabled.
23:8		Reserved
7:1	R/W 00h	**TC/VC1 Map:** This field indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 0b	**TC0/VC1 Map:** Traffic Class 0 is always routed to VC0.

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8.1.54   VC1RSTS—VC1 Resource Status (D1:F0)

PCI Device: 1
Address Offset: 126h
Default Value: 0000h
Access: RO
Size: 16 bits

This register reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		Reserved
1	RO 1b	**VC1 Negotiation Pending** 0 = The VC negotiation is complete. 1 = The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as when the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0		Reserved

8.1.55   RCLDECH—Root Complex Link Declaration Enhanced Capability Header (D1:F0)

PCI Device: 1
Address Offset: 140h
Default Value: 00010005h
Access: RO
Size: 32 bits

This capability declares links from this element (PCI Express* x16 Graphics Interface) to other elements of the root complex component to which it belongs. See the PCI Express specification for link/topology declaration requirements.

Bit	Access & Default	Description
31:20	RO 000h	**Pointer to Next Capability:** This is the last capability in the PCI Express* extended capabilities list.
19:16	RO 1h	**Link Declaration Capability Version:** Hardwired to 1 to indicate compliances with the 1.0a version of the PCI Express specification.
15:0	RO 0005h	**Extended Capability ID:** Value of 0005h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.

Note: See corresponding Egress Port Link Declaration Capability registers for diagram of Link Declaration Topology.

8.1.56   ESD—Element Self Description (D1:F0)

PCI Device: 1
Address Offset: 144h
Default Value: 02000100h
Access: RO, R/WO
Size: 32 bits

This register provides information about the root complex element containing this Link Declaration Capability.

Bit	Access & Default	Description
31:24	RO 02h	**Port Number:** This field specifies the port number associated with this element with respect to the component that contains this element. The egress port of the component to provide arbitration to this Root Complex Element uses this port number value.
23:16	R/WO 00h	**Component ID:** This field indicates the physical component that contains this Root Complex Element. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:8	RO 01h	**Number of Link Entries:** This field indicates the number of link entries following the Element Self Description. This field reports 1 (to Egress port only as peer-to-peer capabilities in this topology are not reported).
7:4		Reserved
3:0	RO 0h	**Element Type:** This field indicates the type of the Root Complex Element. 0h = root port.

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8.1.57 LE1D—Link Entry 1 Description (D1:F0)

PCI Device: 1
Address Offset: 150h
Default Value: 00000000h
Access: RO, R/WO
Size: 32 bits

This register provides the First part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 00h	**Target Port Number:** This field specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00h	**Target Component ID:** This field indicates the physical or logical component that is targeted by this link entry. A value of 0 is reserved; Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2		Reserved
1	RO 0b	**Link Type:** This field indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO 0b	**Link Valid:** 0 = Link Entry is not valid and will be ignored. 1 = Link Entry specifies a valid link.

8.1.58 LE1A—Link Entry 1 Address (D1:F0)

PCI Device: 1
Address Offset: 158h
Default Value: 0000000000000000h
Access: R/WO
Size: 64 bits

This register provides the second part of a Link Entry that declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:32		Reserved
31:12	R/WO 0 0000h	**Link Address:** This field indicates memory-mapped base address of the RCRB that is the target element (Egress Port) for this link entry.
11:0		Reserved

8.1.59 PEGSSTS—PCI Express*-G Sequence Status (D1:F0)

PCI Device: 1
Address Offset: 218h
Default Value: 0000000000000FFFh
Access: RO
Size: 64 bits

This register provides PCI Express status reporting that is required by the PCI Express specification.

Bit	Access & Default	Description
63:60		Reserved
59:48	RO 000h	**Next Transmit Sequence Number:** Value of the NXT_TRANS_SEQ counter. This counter represents the transmit Sequence number to be applied to the next TLP to be transmitted onto the Link for the first time.
47:44		Reserved
43:32	RO 000h	**Next Packet Sequence Number:** Packet sequence number to be applied to the next TLP to be transmitted or re-transmitted onto the Link.
31:28		Reserved
27:16	RO 000h	**Next Receive Sequence Number:** This is the sequence number associated with the TLP that is expected to be received next.
15:12		Reserved
11:0	RO FFFh	**Last Acknowledged Sequence Number:** This is the sequence number associated with the last acknowledged TLP.

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9 System Address Map

The MCH supports 4 GB of addressable memory space (see Figure 9-1) and 64 KB+3 bytes of addressable I/O space. A programmable memory address space under the 1-MB region is divided into regions that can be individually controlled with programmable attributes such as disable, read/write, write only, or read only. This section focuses on how the memory space is partitioned and what the separate memory regions are used for. I/O address space has simpler mapping and is explained near the end of this section.

Addressing of memory ranges larger than 4 GB is **not** supported. The HREQ[4:3] FSB pins are decoded to determine whether the access is above or below 4 GB.

The MCH does not support the PCI Dual Address Cycle (DAC) Mechanism, PCI Express 64-bit prefetchable memory transactions, or any other addressing mechanism that allows addressing of greater than 4 GB on either the DMI or PCI Express interface. The MCH does not limit system memory space in hardware. There is no hardware lock to stop someone from inserting more memory than is addressable.

In the following sections, it is assumed that all of the compatibility memory ranges reside on the DMI. The exception to this rule is VGA ranges that may be mapped to PCI Express or DMI. In the absence of more specific references, cycle descriptions referencing PCI should be interpreted as the DMI/PCI, while cycle descriptions referencing PCI Express are related to the PCI Express bus. The MCH does not remap APIC or any other memory spaces above TOLUD (Top of Low Usable DRAM). The TOLUD register is set to the appropriate value by BIOS.

- Device 0
  — EPBAR – Egress port registers. Necessary for setting up VC1 as an isochronous channel using time based weighted round robin arbitration. (4-KB window)
  — MCHBAR – Memory mapped range for internal MCH registers. For example, memory buffer register controls. (16-KB window)
  — PCIEXBAR – Flat memory-mapped address space to access device configuration registers. This mechanism can be used to access PCI configuration space (0h–FFh) and Extended configuration space (100h–FFFh) for PCI Express devices. This enhanced configuration access mechanism is defined in the PCI Express specification. (256-MB window)
  — DMIBAR –This window is used to access registers associated with the MCH/ICH6 (DMI) register memory range. (4-KB window)
  — IFPBAR – Any write to this window will trigger a flush of the MCH's Global Write Buffer to let software guarantee coherency between writes from an isochronous agent and writes from the processor (4-KB window).

- Device 1: Function 0:
  — MBASE1/MLIMIT1 – PCI Express port non-prefetchable memory access window.
  — PMBASE1/PMLIMIT1 – PCI Express port prefetchable memory access window.
  — IOBASE1/IOLIMIT1 – PCI Express port I/O access window.

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The rules for the above programmable ranges are:

- ALL of these ranges MUST be unique and NON-OVERLAPPING. It is the BIOS or system designer's responsibility to limit memory population so that adequate PCI, PCI Express, High BIOS, PCI Express Memory Mapped space, and APIC memory space can be allocated.

- In the case of overlapping ranges with memory, the memory decode will be given priority.

- There are NO Hardware Interlocks to prevent problems in the case of overlapping ranges.

- Accesses to overlapped ranges may produce indeterminate results.

- The only peer-to-peer cycles allowed below the top of memory (register TOLUD) are DMI to PCI Express VGA range writes.

Figure 9-1 shows the system memory address map in a simplified form.

Figure 9-1. System Address Ranges
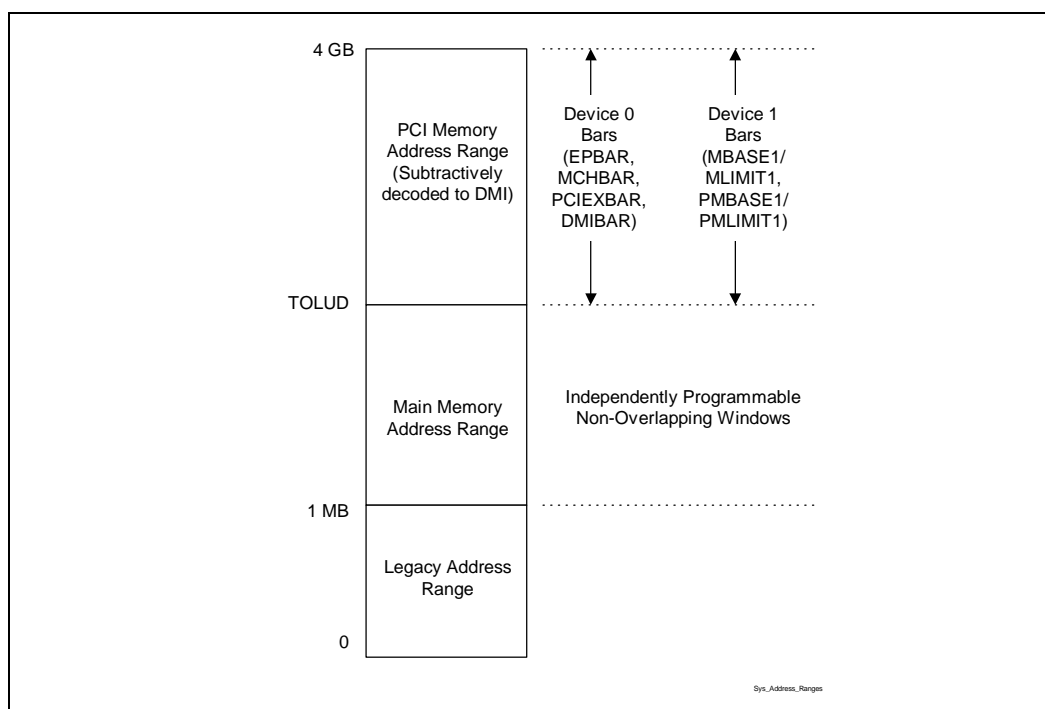
9.1 Legacy Address Range

This area is divided into the following address regions:

- 0 – 640 KB: DOS Area

- 640 – 768 KB: Legacy Video Buffer Area

- 768 – 896 KB in 16-KB sections (total of 8 sections): Expansion Area

- 896 – 960 KB in 16-KB sections (total of 4 sections): Extended System BIOS Area

- 960-KB – 1-MB Memory: System BIOS Area

Figure 9-2. Microsoft MS-DOS* Legacy Address Range

000F_FFFFh	1MB
000F_0000h	System BIOS (Upper) 64KB
000E_FFFFh	960KB
000E_0000h	Extended System BIOS (Lower) 64KB (16KBx4)
000D_FFFFh	896KB
	Expansion Area 128KB (16KBx8)
000C_0000h	
000B_FFFFh	768KB
	Legacy Video Area (SMM Memory) 128KB
000A_0000h	
0009_FFFFh	640KB
	DOS Area
0000_0000h	
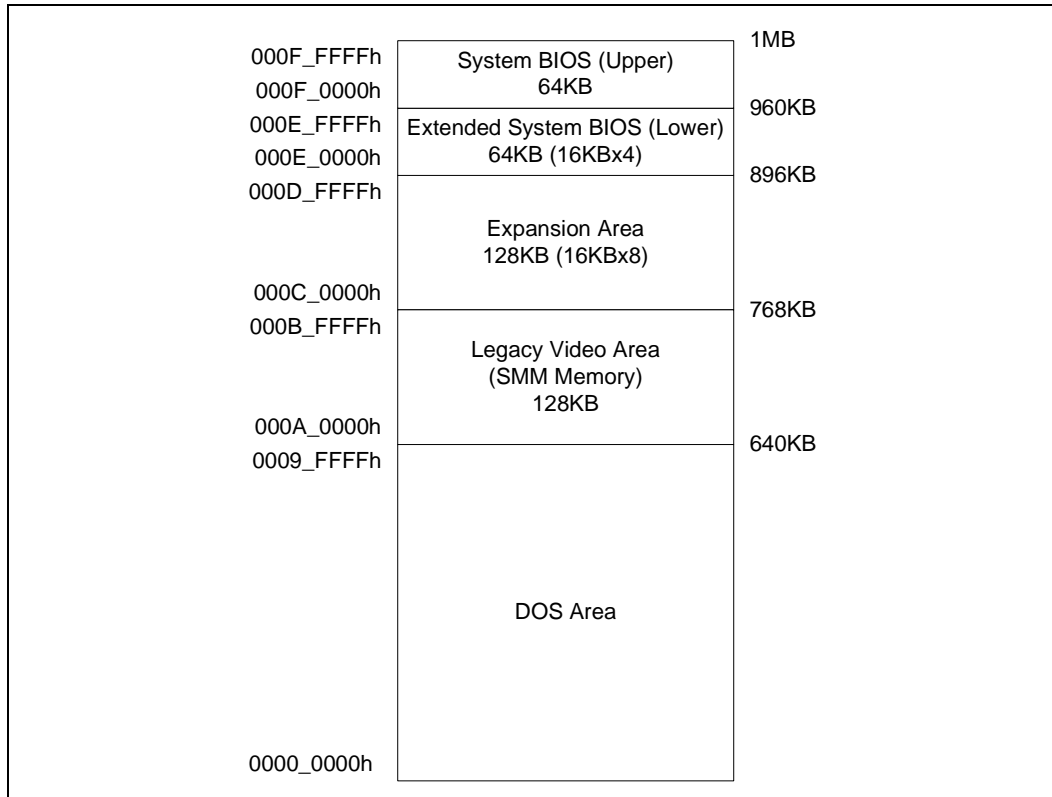
9.1.1   DOS Range (0h – 9_FFFFh)

The DOS area is 640 KB (0000_0000h – 0009_FFFFh) in size and is always mapped to the main memory controlled by the MCH.

9.1.2   Legacy Video Area (A_0000h–B_FFFFh)

The legacy 128-KB VGA memory range, frame buffer, (000A_0000h – 000B_FFFFh) can be mapped to PCI Express and/or to the DMI. The appropriate mapping is programmable. Based on the programming, priority for VGA mapping is constant. The MCH always decodes internally mapped devices first. The MCH always positively decodes internally mapped devices, namely the PCI Express. Subsequent decoding of regions mapped to PCI Express or the DMI depends on the programming. This region is also the default for SMM space.

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Compatible SMRAM Address Range (A_0000h–B_FFFFh)

When compatible SMM space is enabled, SMM-mode processor accesses to this range are routed to physical system DRAM at 000A_0000h–000B_FFFFh. Non-SMM-mode processor accesses to this range are considered to be to the Video Buffer Area as described above. PCI Express and DMI originated cycles to enabled SMM space are not allowed. PCI Express and DMI initiated cycles are attempted as peer cycles, and will master abort on PCI if no external VGA device claims them.

Monochrome Adapter (MDA) Range (B_0000h–B_7FFFh)

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to PCI Express or the DMI (depending on the programming of the on-chip registers). Since the monochrome adapter may be mapped to any one of these devices, the MCH must decode cycles in the MDA range (000B_0000h – 000B_7FFFh) and forward either PCI Express or the DMI. In addition to the memory range B0000h to B7FFFh, the MCH decodes I/O cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh and forwards them to the either PCI Express, and/or the DMI.

9.1.3   Expansion Area (C_0000h–D_FFFFh)

This 128-KB ISA Expansion region (000C_0000h – 000D_FFFFh) is divided into eight, 16-KB segments. Each segment can be assigned one of four read/write states: read only, write only, read/write, or disabled. Typically, these blocks are mapped through the MCH and are subtractively decoded to ISA space. Memory that is disabled is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to main memory.

Table 9-1. Expansion Area Memory Segments

Memory Segments	Attributes	Comments
0C0000h–0C3FFFh	W/R	Add-on BIOS
0C4000h–0C7FFFh	W/R	Add-on BIOS
0C8000h–0CBFFFh	W/R	Add-on BIOS
0CC000h –0CFFFFh	W/R	Add-on BIOS
0D0000h–0D3FFFh	W/R	Add-on BIOS
0D4000h–0D7FFFh	W/R	Add-on BIOS
0D8000h–0DBFFFh	W/R	Add-on BIOS
0DC000h–0DFFFFh	W/R	Add-on BIOS

9.1.4 Extended System BIOS Area (E_0000h–E_FFFFh)

This 64-KB area (000E_0000h–000E_FFFFh) is divided into four, 16-KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to the DMI. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

Non-snooped accesses from PCI Express or DMI to this region are always sent to main memory.

Table 9-2. Extended System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0E0000h–0E3FFFh	W/R	BIOS Extension
0E4000h–0E7FFFh	W/R	BIOS Extension
0E8000h–0EBFFFh	W/R	BIOS Extension
0EC000h–0EFFFFh	W/R	BIOS Extension

9.1.5 System BIOS Area (F_0000h–F_FFFFh)

This area is a single, 64-KB segment (000F_0000h – 000F_FFFFh). This segment can be assigned read and write attributes. It is by default (after reset) read/write disabled and cycles are forwarded to the DMI. By programming the read/write attributes, the MCH can "shadow" BIOS into main memory. When disabled, this segment is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to main memory.

Table 9-3. System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0F0000h–0FFFFFh	WE RE	BIOS Area

9.1.6 Programmable Attribute Map (PAM) Memory Area Details

The 13 sections from 768 KB to 1 MB comprise what is also known as the PAM memory area.

The MCH does not handle IWB (Implicit Write-Back) cycles targeting DMI. Since all memory residing on DMI should be set as non-cacheable, there will normally not be IWB cycles targeting DMI.

However, DMI becomes the default target for processor and DMI originated accesses to disabled segments of the PAM region. If the MTRRs covering the PAM regions are set to WB or RC, it is possible to get IWB cycles targeting DMI. This may occur for DMI-originated cycles to disabled PAM regions.

Note: For example, assume that a particular PAM region is set for "Read Disabled" and the MTRR associated with this region is set to WB. A DMI master generates a memory read targeting the PAM region. A snoop is generated on the FSB and the result is an IWB. Since the PAM region is

"Read Disabled", the default target for the memory read becomes DMI. The IWB associated with this cycle will cause the MCH to hang.

9.2 Main Memory Address Range (1 MB to TOLUD)

This address range extends from 1 MB to the top of physical memory that is permitted to be accessible by the MCH (as programmed by BIOS). All accesses to addresses within this range will be forwarded by the MCH to the main memory unless they fall into the optional TSEG or optional ISA Hole.

The MCH provides a maximum main memory address decode space of 4 GB. The MCH does not remap APIC or PCI Express memory space. This means that as the amount of physical memory populated in the system reaches 4 GB, there will be physical memory that exists, yet non-addressable; therefore, this memory is unusable by the system.

The MCH does not limit main memory address space in hardware.

Figure 9-3. Main Memory Address Range
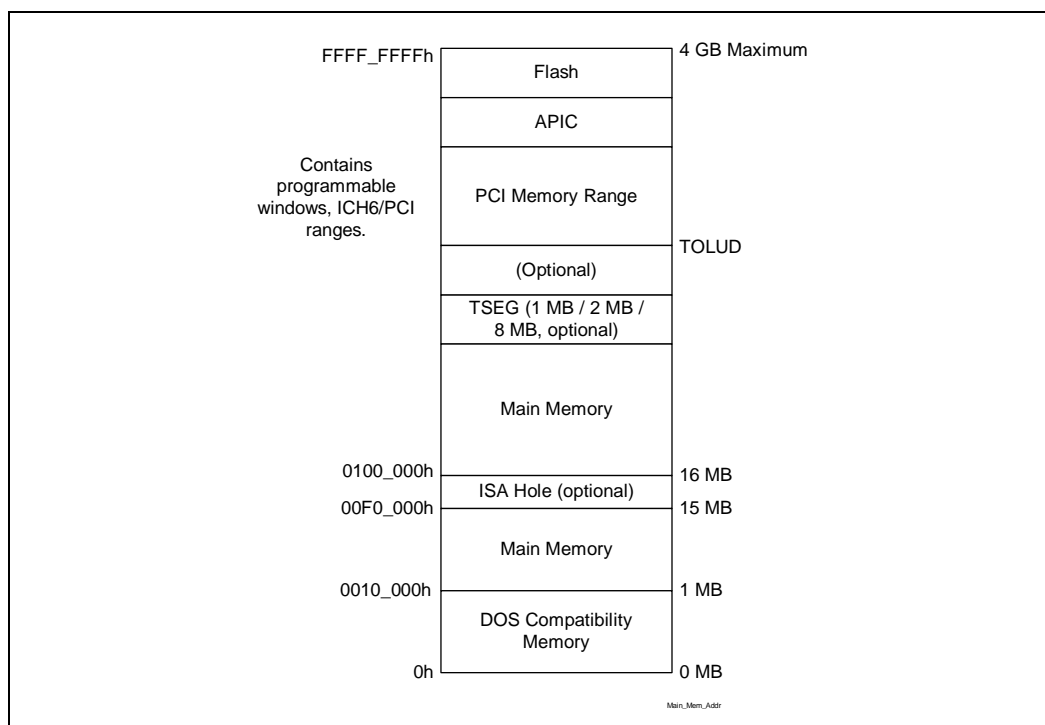
9.2.1 ISA Hole (15 MB–16 MB)

BIOS can create a hole at 15 MB–16 MB. Accesses within this hole are forwarded to the DMI. The range of physical main memory disabled by opening the hole is not remapped to the top of the memory; that physical main memory space is not accessible. This 15 MB–16 MB hole is an optionally enabled ISA hole.

9.2.2   TSEG

TSEG is optionally 1 MB, 2 MB, or 8 MB in size. SMM-mode processor accesses to enabled TSEG access the physical DRAM at the same address. Non-processor originated accesses are not allowed to SMM space. PCI Express and DMI originated cycles to enabled SMM space are handled as invalid cycle type with reads and writes to location 0 and byte enables turned off for writes. When the extended SMRAM space is enabled, processor accesses to the TSEG range without SMM attribute or without WB attribute are also forwarded to memory as invalid accesses. Non-SMM-mode write-back cycles that target TSEG space are completed to main memory for cache coherency. When SMM is enabled, the maximum amount of memory available to the system is equal to the amount of physical main memory minus the value in the TSEG register which is fixed at 1 MB, 2 MB or 8 MB.

9.2.3   Pre-allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< TOLUD) are created for SMM-mode and legacy VGA graphics compatibility. **It is the responsibility of BIOS to properly initialize these regions**. Table 9-4 details the location and attributes of the regions.

Table 9-4. Pre-Allocated Memory Example for 64-MB DRAM and 1-MB TSEG

Memory Segments	Attributes	Comments
0000_0000h – 03DF_FFFFh	R/W	Available system memory 62 MB
03E0_0000h – 03EF_FFFFh	SMM Mode Only - processor reads	TSEG Address Range and Pre-allocated memory
03F0_0000h – 03FF_FFFFh	R/W	Pre-allocated Graphics VGA memory.

9.3   PCI Memory Address Range (TOLUD – 4 GB)

This address range, from the top of physical memory to 4 GB (top of addressable memory space supported by the MCH) is normally mapped via the DMI to PCI.

Note: AGIP Aperture no longer exists with PCI Express.

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Figure 9-4. PCI Memory Address Range
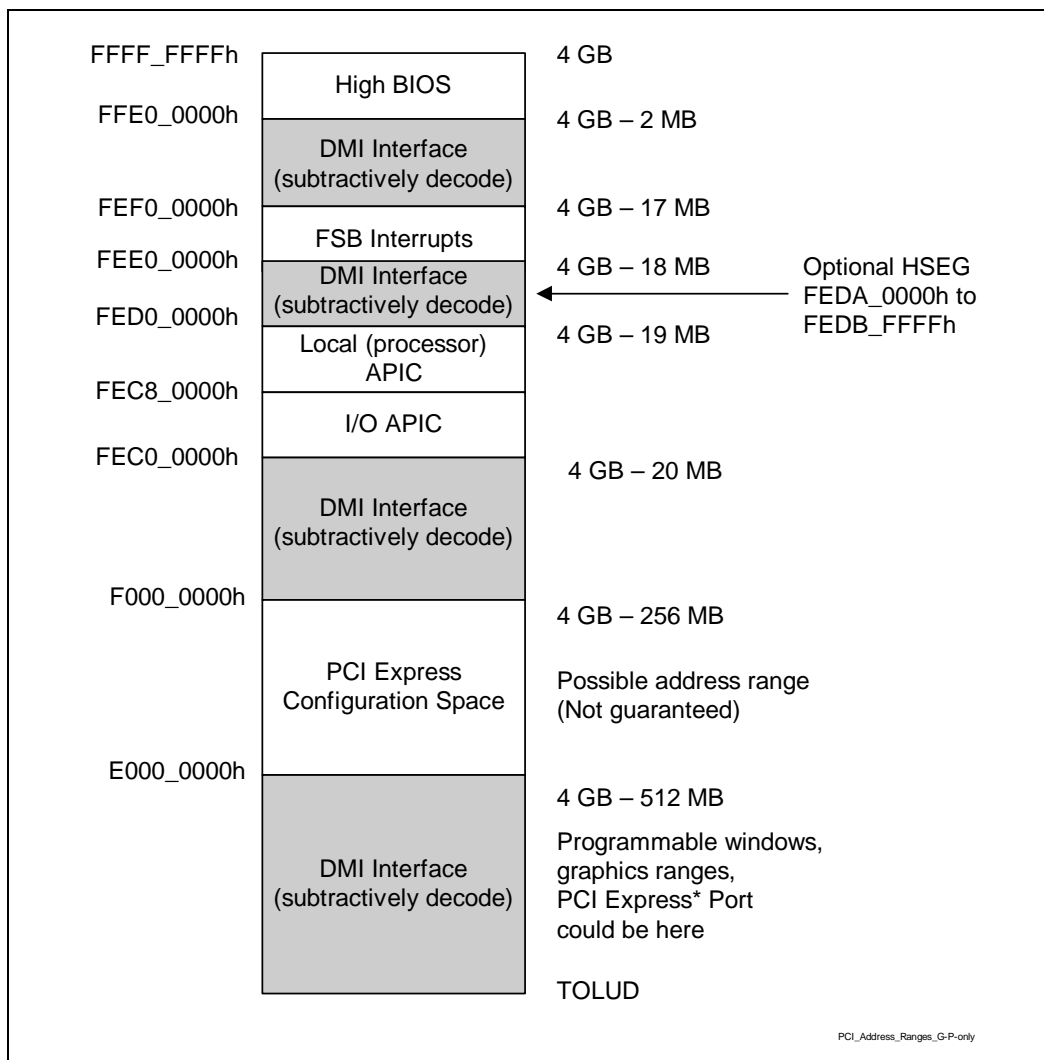
9.3.1   APIC Configuration Space (FEC0_0000h-FECF_FFFFh)

This range is reserved for APIC configuration space. The I/O APIC(s) usually reside in the ICH6 portion of the chipset, but may also exist as stand-alone components.

The IOAPIC spaces are used to communicate with IOAPIC interrupt controllers that may be populated in the system. Since it is difficult to relocate an interrupt controller using plug-and-play software, fixed address decode regions have been allocated for them. Processor accesses to the default IOAPIC region (FEC0_0000h to FEC7_FFFFh) are always forwarded to DMI.

9.3.2 HSEG (FEDA_0000h–FEDB_FFFFh)

This optional segment from FEDA_0000h to FEDB_FFFFh provides a remapping window to SMM memory. It is sometimes called the High SMM memory space. SMM-mode processor accesses to the optionally enabled HSEG are remapped to 000A_0000h – 000B_FFFFh. Non-SMM-mode processor accesses to enabled HSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM-mode write-back cycles that are remapped to SMM space to maintain cache coherency. PCI Express and DMI originated cycles to enabled SMM space are not allowed. Physical main memory behind the HSEG transaction address is not remapped and is not accessible. All cacheline writes with WB attribute or Implicit write backs to the HSEG range are completed to DRAM like an SMM cycle.

9.3.3 FSB Interrupt Memory Space (FEE0_0000–FEEF_FFFF)

The FSB Interrupt space is the address used to deliver interrupts to the FSB. Any device on PCI Express or DMI may issue a memory write to 0FEEx_xxxxh. The MCH will forward this memory write along with the data to the FSB as an Interrupt Message Transaction. The MCH terminates the FSB transaction by providing the response and asserting HTRDY#. This memory write cycle does not go to main memory.

9.3.4 High BIOS Area

The top 2 MB (FFE0_0000h -FFFF_FFFFh) of the PCI memory address range is reserved for system BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The processor begins execution from the High BIOS after reset. This region is mapped to the DMI so that the upper subset of this region aliases to the 16-MB–256-KB range. The actual address space required for the BIOS is less than 2 MB, but the minimum processor MTRR range for this region is 2 MB; thus, that full 2 MB must be considered.

9.3.5 PCI Express* Configuration Address Space

A configuration register defines the base address for the 256-MB block of addresses below top of addressable memory (4 GB) for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. This range will be aligned to a 256-MB boundary. BIOS must assign this address range such that it will not conflict with any other address ranges.

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9.3.6 PCI Express* Graphics Attach

The MCH can be programmed to direct memory accesses to the PCI Express interface when addresses are within either of two programmed ranges specified via registers in the MCH's Device 1 configuration space.

- The first range is controlled via the Memory Base Register (MBASE) and Memory Limit Register (MLIMIT) registers.

- The second range is controlled via the Prefetchable Memory Base (PMBASE) and Prefetchable Memory Limit (PMLIMIT) registers.

The MCH positively decodes memory accesses to PCI Express memory address space as defined by the following equations:

$$\text{Memory\_Base\_Address} \leq \text{Address} \leq \text{Memory\_Limit\_Address}$$

$$\text{Prefetchable\_Memory\_Base\_Address} \leq \text{Address} \leq \text{Prefetchable\_Memory\_Limit\_Address}$$

It is essential to support a separate Prefetchable range to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

Note: The programmable ranges are used to allocate memory address space for any PCI Express devices sitting on PCI Express that require such a window.

The PCICMD1 register can override the routing of memory accesses to PCI Express. In other words, the memory access enable bit must be set in the device 1 PCICMD1 register to enable the memory base/limit and prefetchable base/limit windows.

9.3.7 AGP DRAM Graphics Aperture

Unlike AGP4x, PCI Express has no concept of aperture for PCI Express devices. As a result, there is no need to translate addresses from PCI Express. Therefore, the MCH has no APBASE and APSIZE registers.

9.4 System Management Mode (SMM)

System Management Mode uses main memory for System Management RAM (SMM RAM). The MCH supports: Compatible SMRAM (C_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM. MCH provides three SMRAM options:

- Below 1-MB option that supports compatible SMI handlers.

- Above 1-MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.

- Optional TSEG area of 1 MB, 2 MB, or 8 MB in size.

The above 1-MB solutions require changes to compatible SMRAM handler's code to properly execute above 1 MB.

Note: DMI and PCI Express masters are not allowed to access the SMM space.

9.4.1 SMM Space Definition

SMM space is defined by its **addressed** SMM space and its DRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the processor to access SMM space. DRAM SMM space is defined as the range of physical main memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High, and TSEG. The Compatible and TSEG SMM space is not remapped; therefore, the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped, the addressed and DRAM SMM space are different address ranges. Note that the High DRAM space is the same as the Compatible Transaction Address space. The following table describes three unique address ranges:

- Compatible Transaction Address

- High Transaction Address

- TSEG Transaction Address

SMM Space Enabled	Transaction Address Space	DRAM Space (DRAM)
Compatible (C)	000A_0000h to 000B_FFFFh	000A_0000h to 000B_FFFFh
High (H)	FEDA_0000h to FEDB_FFFFh	000A_0000h to 000B_FFFFh
TSEG (T)	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN

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9.4.2   SMM Space Restrictions

If any of the following conditions are violated, the results of SMM accesses are unpredictable and may cause the system to hang:

- The Compatible SMM space **must not** be set-up as cacheable.

- High or TSEG SMM transaction address space **must not** overlap address space assigned to system main memory, or to any "PCI" devices (including DMI, PCI Express, and graphics devices). This is a BIOS responsibility.

- Both D_OPEN and D_CLOSE capability **must not** be enabled at the same time.

- When TSEG SMM space is enabled, the TSEG space **must not** be reported to the OS as available main memory. This is a BIOS responsibility.

- Any address translated through the GMADR TLB must not target main memory from A_0000-F_FFFF.

9.4.3   SMM Space Combinations

When High SMM is enabled, the Compatible SMM space is effectively disabled. Processor originated accesses to the Compatible SMM space are forwarded to PCI Express if this VGA capability is enabled; otherwise, they are forwarded to the DMI. PCI Express and DMI originated accesses are **never** allowed to access SMM space.

Table 9-5. SMM Space Table

Global Enable G_SMRAME	High Enable H_SMRAM_EN	TSEG Enable TSEG_EN	Compatible (C) Range	High (H) Range	TSEG (T) Range
0	X	X	Disable	Disable	Disable
1	0	0	Enable	Disable	Disable
1	0	1	Enable	Disable	Enable
1	1	0	Disabled	Enable	Disable
1	1	1	Disabled	Enable	Enable

9.4.4 SMM Control Combinations

The G_SMRAME bit provides a global enable for all SMM memory. The D_OPEN bit allows software to write to the SMM ranges without being in SMM mode. BIOS software can use this bit to initialize SMM code at powerup. The D_LCK bit limits the SMM range access to only SMM mode accesses. The D_CLS bit causes SMM data accesses to be forwarded to the DMI or PCI Express. The SMM software can use this bit to write to video memory while running SMM code out of DRAM.

Table 9-6. SMM Control Table

G_SMRAME	D_LCK	D_CLS	D_OPEN	CPU in SMM Mode	SMM Code Access	SMM Data Access
0	x	X	x	x	Disable	Disable
1	0	X	0	0	Disable	Disable
1	0	0	0	1	Enable	Enable
1	0	0	1	x	Enable	Enable
1	0	1	0	1	Enable	Disable
1	0	1	1	x	Invalid	Invalid
1	1	X	x	0	Disable	Disable
1	1	0	x	1	Enable	Enable
1	1	1	x	1	Enable	Disable

9.4.5 SMM Space Decode and Transaction Handling

Only the processor is allowed to access SMM space. PCI Express and DMI originated transactions are not allowed to SMM space.

9.4.6 Processor WB Transaction to an Enabled SMM Address Space

Processor write-back transactions (HREQ1# = 0) to enabled SMM address space must be written to the associated SMM DRAM, even though the space is not open and the transaction is not performed in SMM mode. This ensures SMM space cache coherency when cacheable extended SMM space is used.

9.4.7   SMM Access through GTT TLB

Accesses through GTT TLB address translation to enabled SMM DRAM space are not allowed. Writes will be routed to memory address 0h with byte enables de-asserted and reads will be routed to memory address 0h. If a GTT TLB translated address hits enabled SMM DRAM space, an Invalid Translation Table Entry Flag is reported to BIOS.

PCI Express and DMI originated accesses are **never** allowed to access SMM space directly or through the GTT TLB address translation. If a GTT TLB translated address hits enabled SMM DRAM space, an Invalid Translation Table Entry Flag is reported to BIOS.

PCI Express and DMI write accesses through the graphics memory range set up by BIOS will be snooped. If, when translated, the resulting physical address is to enabled SMM DRAM space, the request will be remapped to address 0h with de-asserted byte enables.

PCI Express and DMI read accesses to the graphics memory range set up by BIOS are not supported; therefore, users/systems will be remapped to address 0h. The read will complete with UR (unsupported request) completion status.

GTT fetches are always decoded (at fetch time) to ensure they are not in SMM (actually, anything above base of TSEG or 640 KB–1 MB). Thus, they will be invalid and go to address 0h. This is not specific to PCI Express or DMI; it applies to the processor. Also, since the graphics memory range snoop would not be directly to SMM space, there would not be a writeback to SMM. In fact, the writeback would also be invalid (because it uses the same translation) and goes to address 0h.

9.4.8   Memory Shadowing

Any block of memory that can be designated as "read only" or "write only" can be "shadowed" into MCH main memory. Typically, this is done to allow ROM code to execute more rapidly out of main DRAM memory. ROM is used as read-only during the copy process while main DRAM memory at the same time is designated write-only. After copying, the main DRAM memory is designated read-only so that ROM is shadowed. Processor bus transactions are routed accordingly.

9.4.9   I/O Address Space

The MCH does not support the existence of any other I/O devices beside itself on the processor bus. The MCH generates either DMI or PCI Express bus cycles for all processor I/O accesses that it does not claim. Within the host bridge, the MCH contains two internal registers in the processor I/O space. These locations are used to implement a configuration space access mechanism.

The processor allows 64 KB+3 bytes to be addressed within the I/O space. The MCH propagates the processor I/O address without any translation on to the destination bus; therefore, providing addressability for 64 KB+3 byte locations. Note that the upper 3 locations can be accessed only during I/O address wrap-around when processor bus HA16# address signal is asserted. HA16# is asserted on the processor bus when an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. HA16# is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the DMI bus unless they fall within the PCI Express I/O address range as defined by the mechanisms explained below. I/O writes are **not** posted. Memory writes to the ICH6 or PCI Express are posted.

The MCH responds to I/O cycles initiated on PCI Express or DMI with a UR status. Upstream I/O cycles and configuration cycles should never occur. If one does occur, the request will route as a read to memory address 0h so a completion is naturally generated (whether the original request was a read or write). The transaction will complete with a UR completion status.

For Pentium 4 processors, I/O reads that lie within 8-byte boundaries but cross 4-byte boundaries are issued from the processor as 1 transaction. The MCH will break this into 2 separate transactions. This has not been done on previous chipsets. I/O writes that lie within 8-byte boundaries but cross 4-byte boundaries are assumed to be split into 2 transactions by the processor.

9.4.10   PCI Express* I/O Address Mapping

The MCH can be programmed to direct non-memory (I/O) accesses to the PCI Express bus interface when processor-initiated I/O cycle addresses are within the PCI Express I/O address range.

9.4.11   MCH Decode Rules and Cross-Bridge Address Mapping

The following are MCH decode rules and cross-bridge address mapping used in this chipset:

- VGAA = 000A_0000h – 000A_FFFFh

- MDA = 000B_0000h – 000B_7FFFh

- VGAB = 000B_8000h – 000B_FFFFh

- MAINMEM = 0100_0000 to TOLUD

9.4.12   Legacy VGA and I/O Range Decode Rules

The legacy 128-KB VGA memory range 000A_0000h-000B_FFFFh can be mapped to PCI Express (Device 1), and/or to the DMI depending on BIOS programming. Priority for VGA mapping is constant in that the MCH always decodes internally mapped devices first. The MCH always positively decodes internally mapped devices, namely the PCI Express.

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10 Functional Description

This chapter describes the MCH interfaces and major functional units.

10.1 Host Interface

The MCH supports the Pentium 4 processor subset of the Enhanced Mode Scaleable Bus. The cache line size is 64 bytes. Source synchronous transfer is used for the address and data signals. The address signals are double pumped, and a new address can be generated every other bus clock. At 200 MHz bus clock, the address signals run at 400 MT/s for a maximum address queue rate of 66/100 million addresses/sec. The data is quad pumped and an entire 64 byte cache line can be transferred in two bus clocks. At 200 MHz bus clock, the data signals run at 800 MT/s for a maximum bandwidth of 6.4 GB/s.

The FSB interface supports up to 12 simultaneous outstanding transactions. The MCH supports only one outstanding deferred transaction on the FSB.

10.1.1 FSB GTL+ Termination

The MCH integrates GTL+ termination resistors on die. Also, approximately
2.8 pf (fast) – 3.3 pf (slow) per pad of on die capacitance will be implemented to provide better FSB electrical performance.

10.1.2 FSB Dynamic Bus Inversion

The MCH supports Dynamic Bus Inversion (DBI) when driving and when receiving data from the processor. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the worst-case power consumption of the MCH. HDINV[3:0]# indicate if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase:

HDINV[3:0]#	Data Bits
HDINV0#	HD[15:0]#
HDINV1#	HD[31:16]#
HDINV2#	HD[47:32]#
HDINV3#	HD[63:48]#

When the processor or the MCH drives data, each 16-bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus, the corresponding HDINV# signal will be asserted and the data will be inverted prior to being driven on the bus. When the processor or the MCH receives data, it monitors HDINV[3:0]# to determine if the corresponding data segment should be inverted.

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10.1.3   APIC Cluster Mode Support

This is required for backwards compatibility with existing software, including various operating systems. As one example, beginning with Microsoft Windows 2000 there is a mode (boot.ini) that allows an end user to enable the use of cluster addressing support of the APIC.

The MCH supports three types of interrupt re-direction:

- Physical
- Flat-Logical
- Clustered-Logical

10.2   System Memory Controller

This section describes the MCH system memory interface for DDR2 memory. The MCH supports DDR2 memory and either one or two DIMMs per channel.

10.2.1   Memory Organization Modes

The system memory controller supports two styles of memory organization (Interleaved and Asymmetric). Rules for populating DIMM slots are included in this chapter.

Interleaved Mode

This mode provides maximum performance on real applications. Addresses are ping-ponged between the channels, and the switch happens after each cache line (64 byte boundary). If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are guaranteed to be on opposite channels. The drawbacks of Interleaved Mode are that the system designer must populate both channels of memory such that they have equal capacity, but the technology and device width may vary from one channel to the other. Refer to Figure 10-1 for further clarification.

Asymmetric Mode

This mode trades performance for system design flexibility. Unlike the previous mode, addresses start in channel A and stay there until the end of the highest rank in channel A; then, addresses continue from the bottom of channel B to the top. Real world applications are unlikely to make requests that alternate between addresses that sit on opposite channels with this memory organization, so in most cases, bandwidth will be limited to that of a single channel. The system designer is free to populate or not to populate any rank on either channel, including either degenerate single channel case. Refer to Figure 10-1 for further clarification.

Figure 10-1. System Memory Styles
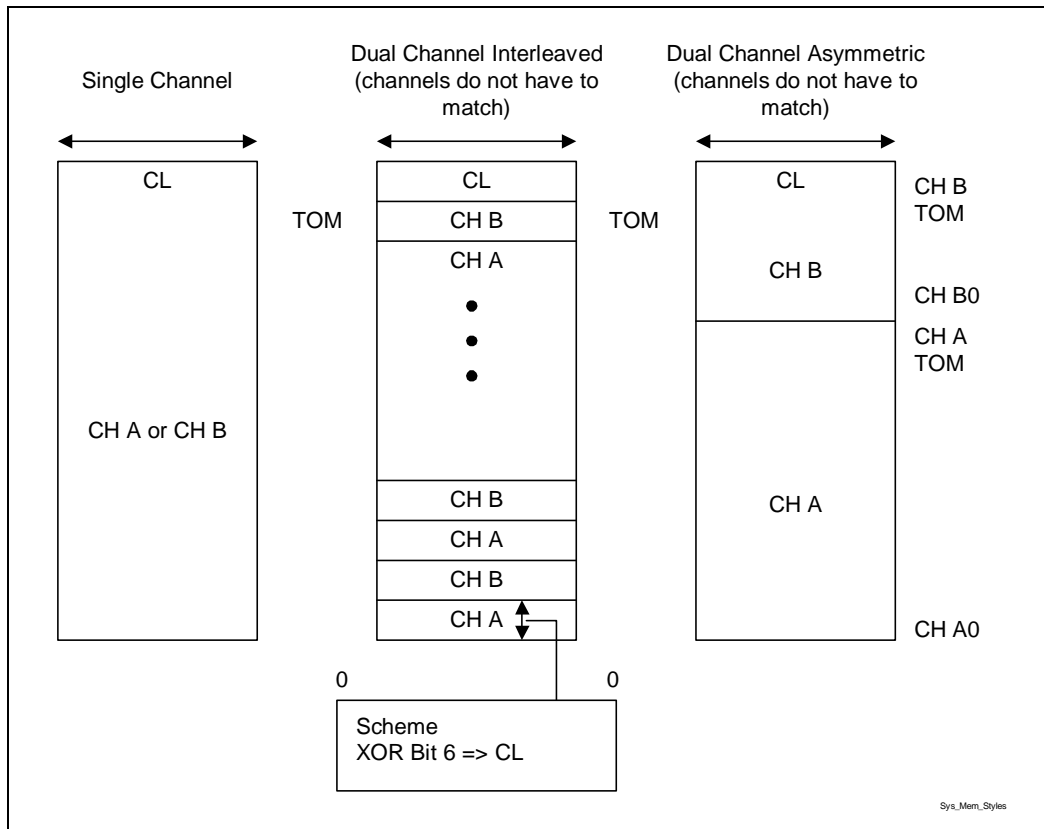
Table 10-1. Sample System Memory Organization with Interleaved Channels

Rank	Channel A population	Cumulative top address in Channel A	Channel B population	Cumulative top address in Channel B
3	0 MB	2560 MB	0 MB	2560 MB
2	256 MB	2560 MB	256 MB	2560 MB
1	512 MB	2048 MB	512 MB	2048 MB
0	512 MB	1024 MB	512 MB	1024 MB

Table 10-2. Sample System Memory Organization with Asymmetric Channels

Rank	Channel A population	Cumulative top address in Channel A	Channel B population	Cumulative top address in Channel B
3	0 MB	1280 MB	0 MB	2560 MB
2	256 MB	1280 MB	256 MB	2560 MB
1	512 MB	1024 MB	512 MB	2304 MB
0	512 MB	512 MB	512 MB	1792 MB

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10.3   System Memory Configuration Register Overview

The configuration registers located in the PCI configuration space of the MCH control the system memory operation. Following is a brief description of configuration registers.

- **DRAM Rank Boundary (CxDRBy):** The x represents a channel, either A (where x = 0) or B (where x = 1). The y represents a rank, 0 through 3. DRB registers define the upper addresses for a rank of DRAM devices in a channel. When the MCH is configured in asymmetric mode, each register represents a single rank. When the MCH is configured in a dual interleaved mode, each register represents a pair of corresponding ranks in opposing channels. There are 4 DRB registers for each channel.

- **DRAM Rank Architecture (CxDRAy):** The x represents a channel, either A (where x = 0) or B (where x = 1). The y represents a rank, 0 through 3. DRA registers specify the architecture features of each rank of devices in a channel. The only architecture feature specified is page size. When the MCH is configured in asymmetric mode, each DRA represents a single rank in a single channel. When the MCH is configured in a dual-channel lock-step or interleaved mode, each DRA represents a pair of corresponding ranks in opposing channels. There are 4 DRA registers per channel. Each requires only 3 bits, so there are two DRAs packed into a byte.

- **Clock Configuration (CLKCFG):** Specifies DRAM frequency. The same clock frequency will be driven to all DIMMs.

- **DRAM Timing (CxDRTy):** The x represents a channel, A (where x = 0) or B (where x = 1). A second register for a channel is differentiated by y, A or B. The DRT registers define the timing parameters for all devices in a channel. The BIOS programs this register with "least common denominator" values after reading the SPD registers of each DIMM in the channel.

- **DRAM Control (CxDRCy):** The x represents a channel, A (where x = 0) or B (where x = 1). A second register for a channel is differentiated by y, A or B. DRAM refresh mode, rate, and other controls are selected here.

10.3.1   DRAM Technologies and Organization

All standard 256-Mb, 512-Mb, and 1-Gb technologies and addressing are supported for x16 and x8 devices.

- All supported DDR2 devices have 4 or 8 banks.

- The MCH supports various page sizes. Page size is individually selected for every rank.

- 4 KB, 8 KB, and 16 KB for asymmetric, interleaved, or single channel modes.

- The DRAM sub-system supports single or dual channels, 64b wide per channel for non-ECC and 72b wide per channel with ECC.

- There can be a maximum of 4 ranks populated (2 Double Sided DIMMs) per channel.

- Mixed mode Double Sided DIMMs (x8 and x16 on the same DIMM) are not supported

- By using 1-Gb technology, the largest memory capacity is 8 GB

  32M rows/bank * 4 banks/device * 8 columns * 8 devices/rank * 4 ranks/channel * 2 channel * 1b/(row*column) * 1G/1024M * 1B/8b = 8 GB.

  Though it is possible to put 8 GB in system by stuffing both channels this way, the MCH is still limited to 4 GB of addressable space due to the number of address pins on the FSB.

- By using 256Mb technology, the smallest memory capacity is 128 MB
  (4M rows/bank * 4banks/device * 16 columns * 4 devices/rank * 1 rank * 1B/8b =128 MB)

10.3.1.1   Rules for Populating DIMM Slots

- In all modes, the frequency of system memory will be the lowest frequency of all DIMMs in the system, as determined through the SPD registers on the DIMMs.

- In the Single Channel mode, any DIMM slot within the channel may be populated in any order. Either channel may be used. To save power, do not populate the unused channel.

- In Dual Channel Asymmetric mode, any DIMM slot may be populated in any order.

- In Dual Channel Interleaved mode, any DIMM slot may be populated in any order, but the total memory in each channel must be the same.

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10.3.1.2   System Memory Supported Configurations

The MCH supports the 256-Mbit, 512-Mbit and 1-Gbit technology-based DIMMs from
Table 10-3.

Table 10-3. DDR2 DIMM Supported Configurations

Technology	Configuration	# of Row Address Bits	# of Column Address Bits	# of Bank Address Bits	Page Size	Rank Size
256 Mbit	16M X 16	13	9	2	4K	128 MB
256 Mbit	32M X 8	13	10	2	8K	256 MB
512 Mbit	32M X 16	13	10	2	8K	256 MB
512 Mbit	64M X 8	13	11	2	16K	512 MB
512 Mbit	64M X 8	14	10	2	8K	512 MB
1 Gbit	64M X 16	14	10	2	8K	512 MB
1 Gbit	128M X 8	14	11	2	16K	1 GB
1 Gbit	64M X 16	13	10	3	8K	512 MB
1 Gbit	128M X 8	14	10	3	8K	1 GB

10.3.1.3   Main Memory DRAM Address Translation and Decoding

Table 10-4 and Table 10-5 specify the host interface to memory interface address multiplex for the
MCH. Refer to the details of the various DIMM configurations as described in Table 10-3. The
address lines specified in the column header refer to the host (processor) address lines.

Table 10-4. DRAM Address Translation (Single Channel/Dual Asymmetric Mode)

Tech	Banks	Page Size	Rank Size	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3
256 Mb x16	4i	4 KB	128 MB						r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	r12	b0	b1	c8	c7	c6	c5	c4	c3	c2	c1	c0
256 Mb x8	4i	8 KB	256 MB					r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
512 Mb x16	4i	8 KB	256 MB					r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
512 Mb x8	4i	16 KB	512 MB				r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	c11	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
512 Mb x16	4i	8 KB	256 MB					r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
512 Mb x8	4i	8 KB	512 MB				r13	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
1 Gb x16	4i	8 KB	512 MB				r13	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
1 Gb x8	4i	16 KB	1 GB			r13	r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	c11	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
1 Gb x16	8i	8 KB	512 MB					r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	b2	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0
1 Gb x8	8i	8 KB	1 GB			r13	r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	b2	c9	c8	c7	c6	c5	c4	c3	c2	c1	c0

NOTES:
1. b – 'bank' select bit
2. c – 'column' address bit
3. r – 'row' address bit

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Table 10-5. DRAM Address Translation (Dual Channel Symmetric Mode)

Tech	Banks	Page Size	Rank Size	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3
256 Mb x16	4i	4 KB	128 MB					r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	r12	b0	b1	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
256 Mb x8	4i	8 KB	256 MB				r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
512 Mb x16	4i	8 KB	256 MB				r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
512 Mb x8	4i	16 KB	512 MB			r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	c11	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
512 Mb x16	4i	4 KB	256 MB				r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
512 Mb x8	4i	8 KB	512 MB			r13	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
1 Gb x16	4i	8 KB	512 MB			r13	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	r11	b1	b0	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
1 Gb x8	4i	16 KB	1 GB		r13	r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	c11	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
1 Gb x16	8i	4 KB	512 MB			r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	b2	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0
1 Gb x8	8i	8 KB	1 GB		r13	r11	r12	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0	b0	b1	b2	c9	c8	c7	c6	c5	c4	c3	h	c2	c1	c0

NOTES:
1. b – 'bank' select bit
2. c – 'column' address bit
3. h – channel select bit
4. r – 'row' address bit

10.3.2 DRAM Clock Generation

The MCH generates three differential clock pairs for every supported DIMM. There are a total of 6 clock pairs driven directly by the MCH to 2 DIMMs per channel.

10.3.3 Suspend to RAM and Resume

When entering the Suspend-to-RAM (STR) state, the SDRAM controller will flush pending cycles and then enter all SDRAM rows into self refresh. In STR, the CKE signals remain LOW so the SDRAM devices will perform self-refresh.

10.3.4 DDR2 On-Die Termination

On-die termination (ODT) is a feature that allows a DRAM to turn on/off internal termination resistance for each DQ, DM, DQS, and DQS# signal for x8 and x16 configurations via the ODT control signals. The ODT feature is designed to improve signal integrity of the memory channel by allowing the termination resistance for the DQ, DM, DQS, and DQS# signals to be located inside the DRAM devices themselves, instead of on the motherboard. The MCH drives out the required ODT signals, based on memory configuration and which rank is being written to or read from, to the DRAM devices on a targeted DIMM rank to enable or disable their termination resistance.

10.3.5 DDR2 Off-Chip Driver Impedance Calibration

The OCD impedance adjustment mode allows the MCH to measure and adjust the pull-up and pull-down strength of the DRAM devices. It uses a series of EMRS commands to guide the DRAM through measurement and calibration cycles. This feature is described in more detail in the JEDEC DDR2 device specification.

The algorithm and sequence of the adjustment cycles is handled by software. The MCH adjusts the DRAM driver impedance by issuing OCD commands to the DIMM and looking at the analog voltage on the DQ lines.

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10.4   PCI Express*

Refer to Chapter 1 for a list of PCI Express features, and the PCI Express specification for further details.

The MCH is part of a PCI Express root complex. This means it connects a host processor/memory subsystem to a PCI Express hierarchy.

The PCI Express architecture is specified in layers. Compatibility with the PCI addressing model (a load-store architecture with a flat address space) is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The initial speed of 1.25 GHz (250 MHz internally) results in 2.5 Gb/s/direction that provides a 250 MB/s communications channel in each direction (500 MB/s total) that is close to twice the data rate of classic PCI per lane.

Note: The PCI Express graphics port will operate in x1 mode if a non-graphics card is plugged in.

10.4.1   Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions (such as read and write as well as certain types of events). The Transaction Layer also manages flow control of TLPs.

Note: If the MCH receives two back-to-back malformed packets, the second malformed packet is not trapped or logged. The MCH will not log or identify the second malformed packet. However, the 1st malformed TLP is logged, and is considered a Fatal Error. Link behavior is not guaranteed at that point whether a 2nd malformed TLP is detected or not.

10.4.2   Data Link Layer

The middle layer in the PCI Express stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

10.4.3   Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry.

10.5   Power Management

Power Management capabilities of the MCH include the following:

- ACPI 1.0b support

- ACPI S0, S3, S4, S5, C0, C1, C2, C3, C4

- Enhanced power management state transitions for increasing time the processor spends in low power states

- Graphics Adapter States: D0, D3.

- PCI Express Link States: L0, L0s, L1, L2/L3 Ready, L3

- PM_THRMTRIP# output

- Conditional memory Self-Refresh during C2, C3, and C4 states

10.6   Clocking

The MCH has PLLs to provide the internal clocks.

- Host PLL – This PLL generates the main core clocks in the host clock domain. The host PLL is used to generate memory and internal graphics core clocks. It uses the Host clock (HCLKIN) as a reference.

- PCI Express PLL – This PLL generates all PCI Express related clocks, including the Direct Media Interface that connects to the ICH6. This PLL uses the 100 MHz (GCLKIN) as a reference.

Figure 10-2 illustrates the various clocks in the platform.

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Figure 10-2. System Clocking Example

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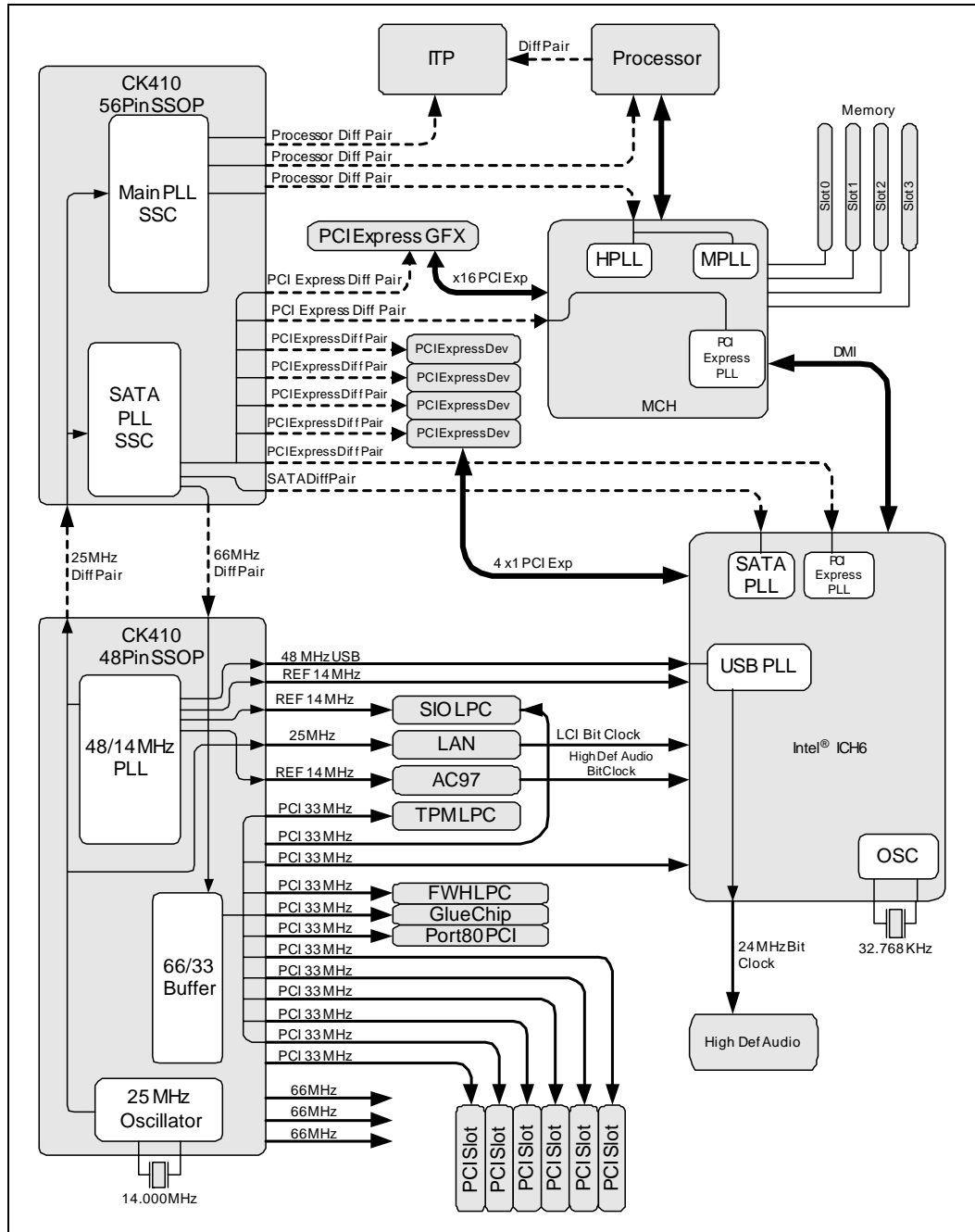
11 Electrical Characteristics

This chapter contains the MCH absolute maximum electrical ratings, power dissipation values, and DC characteristics.

11.1 Absolute Maximum Ratings

Table 11-1 lists the MCH's maximum environmental stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. Functional operating parameters are listed in the DC tables.

Warning: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operating beyond the "operating conditions" is not recommended and extended exposure beyond "operating conditions" may affect reliability.

Table 11-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
$T_{storage}$	Storage Temperature	−55	150	°C	1
MCH Core					
VCC	1.5 V Core Supply Voltage with respect to V_{SS}	−0.3	1.65	V	
Host Interface (800 MHz)					
VTT	1.2 V System Bus Input Voltage with respect to V_{SS}	−0.3	1.65	V	
VCCA_HPLL	1.5 V Host PLL Analog Supply Voltage with respect to V_{SS}	−0.3	1.65	V	
DDR2 Interface (400 MHz / 533 MHz)					
VCCSM (DDR2)	1.8 V DDR2 System Memory Supply Voltage with Respect to V_{SS}	−0.3	4.0	V	
VCCA_SMPLL (DDR2)	1.5 V System Memory PLL Analog Supply Voltage with respect to V_{SS}	−0.3	1.65	V	
PCI Express* / DMI Interface					
VCC_EXP	1.5 V PCI Express* and DMI Supply Voltage with respect to V_{SS}	−0.3	1.65	V	
VCCA_EXPPLL	1.5 V PCI Express PLL Analog Supply Voltage with respect to V_{SS}	−0.3	1.65	V	
CMOS Interface					
VCC2	2.5 V CMOS Supply Voltage with respect to V_{SS}	−0.3	2.65	V	

NOTES:
1. Possible damage to the MCH may occur if the MCH temperature exceeds 150 °C. Intel does not guarantee functionality for parts that have exceeded temperatures above 150 °C due to specification violation.

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11.2 Power Characteristics

Table 11-2. Non-Memory Power Characteristics

Symbol	Parameter	Signal Names	Min	Typ	Max	Unit	Notes
I$_{VTT}$	1.2 V System Bus Supply Bus Current	VTT	—	—	1.0	A	1, 4
I$_{VCC}$	1.5 V Core Supply Current (Integrated)	VCC	—	—	9.7	A	2,3,4
I$_{VCC}$	1.5 V Core Supply Current (Discrete)	VCC	—	—	7.7	A	2,3,4
I$_{VCC\_EXP}$	1.5 V PCI Express* and DMI Supply Current	VCC_EXP	—	—	1.4	A	
I$_{VCC2}$	2.5 V CMOS Supply Current	VCC2	—	—	2	mA	
I$_{VCCA\_EXPPLL}$	1.5 V PCI Express and DMI PLL Analog Supply Current	VCCA_EXPPLL	—	—	45	mA	
I$_{VCCA\_HPLL}$	1.5 V Host PLL Supply Current	VCCA_HPLL	—	—	45	mA	

NOTES:
1. Estimate is only for max current coming through the chipset's supply balls.
2. Rail includes PLL current.
3. Includes Worst case Leakage.
4. Calculated for highest frequencies.

Table 11-3. DDR2 Power Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
I$_{VCCSM}$ (DDR2)	DDR2 System Memory Interface (1.8 V) Supply Current	—	4.7	A	
I$_{SUS\_VCCSM}$ (DDR2)	DDR2 System Memory Interface (1.8 V) **Standby** Supply Current	—	25	mA	
I$_{SMVREF}$ (DDR2)	DDR2 System Memory Interface Reference Voltage (0.90 V) Supply Current	—	10	µA	
I$_{SUS\_SMVREF}$ (DDR2)	DDR2 System Memory Interface Reference Voltage (0.90 V) **Standby** Supply Current	—	10	µA	
I$_{TTRC}$ (DDR2)	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Supply Current	—	32	mA	
I$_{SUS\_TTRC}$ (DDR2)	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) **Standby** Supply Current	—	0	µA	
I$_{VCCA\_SMPLL}$ (DDR2)	System Memory PLL Analog (1.5 V) Supply Current	—	—	—	

11.3   Signal Groups

The signal description includes the type of buffer used for the particular signal:

GTL+   Open Drain GTL+ interface signal. Refer to the *GTL+ I/O Specification* for complete details. The MCH integrates most GTL+ termination resistors.

DDR2   DDR2 System Memory (1.8 V CMOS buffers)

PCI Express* PCI Express Interface Signals. These signals are compatible with the *PCI Express Interface Specification 1.0a* signaling environment AC specifications. The buffers are **not** 3.3V tolerant.

Analog   Analog signal interface.

Ref   Voltage reference signal.

HVCMOS   2.5 V tolerant high voltage CMOS buffers.

SSTL-1.8   1.8 V tolerant stub series termination logic.

Table 11-4. Signal Groups

Signal Group	Signal Type	Signals	Notes
Host Interface Signal Groups			
(a)	GTL+ Input/Outputs	HADS#, HBNR#, HBREQ0#, HDBSY#, HDRDY#, HDINV[3:0]#, HA[31:3]#, HADSTB[1:0]#, HD[63:0], HDSTBP[3:0]#, HDSTBN[3:0]#, HHIT#, HHITM#, HREQ[4:0]#, HLOCK#	
(b)	GTL+ Common Clock Outputs	HBPRI#, HCPURST#, HDEFER#, HTRDY#, HRS[2:0]#, HDPWR#, HEDRDY#	
(c)	GTL+ Asynchronous Input	BSEL[2:0], HPCREQ#	
(d)	Analog Host I/F Ref & Comp. Signals	HVREF, HSWING HRCOMP, HSCOMP	
PCI Express* Interface Signal Groups			
(e)	PCI Express* Input	**PCI Express Interface:** EXP_RXN(15:0), EXP_RXP(15:0),	
(f)	PCI Express Output	**PCI Express Interface:** EXP_TXN(15:0), EXP_TXP(15:0)	
(g)	Analog PCI Express I/F Compensation Signals	EXP_COMP0 EXP_COMPI	

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Signal Group	Signal Type	Signals	Notes
DDR2 Interface Signal Groups			
(k)	SSTL – 1.8 DDR2 CMOS I/O	SDQ_A[63:0]#, SDQ_B[63:0]#, SDQS_A[7:0], SDQS_A[7:0]#, SDQS_B[7:0]#, SDQS_B[7:0]#	
(l)	SSTL – 1.8 DDR2 CMOS Output	SDM_A[7:0], SDM_B[7:0], SMA[13:0], SMA_B[13:0] SBS_A[2:0], SBS_B[2:0] SRAS_A#, SRAS_B#, SCAS_A#, SCAS_B#, SWE_A#, SWE_B#, SODT_A[3:0], SODT_B[3:0], SCKE_A[3:0], SCKE_B[3:0], SCS_A[3:0]#, SCS_B[3:0]#, SCLK_A[5:0], SCLK_A[5:0]#, SCLK_B[5:0], SCLK_B[5:0]#	
(m)	DDR2 Reference Voltage	SMVREF[1:0] (DDR2)	
Clocks, Reset, and Miscellaneous Signal Groups			
(n)	HVCMOS Input	EXTTS#	
(n1)	Miscellaneous Inputs	RSTIN#, PWROK	
(0)	Low Voltage Diff. Clock Input	HCLKN, HCLKP, DREFCLKP, DREFCLKN, GCLKP, GCLKN	
(p)	HVCMOS I/O	DDC_CLK, DDC_DATA	
I/O Buffer Supply Voltages			
(q)	1.2 V System Bus Input Supply Voltage	VTT	
(r)	1.5 V PCI Express Supply Voltages	VCC_EXP	
(t)	1.8 V DDR2 Supply Voltage	VCCSM (DDR2)	
(v)	1.5 V DDR2 PLL Analog Supply Voltage	VCCA_SMPLL (DDR2)	
(w)	1.5 V MCH Core Supply Voltage	VCC	
(x)	2.5 V CMOS Supply Voltage	VCC2	
(z)	PLL Analog Supply Voltages	VCCA_HPLL, VCCA_EXPPLL	

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11.4 General DC Characteristics

Table 11-5. DC Characteristics

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes[3]
I/O Buffer Supply Voltage (AC noise not included)							
VCCSM (DDR2)	(t)	DDR2 I/O Supply Voltage	1.7	1.8	1.9	V	
VCCA_SMPLL (DDR2)	(v)	DDR2 I/O PLL Analog Supply Voltage	1.425	1.5	1.575	V	
VCC_EXP	(r)	PCI Express* Supply Voltage	1.425	1.5	1.575	V	
VTT	(q)	System Bus Input Supply Voltage	1.09	1.2	1.26	V	
VCC	(w)	MCH Core Supply Voltage	1.425	1.5	1.575	V	
VCC2	(x)	CMOS Supply Voltage	2.375	2.5	2.625	V	
VCCA_HPLL, VCCA_EXPPLL	(z)	Various PLL's Analog Supply Voltages	1.425	1.5	1.575	V	
Reference Voltages							
HVREF	(d)	Host Address, Data, and Common Clock Signal Reference Voltage	$2/3 \times V_{TT} - 2\%$	$2/3 \times V_{TT}$	$2/3 \times V_{TT} + 2\%$	V	
HSWING	(d)	Host Compensation Reference Voltage	$1/4 \times V_{TT} - 2\%$	$1/4 \times VTT$	$1/4 \times VTT + 2\%$	V	
SMVREF (DDR2)	(m)	DDR2 Reference Voltage	$0.49 \times$ VCCSM (DDR2)	$0.50 \times$ VCCSM (DDR2)	$0.51 \times$ VCCSM (DDR2)	V	
Host Interface							
V_{IL_H}	(a, c)	Host GTL+ Input Low Voltage	−0.10	0	$(2/3 \times V_{TT}) - 0.1$	V	
V_{IH_H}	(a, c)	Host GTL+ Input High Voltage	$(2/3 \times V_{TT}) + 0.1$	V_{TT}	$V_{TT} + 0.1$	V	
V_{OL_H}	(a, b)	Host GTL+ Output Low Voltage	—	—	$(0.25 \times V_{TT}) + 0.1$	V	
V_{OH_H}	(a, b)	Host GTL+ Output High Voltage	$V_{TT} - 0.1$	—	V_{TT}	V	
I_{OL_H}	(a, b)	Host GTL+ Output Low Current	—	—	$VTT_{max} / (1-0.25)Rtt_{min}$	mA	$Rtt_{min} = 54\ \Omega$
I_{LEAK_H}	(a, c)	Host GTL+ Input Leakage Current	—	—	20	µA	$V_{OL} < Vpad < V_{TT}$

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Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes[3]
C_{PAD}	(a, c)	Host GTL+ Input Capacitance	2	—	3.5	pF	
C_{PCKG}	(a, c)	Host GTL+ Input Capacitance (common clock)	0.90	—	2.5	pF	
DDR2 Interface							
$V_{IL(DC)}$ (DDR2)	(k)	DDR2 Input Low Voltage	—	—	SMVREF (DDR2) − 0.125	V	
$V_{IH(DC)}$ (DDR2)	(k)	DDR2 Input High Voltage	SMVREF (DDR2) + 0.125	—	—	V	
$V_{IL(AC)}$ (DDR2)	(k)	DDR2 Input Low Voltage	—	—	SMVREF (DDR2) − 0.250	V	
$V_{IH(AC)}$ (DDR2)	(k)	DDR2 Input High Voltage	SMVREF (DDR2) + 0.250	—	—	V	
V_{OL} (DDR2)	(k, l)	DDR2 Output Low Voltage	—	—	0.3	V	1
V_{OH} (DDR2)	(k, l)	DDR2 Output High Voltage	1.5	—		V	1
I_{Leak} (DDR2)	(k)	Input Leakage Current	—	—	±10	µA	
$C_{I/O}$ (DDR2)	(k, l)	DDR2 Input/Output Pin Capacitance	3.0	—	6.0	pF	
1.5V *PCI Express Interface Specification 1.0a*							
$V_{TX-DIFF\ P-P}$	(f)	Differential Peak to Peak Output Voltage	0.400	—	0.600	V	2
V_{TX_CM-ACp}	(f)	AC Peak Common Mode Output Voltage	—	—	20	mV	
$Z_{TX-DIFF-DC}$	(f)	DC Differential TX Impedance	80	100	120	Ohms	
$V_{RX-DIFF\ p-p}$	(e)	Differential Peak to Peak Input Voltage	0.175	—	0.600	V	3
V_{RX_CM-ACp}	(e)	AC peak Common Mode Input Voltage	—	—	150	mV	
Clocks, Reset, and Miscellaneous Signals							
V_{IL}	(n)	Input Low Voltage	—	—	0.8	V	
V_{IH}	(n)	Input High Voltage	2.0	—	—	V	
I_{LEAK}	(n)	Input Leakage Current	—	—	±10	µA	
C_{IN}	(n)	Input Capacitance	3.0	—	6.0	pF	
V_{IL}	(o)	Input Low Voltage	—	0	—	V	
V_{IH}	(o)	Input High Voltage	0.660	0.710	0.850	V	

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Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes[3]
V_{CROSS}	(o)	Crossing Voltage	0.45 x $(V_{IH} - V_{IL})$	0.5 x $(V_{IH} - V_{IL})$	0.55 x $(V_{IH} - V_{IL})$	V	
V_{OL}	(p)	Output Low Voltage (CMOS Outputs)	—	—	0.4	V	
V_{OH}	(p)	Output High Voltage (CMOS Outputs)	2.1	—	—	V	
I_{OL}	(p)	Output Low Current (CMOS Outputs)	—	—	1	mA	@V_{OL_HI} max
I_{OH}	(p)	Output High Current (CMOS Outputs)	−1	—	—	mA	@V_{OH_HI} min
V_{IL}	(p)	Input Low Voltage	—	—	1.1	V	
V_{IH}	(p)	Input High Voltage	1.4			V	
I_{LEAK}	(p)	Crossing Voltage	—	—	±10	µA	
C_{IN}	(p)	Input Capacitance	3.0	—	6.0	pF	
V_{IL}	(n1)	Input Low Voltage	—	—	0.8	V	
V_{IH}	(n1)	Input High Voltage	2.0	—	—	V	
I_{LEAK}	(n1)	Crossing Voltage	—	—	±100	µA	0 < V_{in} < VCC3_3
C_{IN}	(n1)	Input Capacitance	4.690	—	5.370	pF	

NOTES:
1. Determined with 2x MCH DDR2 Buffer Strength Settings into a 50 Ω to 0.5xV_{CCSM} (DDR2) test load.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Transmitter compliance eye diagram of the *PCI Express Interface Specification 1.0a* and measured over any 250 consecutive TX UIs.
3. Specified at the measurement point and measured over any 250 consecutive UIs. The test load shown in Receiver compliance eye diagram of the *PCI Express Interface Specification 1.0a* should be used as the RX device when taking measurements.

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12 Ballout and Package Information

This chapter provides the ballout and package information.

12.1 Ballout

Figure 12-1 and Figure 12-2 show the 82925X MCH ballout as viewed from the top side of the package. Table 12-1 provides the MCH ballout sorted by signal name and Table 12-2 provides the MCH ballout sorted by ball number.

Note: Balls that are listed as RSV are reserved. Board traces should be routed to these balls.

Note: Balls that are listed as NC are No Connects.

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Figure 12-1. Intel® 82925X MCH Ballout (Top View: Left Side)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A		NC	VSS		VSS	EXP_TXN3	EXP_TXP3	EXP_TXN1	EXP_TXP1	VSS	GCLKP	VCCA_DPLLA	VCC2	VCCA_EXPPLL	RSV	RSV	VCCA_HPLL	VSS
B	NC	VSS	EXP_RXP4	EXP_RXN4	VSS	VSS	VSS	VSS	VSS	VSS	GCLKN	VSS	VCCA_DPLLB	VSS	RSV	VSS	VCCA_SMPLL	VSS
C	VSS	EXP_TXP5	VSS	VSS	EXP_TXN4	EXP_TXP4	EXP_TXN2	EXP_TXP2	EXP_TXN0	EXP_TXP0	VSS		VSS	RSV	MTYPE	NC	VSS	VSS
D		EXP_TXN5	VSS	VSS	EXP_RXP5	VSS	VSS	VSS	VSS	VSS	VSS	RSV	RSV	RSV	VSS	VSS	BSEL2	VSS
E	VSS	VSS	EXP_TXP6	VSS	EXP_RXN5	VSS	EXP_RXN3	VSS	EXP_RXN2	VSS	EXP_RXP0	RSV	RSV	RSV	BSEL1	NC	VSS	VSS
F	EXP_TXP7	VSS	EXP_TXN6	VSS	VSS	VSS	EXP_RXP3	VSS	EXP_RXP2	VSS	EXP_RXN0	NC	RSV	RSV	RSV	VSS	HD47	VSS
G	EXP_TXN7	VSS	EXP_TXP8	VSS	EXP_RXN6	EXP_RXP6	VSS	VSS	VSS	VSS	VSS	NC	VSS	RSV	VSS	RSV	VSS	HD45
H	EXP_TXP9	VSS	EXP_TXN8	VSS	VSS	VSS	EXP_RXN7	EXP_RXP7	VSS	VSS	EXP_RXN1	NC	VSS	RSV	NC	BSEL0	NC	HD46
J	EXP_TXN9	VSS	EXP_TXP10	VSS	EXP_RXN8	EXP_RXP8	VSS	VSS	VSS	VSS	EXP_RXP1	NC	RSV	RSV	VSS	VSS	VSS	VSS
K	EXP_TXP11	VSS	EXP_TXN10	VSS	VSS	VSS	EXP_RXN9	EXP_RXP9	VSS	VSS	VSS	NC	RSV	VSS	RSV	EXTTS#	HD44	HD43
L	EXP_TXN11	VSS	EXP_TXP12	VSS	EXP_RXN10	EXP_RXP10	VSS	VSS	VSS	VCC	VSS	NC	VSS	RSV	VSS	VSS	VSS	VSS
M	EXP_TXP13	VSS	EXP_TXN12	VSS	VSS	VSS	EXP_RXN12	EXP_RXP12	VSS	VSS	VSS	DREFCLKN	DREFCLKP	ICH_SYNC#	RSV	RSV	VSS	HD42
N	EXP_TXN13	VSS	EXP_TXP14	VSS	EXP_RXN13	EXP_RXP13	VSS	VSS	VSS	VSS	VSS	NC	VCC	VCC	VCC	VCC	VSS	VCC
P	EXP_TXP15	VSS	EXP_TXN14	VSS	VSS	VSS	EXP_RXP14	EXP_RXN14	VSS	EXP_RXP11	VSS	NC	VCC	VCC	VCC	VSS	VCC	VSS
R	EXP_TXN15	VSS	DMI_TXP0	VSS	EXP_RXN15	EXP_RXP15	VSS	VSS	VSS	EXP_RXN11	VSS	NC	VCC	VCC	VCC	VCC	VSS	VCC
T	DMI_TXP1	VSS	DMI_TXN0	VSS	VSS	VSS	VSS	DMI_RXN1	DMI_RXP1	VSS	VSS	NC	VCC	VCC	VCC	VCC	VCC	VSS
U	DMI_TXN1	VSS	DMI_TXP2	VSS	DMI_RXP0	DMI_RXN0	VSS	VSS	VSS	DMI_RXN3	VSS	NC	VCC	VCC	VSS	VCC	VSS	VCC
V	VSS	VSS	DMI_TXN2	VSS	DMI_TXP3	VSS	DMI_RXP2	DMI_RXN2	VSS	DMI_RXP3	VSS	NC	VCC	VCC	VCC	VSS	VCC	VSS
W	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	DMI_TXN3	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	EXP_COMPI	VSS	NC	VCC	VCC	VSS	VCC	VSS	VCC
Y	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	VCC_EXP	EXP_COMPO	VSS	NC	VCC	VCC	VCC	VCC	VCC	VSS
AA	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC	VCC	VCC	VSS	VCC	VSS	VCC
AB	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	NC	VCC	VCC	VCC	VCC	VCC	VCC
AC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	RSV	RSV	RSV	RSV	RSV	RSV	RSV
AD	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VSS	SDQ_B20	VSS	SDQ_B17	SDQ_B29	VSS	SDQ_A29	SDQ_A24
AE	SDQ_A5	SDQ_A4	SDQ_A0	VSS	SOCOMP1	VSS	SVREF0	SVREF1	VSS	SMSLEWOUT1	SDQ_B4	VSS	SDQ_B21	SDQ_B19	SDQ_A28	RSV_TP0	SDQ_A24	NC
AF	VSS	SDM_A0	SDQ_A1	VSS	SOCOMP0	VSS	RSTIN#	VSS	SMSLEWIN1	VSS	SDQ_B5	SDQ_B11	SDQ_B16	SDQ_B18	SDQ_B28	SDQ_A25	SDM_A3	VSS
AG	SDQS_A0	SDQS_A0#	SDQ_A6	SRCOMP0	VSS	NC	PWROK	SRCOMP1	VSS	SDQ_B1	SDQ_B0	VSS	VSS	SDQS_B2#	VSS	VSS	SDQS_A3#	VSS
AH	VSS	SDQ_A7	SDQ_A2	SDQ_B12	NC	VSS	SDQ_B7	SDQS_B0	SDQS_B0#	SDM_B0	VSS	SDM_B2	SDQS_B2	VSS	RSV_TP1	SDQS_A3	SDQ_A27	VSS
AJ	SDQ_A12	SDQ_A3	SDQ_A13	VSS	SDQ_B13	SDQ_B3	SDQ_B2	SDQ_B6	VSS	VSS	SCLK_B1#	SMSLEWIN0	VSS	NC	VSS	VSS	SDQ_A31	SCB_B1
AK	VSS	SDQ_A8	SDQ_A9	VSS	SDM_B1	VSS	SDQ_A17	VSS	SCLK_B4	SDQ_B8	VSS	SMSLEWOUT0	SDQ_B22	VSS	RSV_TP3	SDQ_A30	VSS	SCB_B5
AL	SDM_A1	SDQS_A1#	SDQS_A1	SDQ_B9	SDQS_B1#	SDQ_B14	SDQ_A19	SDQ_B10	SCLK_B4#	VSS	SCLK_B1	VCCSM	VSS	SDQ_B23	RSV_TP2	VSS	SDQ_A26	SDQ_B26
AM		SCLK_A1	SCLK_A1#	VSS	SDQS_B1	VSS	SDQ_A22	SDQ_A23	SDQ_A18	VCCSM	VCCSM	NC	VCCSM	VCCSM	NC	VCCSM	VCCSM	NC
AN	VSS	SCLK_A4	SCLK_A4#	SDQ_A10	SDQ_A21	SDQ_B15	SDQS_A2#	SCKE_B3	SBS_B2	SMA_B12	SMA_B5		SMA_B4	SMA_B2	SMA_B0	SBS_B1	SRAS_B#	SCKE_A2
AP	NC	SDQ_A14	SDQ_A15	SDQ_A11	SDQ_A16	SDM_A2	SDQS_A2	VCCSM	SCKE_B1	SMA_B11	SMA_B9	VCCSM	SMA_B6	SMA_B3	SMA_B10	VCCSM	SWE_B#	SCAS_B#
AR	NC	NC	VSS		SDQ_A20	VSS	VCCSM	SCKE_B2	SCKE_B0	VCCSM	SMA_B7	SMA_B8	VSS	VCCSM	SMA_B1	SBS_B0	VSS	VCCSM
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**

Figure 12-2. Intel® 82925X MCH Ballout (Top View: Right Side)

	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35
A	VTT	VTT	VTT	VTT	HSWING	HVREF	HD48	VSS	HD61	HD57	HD55	VSS	HD53		VSS	NC	NC
B	VTT	VTT	VTT	VTT	HRCOMP	VSS	HD63	HDINV3#	HD54	VSS	HDSTBP3#	HD51	HD52	HD15	HD13	HD11	NC
C	VTT	VTT	VTT	VTT	VSS		HD58	HD59	HD49	HD56	HDSTBN3#	HD17	HD50	HD14	HD9	HD12	VSS
D	VTT	VTT	VTT	VTT	VSS	HSCOMP	VSS	VSS	HD60	VSS	HD18	VSS	VSS	VSS	HD10	HD8	
E	VTT	VTT	VTT	VTT	VSS	HD62	HD25	VSS	HD24	HD16	VSS	HBPRI#	HPCREQ#	HREQ1#	HDSTBP0#	HDINV0#	HDSTBN0#
F	HDSTBN2#	VTT	VTT	VTT	VSS	NC	VSS	HDSTBN1#	HD23	HD22	VSS	VSS	HREQ4#	VSS	HREQ0#	HD6	VSS
G	VSS	VSS	VTT	VTT	VSS	HCPURST#	HD26	VSS	VSS	VSS	HD20	HA6#	HREQ3#	HA7#	HD7	HD5	HD3
H	HD41	HD40	VSS	VTT	HD37	VSS	VSS	HDSTBP1#	VSS	HD19	HA3#	VSS	HREQ2#	VSS	HD1	VSS	HD4
J	HDSTBP2#	VSS	HD35	HD32	VSS	HD33	HD27	HDINV1#	HD21	HA13#	HA5#	VSS	HADSTB0	HRS2#	HD0	HD2	HDEFER#
K	HDINV2#	VSS	HD39	HD34	HD31	VSS	HD28	VSS	HA14#	VSS	HA4#	HA8#	VSS	VSS	HA15#	HRS0#	VSS
L	NC	VSS	VSS	VSS	HD30	VSS	HD29	HA18#	VSS	HA12#	HA9#	VSS	HA11#	VSS	HLOCK#	HHIT#	HDBSY#
M	HD38	VSS	HD36	HCLKN	HCLKP	VSS	VSS	HA20#	VSS	HA16#	VSS	HA10#	HADS#	HDRDY#		VSS	HBNR#
N	VSS	VCC	VCC	NC	NC	NC	VSS	HA19#	HADSTB1#	VSS	HA23#	VSS	HA21#	VSS	HA26#	HTRDY#	HHITM#
P	VCC	VSS	VCC	VCC	NC	NC	VSS	HA22#	VSS	HA24#	VSS	NC	VSS	VSS	HEDRDY#	HRS1#	VSS
R	VSS	VCC	VSS	VCC	VCC	NC	VSS	VSS	VSS	HA25#	HA17#	SCB_A4	SCB_A5	SDQ_A58	HBREQ0#	SDQ_A59	RSV
T	VCC	VCC	VCC	VSS	VCC	VCC	VSS	HA30#	HA27#	VSS	HA31#	VSS	HA28#	VSS	SDQ_A62	VSS	SDQ_A63
U	VSS	VCC	VSS	VCC	VSS	VCC	VSS	SDQ_B63	VSS	HA29#	VSS	SDQS_A8#	VSS	VSS	SDM_A7	SDQS_A7	SDQS_A7#
V	VCC	VSS	VCC	VSS	VCC	VCC	VSS	VSS	VSS	SDQ_B58	SDQ_B59	SDQS_A8	SCB_A1	SCB_A0	SDQ_A57	SDQ_A56	VSS
W	VSS	VCC	VSS	VCC	VSS	VCC	VSS	SDQ_B62	SDQS_B7	VSS	SDQ_B57	VSS	SDM_B7	VSS	SDQ_A61	SDQ_A51	SDQ_A60
Y	VCC	VCC	VCC	VSS	VCC	VSS	VSS	SDQ_B60	VSS	SDQS_B7#	VSS	SCB_A6	VSS	VSS	SDQ_A50	VSS	SDQ_A55
AA	VSS	VCC	VCC	VCC	VCC	VCC	VSS	VSS	VSS	SDQ_B56	SDQ_B61	SCB_A3	SCB_A2	SDQ_A54	SDM_A6	SDQS_A6	SDQS_A6#
AB	VCC	VCC	VCC	VCC	VCC	VCC	VSS	SDQ_B51	SDQ_B55	VSS	SCB_A7	VSS	SDQS_B6	VSS	RSV	SCLK_A2	VSS
AC	RSV	RSV	RSV	RSV	NC	NC	VSS	SDQ_B50	VSS	SDQ_B54	VSS	SDQS_B6#	VSS	VSS	SCLK_A2#	SCLK_A5#	SCLK_A5
AD	VSS	VSS	NC	VSS	SDQ_B37	SDM_B6	VSS	VSS	SDQ_A35	SCLK_B5#	SCLK_B5	NC	SDQ_A48	RSV		VSS	SDQ_A49
AE	SDQ_B25	SDM_B3	VSS	VSS	VSS	VSS	SCLK_B2#	SCLK_B2	SDQ_B49	VSS	SDQ_B53	NC	SDQ_B52	VSS	SDQ_A43	SDQ_A53	SDQ_A52
AF	NC	SDQS_B3#	VSS	NC	SDQ_B36	SDQ_B32	SDM_B4	VSS	SDQ_B48	SDQ_A39	VSS	SDQ_B43	VSS	VSS	SDQ_A42	SDQ_A47	VSS
AG	VSS	SDQS_B3	VSS	VSS	SCLK_B0#	SDQ_B33	NC	SDQS_B4#	SDQ_A38	SDQ_B47	NC	SDQ_B46	SDQ_B42	SDQ_A46	SDQS_A5#	SDM_A5	SDQS_A5
AH	SDQ_B30	VSS	SDQ_B31	VSS	SCLK_B0	NC	SDQS_B4	VSS	SDQ_A34	SDQS_B5	VSS	SDQS_B5#	SDM_B5	VSS	VSS	SDQ_A40	SDQ_A41
AJ	VSS	SCB_B0	SDQS_B8#	VSS	SCB_B2	SCB_B3	SDQ_B39	SDQ_B35	VSS	SDQS_A4#	SDQ_B44	VSS	SDQ_B41	VSS	SDM_A4	SDQ_A45	VSS
AK	SDQ_B27	VSS	SDQS_B8	SCLK_B3#	VSS	NC	VSS	VSS	SDQS_A4	SCLK_A0	SDQ_A32	VSS	SDQ_A33	SDQ_B40	SDQ_B45	SDQ_A44	VCCSM
AL	VSS	SCB_B4	SCB_B6	SCB_B7	SCLK_B3	VSS	SDQ_B38	SDQ_B34	NC	SCLK_A0#	SCLK_A3#	SDQ_A36	SDQ_A37	VSS	SODT_B3	SODT_B1	SODT_B2
AM	VCCSM	VCCSM	NC	VCCSM	VCCSM	NC	VCCSM	VCCSM	VCCSM	VSS	VCCSM	SCLK_A3	VSS	VCCSM	SCS_B1#	SCS_A3#	
AN	SCKE_A1	SMA_A12	SMA_A7	SMA_A5	SMA_A8		SMA_A2	SMA_A0	SBS_A0	SWE_A#	SODT_A2	SMA_A13	SCS_A1#	SODT_A3	SCS_B2#	SODT_B0	VCCSM
AP	SCKE_A0	VCCSM	SMA_A11	SMA_A9	SMA_A4	VCCSM	SMA_A1	SMA_A10	SRAS_A#	VCCSM	SCAS_A#	SODT_A0	SCS_A3#	SODT_A1	SCS_B0#	SCS_B3#	NC
AR	SCKE_A3	SBS_A2	VSS	VCCSM	SMA_A6	SMA_A3	VSS	VCCSM	SBS_A1	SCS_A2#	SCS_A0#	VSS	VCCSM		VCCSM	NC	NC
	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35

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Signal Name	Ball #
BSEL0	H16
BSEL1	E15
BSEL2	D17
DMI_RXN0	U6
DMI_RXN1	T8
DMI_RXN2	V8
DMI_RXN3	U10
DMI_RXP0	U5
DMI_RXP1	T9
DMI_RXP2	V7
DMI_RXP3	V10
DMI_TXN0	T3
DMI_TXN1	U1
DMI_TXN2	V3
DMI_TXN3	W5
DMI_TXP0	R3
DMI_TXP1	T1
DMI_TXP2	U3
DMI_TXP3	V5
DREFCLKN	M12
DREFCLKP	M13
EXP_COMPI	W10
EXP_COMPO	Y10
EXP_RXN0	F11
EXP_RXN1	H11
EXP_RXN10	L5
EXP_RXN11	R10
EXP_RXN12	M7
EXP_RXN13	N5
EXP_RXN14	P8
EXP_RXN15	R5
EXP_RXN2	E9
EXP_RXN3	E7
EXP_RXN4	B4
EXP_RXN5	E5
EXP_RXN6	G5
EXP_RXN7	H7

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
EXP_RXN8	J5
EXP_RXN9	K7
EXP_RXP0	E11
EXP_RXP1	J11
EXP_RXP10	L6
EXP_RXP11	P10
EXP_RXP12	M8
EXP_RXP13	N6
EXP_RXP14	P7
EXP_RXP15	R6
EXP_RXP2	F9
EXP_RXP3	F7
EXP_RXP4	B3
EXP_RXP5	D5
EXP_RXP6	G6
EXP_RXP7	H8
EXP_RXP8	J6
EXP_RXP9	K8
EXP_TXN0	C9
EXP_TXN1	A8
EXP_TXN10	K3
EXP_TXN11	L1
EXP_TXN12	M3
EXP_TXN13	N1
EXP_TXN14	P3
EXP_TXN15	R1
EXP_TXN2	C7
EXP_TXN3	A6
EXP_TXN4	C5
EXP_TXN5	D2
EXP_TXN6	F3
EXP_TXN7	G1
EXP_TXN8	H3
EXP_TXN9	J1
EXP_TXP0	C10
EXP_TXP1	A9
EXP_TXP10	J3

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
EXP_TXP11	K1
EXP_TXP12	L3
EXP_TXP13	M1
EXP_TXP14	N3
EXP_TXP15	P1
EXP_TXP2	C8
EXP_TXP3	A7
EXP_TXP4	C6
EXP_TXP5	C2
EXP_TXP6	E3
EXP_TXP7	F1
EXP_TXP8	G3
EXP_TXP9	H1
EXTTS#	K16
GCLKN	B11
GCLKP	A11
HA3#	H29
HA4#	K29
HA5#	J29
HA6#	G30
HA7#	G32
HA8#	K30
HA9#	L29
HA10#	M30
HA11#	L31
HA12#	L28
HA13#	J28
HA14#	K27
HA15#	K33
HA16#	M28
HA17#	R29
HA18#	L26
HA19#	N26
HA20#	M26
HA21#	N31
HA22#	P26
HA23#	N29

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
HA24#	P28
HA25#	R28
HA26#	N33
HA27#	T27
HA28#	T31
HA29#	U28
HA30#	T26
HA31#	T29
HADS#	M31
HADSTB0#	J31
HADSTB1#	N27
HBNR#	M35
HBPRI#	E30
HBREQ0#	R33
HCLKN	M22
HCLKP	M23
HCPURST#	G24
HD00	J33
HD1	H33
HD2	J34
HD3	G35
HD4	H35
HD5	G34
HD6	F34
HD7	G33
HD8	D34
HD9	C33
HD10	D33
HD11	B34
HD12	C34
HD13	B33
HD14	C32
HD15	B32
HD16	E28
HD17	C30
HD18	D29
HD19	H28
HD20	G29

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
HD21	J27
HD22	F28
HD23	F27
HD24	E27
HD25	E25
HD26	G25
HD27	J25
HD28	K25
HD29	L25
HD30	L23
HD31	K23
HD32	J22
HD33	J24
HD34	K22
HD35	J21
HD36	M21
HD37	H23
HD38	M19
HD39	K21
HD40	H20
HD41	H19
HD42	M18
HD43	K18
HD44	K17
HD45	G18
HD46	H18
HD47	F17
HD48	A25
HD49	C27
HD50	C31
HD51	B30
HD52	B31
HD53	A31
HD54	B27
HD55	A29
HD56	C28
HD57	A28
HD58	C25

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
HD59	C26
HD60	D27
HD61	A27
HD62	E24
HD63	B25
HDBSY#	L35
HDEFER#	J35
HDINV0#	E34
HDINV1#	J26
HDINV2#	K19
HDINV3#	B26
HDRDY#	M32
HDSTBN0#	E35
HDSTBN1#	F26
HDSTBN2#	F19
HDSTBN3#	C29
HDSTBP0#	E33
HDSTBP1#	H26
HDSTBP2#	J19
HDSTBP3#	B29
HEDRDY#	P33
HHIT#	L34
HHITM#	N35
HLOCK#	L33
HPCREQ#	E31
HRCOMP	B23
HREQ0#	F33
HREQ1#	E32
HREQ2#	H31
HREQ3#	G31
HREQ4#	F31
HRS0#	K34
HRS1#	P34
HRS2#	J32
HSCOMP	D24
HSWING	A23
HTRDY#	N34
HVREF	A24

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Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
ICH_SYNC#	M14
MTYPE	C15
NC	A34
NC	A35
NC	AA12
NC	AB12
NC	AC23
NC	AC24
NC	AD21
NC	AD30
NC	AE18
NC	AE30
NC	AF19
NC	AF22
NC	AG25
NC	AG29
NC	AG6
NC	AH24
NC	AH5
NC	AJ14
NC	AK24
NC	AL27
NC	AM12
NC	AM15
NC	AM18
NC	AM21
NC	AM24
NC	AP1
NC	AP35
NC	AR1
NC	AR2
NC	AR34
NC	AR35
NC	B1
NC	B35
NC	C16
NC	E16
NC	F12

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
NC	F24
NC	G12
NC	H12
NC	H15
NC	H17
NC	J12
NC	K12
NC	L12
NC	L19
NC	N12
NC	N22
NC	N23
NC	N24
NC	P12
NC	P23
NC	P24
NC	P30
NC	R12
NC	R24
NC	T12
NC	U12
NC	V12
NC	W12
NC	Y12
NC	A2
PWROK	AG7
RSTIN#	AF7
RSV	H14
RSV	J14
RSV	M15
RSV	L14
RSV	D14
RSV	E14
RSV	E12
RSV	F14
RSV	G14
RSV	A15
RSV	A16

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
RSV	AC12
RSV	AC13
RSV	AC14
RSV	AC15
RSV	AC16
RSV	AC17
RSV	AC18
RSV	AC19
RSV	AC20
RSV	AC21
RSV	AC22
RSV	B15
RSV	C14
RSV	F15
RSV	G16
RSV	J13
RSV	K13
RSV	K15
RSV	M16
RSV	R35
RSV	D13
RSV	E13
RSV	F13
RSV	AB33
RSV	AD32
RSV	D12
RSV_TP0	AE16
RSV_TP1	AH15
RSV_TP2	AL15
RSV_TP3	AK15
SBS_A0	AN27
SBS_A1	AR27
SBS_A2	AR20
SBS_B0	AR16
SBS_B1	AN16
SBS_B2	AN9
SCAS_A#	AP29
SCAS_B#	AP18

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
SCB_A0	V32
SCB_A1	V31
SCB_A2	AA31
SCB_A3	AA30
SCB_A4	R30
SCB_A5	R31
SCB_A6	Y30
SCB_A7	AB29
SCB_B0	AJ20
SCB_B1	AJ18
SCB_B2	AJ23
SCB_B3	AJ24
SCB_B4	AL20
SCB_B5	AK18
SCB_B6	AL21
SCB_B7	AL22
SCKE_A0	AP19
SCKE_A1	AN19
SCKE_A2	AN18
SCKE_A3	AR19
SCKE_B0	AR9
SCKE_B1	AP9
SCKE_B2	AR8
SCKE_B3	AN8
SCLK_A0	AL29
SCLK_A0#	AM30
SCLK_A1	AN2
SCLK_A1#	AN3
SCLK_A2	AC34
SCLK_A2#	AC35
SCLK_A3	AL28
SCLK_A3#	AK28
SCLK_A4	AM3
SCLK_A4#	AM2
SCLK_A5	AC33
SCLK_A5#	AB34
SCLK_B0	AH23
SCLK_B0#	AG23

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
SCLK_B1	AK9
SCLK_B1#	AL9
SCLK_B2	AE26
SCLK_B2#	AE25
SCLK_B3	AL23
SCLK_B3#	AK22
SCLK_B4	AJ11
SCLK_B4#	AL11
SCLK_B5	AD28
SCLK_B5#	AD29
SCS_A0#	AR29
SCS_A1#	AN31
SCS_A2#	AR28
SCS_A3#	AP31
SCS_B0#	AP33
SCS_B1#	AM33
SCS_B2#	AN33
SCS_B3#	AP34
SDM_A0	AF2
SDM_A1	AL1
SDM_A2	AP6
SDM_A3	AF17
SDM_A4	AJ33
SDM_A5	AG34
SDM_A6	AA33
SDM_A7	U33
SDM_B0	AH10
SDM_B1	AK5
SDM_B2	AH12
SDM_B3	AE20
SDM_B4	AF25
SDM_B5	AH31
SDM_B6	AD24
SDM_B7	W31
SDQ_A00	AE3
SDQ_A01	AF3
SDQ_A02	AH3
SDQ_A03	AJ2

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
SDQ_A04	AE2
SDQ_A05	AE1
SDQ_A06	AG3
SDQ_A07	AH2
SDQ_A08	AK2
SDQ_A09	AK3
SDQ_A10	AN4
SDQ_A11	AP4
SDQ_A12	AJ1
SDQ_A13	AJ3
SDQ_A14	AP2
SDQ_A15	AP3
SDQ_A16	AP5
SDQ_A17	AK7
SDQ_A18	AM9
SDQ_A19	AL7
SDQ_A20	AR5
SDQ_A21	AN5
SDQ_A22	AM7
SDQ_A23	AM8
SDQ_A24	AE17
SDQ_A25	AF16
SDQ_A26	AL17
SDQ_A27	AH17
SDQ_A28	AE15
SDQ_A29	AD17
SDQ_A30	AK16
SDQ_A31	AJ17
SDQ_A32	AK29
SDQ_A33	AK31
SDQ_A34	AH27
SDQ_A35	AD27
SDQ_A36	AL30
SDQ_A37	AL31
SDQ_A38	AG27
SDQ_A39	AF28
SDQ_A40	AH34
SDQ_A41	AH35

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**Table 12-1. MCH Ballout
Sorted By Signal Name**

Signal Name	Ball #
SDQ_A42	AF33
SDQ_A43	AE33
SDQ_A44	AK34
SDQ_A45	AJ34
SDQ_A46	AG32
SDQ_A47	AF34
SDQ_A48	AD31
SDQ_A49	AD35
SDQ_A50	Y33
SDQ_A51	W34
SDQ_A52	AE35
SDQ_A53	AE34
SDQ_A54	AA32
SDQ_A55	Y35
SDQ_A56	V34
SDQ_A57	V33
SDQ_A58	R32
SDQ_A59	R34
SDQ_A60	W35
SDQ_A61	W33
SDQ_A62	T33
SDQ_A63	T35
SDQ_B00	AG11
SDQ_B01	AG10
SDQ_B02	AJ7
SDQ_B03	AJ6
SDQ_B04	AE11
SDQ_B05	AF11
SDQ_B06	AJ8
SDQ_B07	AH7
SDQ_B08	AK10
SDQ_B09	AL4
SDQ_B10	AL8
SDQ_B11	AF12
SDQ_B12	AH4
SDQ_B13	AJ5
SDQ_B14	AL6
SDQ_B15	AN6

Signal Name	Ball #
SDQ_B16	AF13
SDQ_B17	AD14
SDQ_B18	AF14
SDQ_B19	AE14
SDQ_B20	AD12
SDQ_B21	AE13
SDQ_B22	AK13
SDQ_B23	AL14
SDQ_B24	AD18
SDQ_B25	AE19
SDQ_B26	AL18
SDQ_B27	AK19
SDQ_B28	AF15
SDQ_B29	AD15
SDQ_B30	AH19
SDQ_B31	AH21
SDQ_B32	AF24
SDQ_B33	AG24
SDQ_B34	AL26
SDQ_B35	AJ26
SDQ_B36	AF23
SDQ_B37	AD23
SDQ_B38	AL25
SDQ_B39	AJ25
SDQ_B40	AK32
SDQ_B41	AJ31
SDQ_B42	AG31
SDQ_B43	AF30
SDQ_B44	AJ29
SDQ_B45	AK33
SDQ_B46	AG30
SDQ_B47	AG28
SDQ_B48	AF27
SDQ_B49	AE27
SDQ_B50	AC26
SDQ_B51	AB26
SDQ_B52	AE31
SDQ_B53	AE29

Signal Name	Ball #
SDQ_B54	AC28
SDQ_B55	AB27
SDQ_B56	AA28
SDQ_B57	W29
SDQ_B58	V28
SDQ_B59	V29
SDQ_B60	Y26
SDQ_B61	AA29
SDQ_B62	W26
SDQ_B63	U26
SDQS_A0	AG1
SDQS_A0#	AG2
SDQS_A1	AL3
SDQS_A1#	AL2
SDQS_A2	AP7
SDQS_A2#	AN7
SDQS_A3	AH16
SDQS_A3#	AG17
SDQS_A4	AK27
SDQS_A4#	AJ28
SDQS_A5	AG35
SDQS_A5#	AG33
SDQS_A6	AA34
SDQS_A6#	AA35
SDQS_A7	U34
SDQS_A7#	U35
SDQS_A8	V30
SDQS_A8#	U30
SDQS_B0	AH8
SDQS_B0#	AH9
SDQS_B1	AM5
SDQS_B1#	AL5
SDQS_B2	AH13
SDQS_B2#	AG14
SDQS_B3	AG20
SDQS_B3#	AF20
SDQS_B4	AH25
SDQS_B4#	AG26

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
SDQS_B5	AH28
SDQS_B5#	AH30
SDQS_B6	AB31
SDQS_B6#	AC30
SDQS_B7	W27
SDQS_B7#	Y28
SDQS_B8	AK21
SDQS_B8#	AJ21
SMA_A0	AN26
SMA_A1	AP25
SMA_A2	AN25
SMA_A3	AR24
SMA_A4	AP23
SMA_A5	AN22
SMA_A6	AR23
SMA_A7	AN21
SMA_A8	AN23
SMA_A9	AP22
SMA_A10	AP26
SMA_A11	AP21
SMA_A12	AN20
SMA_A13	AN30
SMA_B0	AN15
SMA_B1	AR15
SMA_B2	AN14
SMA_B3	AP14
SMA_B4	AN13
SMA_B5	AN11
SMA_B6	AP13
SMA_B7	AR11
SMA_B8	AR12
SMA_B9	AP11
SMA_B10	AP15
SMA_B11	AP10
SMA_B12	AN10
SMA_B13	AM34
SMSLEWIN0	AJ12
SMSLEWIN1	AF9

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
SMSLEWOUT0	AK12
SMSLEWOUT1	AE10
SOCOMP0	AF5
SOCOMP1	AE5
SODT_A0	AP30
SODT_A1	AP32
SODT_A2	AN29
SODT_A3	AN32
SODT_B0	AN34
SODT_B1	AL34
SODT_B2	AL35
SODT_B3	AL33
SRAS_A#	AP27
SRAS_B#	AN17
SRCOMP0	AG4
SRCOMP1	AG8
SVREF0	AE7
SVREF1	AE8
SWE_A#	AN28
SWE_B#	AP17
VCC	R16
VCC	R18
VCC	R20
VCC	R22
VCC	R23
VCC	T13
VCC	T14
VCC	T15
VCC	T16
VCC	T17
VCC	T19
VCC	T20
VCC	T21
VCC	T23
VCC	T24
VCC	U13
VCC	U14
VCC	U16

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VCC	U18
VCC	U20
VCC	U22
VCC	U24
VCC	V13
VCC	V14
VCC	V15
VCC	V17
VCC	V19
VCC	V21
VCC	V23
VCC	V24
VCC	W13
VCC	W14
VCC	W16
VCC	W18
VCC	W20
VCC	W22
VCC	W24
VCC	Y13
VCC	Y14
VCC	AA13
VCC	AA14
VCC	AA16
VCC	AA18
VCC	AA20
VCC	AA21
VCC	AA22
VCC	AA23
VCC	AA24
VCC	AB1
VCC	AB10
VCC	AB11
VCC	AB13
VCC	AB14
VCC	AB15
VCC	AB16
VCC	AB17

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Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VCC	AB18
VCC	AB19
VCC	AB2
VCC	AB20
VCC	AB21
VCC	AB22
VCC	AB23
VCC	AB24
VCC	AB3
VCC	AB4
VCC	AB5
VCC	AB6
VCC	AB7
VCC	AB8
VCC	AB9
VCC	Y15
VCC	Y16
VCC	Y17
VCC	Y19
VCC	Y20
VCC	Y21
VCC	Y23
VCC	Y24
VCC	AC1
VCC	AC10
VCC	AC11
VCC	AC2
VCC	AC3
VCC	AC4
VCC	AC5
VCC	AC6
VCC	AC7
VCC	AC8
VCC	AC9
VCC	AD1
VCC	AD10
VCC	AD2
VCC	AD3

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VCC	AD4
VCC	AD5
VCC	AD6
VCC	AD7
VCC	AD8
VCC	AD9
VCC	L10
VCC	N13
VCC	N14
VCC	N15
VCC	N16
VCC	N18
VCC	N20
VCC	N21
VCC	P13
VCC	P14
VCC	P15
VCC	P17
VCC	P19
VCC	P21
VCC	P22
VCC	R13
VCC	R14
VCC	R15
VCC_EXP	W1
VCC_EXP	W2
VCC_EXP	W3
VCC_EXP	W4
VCC_EXP	W6
VCC_EXP	W7
VCC_EXP	W8
VCC_EXP	W9
VCC_EXP	Y1
VCC_EXP	Y2
VCC_EXP	Y3
VCC_EXP	Y4
VCC_EXP	Y5
VCC_EXP	Y6

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VCC_EXP	Y7
VCC_EXP	Y8
VCC_EXP	Y9
VCC2	A13
VCCA_DPLLA	A12
VCCA_DPLLB	B13
VCCA_EXPPLL	A14
VCCA_HPLL	A17
VCCA_SMPLL	B17
VCCSM	AK35
VCCSM	AL12
VCCSM	AM10
VCCSM	AM11
VCCSM	AM13
VCCSM	AM14
VCCSM	AM16
VCCSM	AM17
VCCSM	AM19
VCCSM	AM20
VCCSM	AM22
VCCSM	AM23
VCCSM	AM26
VCCSM	AM27
VCCSM	AM29
VCCSM	AM32
VCCSM	AN35
VCCSM	AP12
VCCSM	AP16
VCCSM	AP20
VCCSM	AP24
VCCSM	AP28
VCCSM	AP8
VCCSM	AR10
VCCSM	AR14
VCCSM	AR18
VCCSM	AR22
VCCSM	AR26
VCCSM	AR31

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VCCSM	AR33
VCCSM	AR7
VCCSM	AM25
VSS	AA26
VSS	AA27
VSS	AA3
VSS	AA4
VSS	AA5
VSS	AA6
VSS	AA7
VSS	AA8
VSS	AA9
VSS	AB25
VSS	AB28
VSS	AB30
VSS	AB32
VSS	AB35
VSS	AC25
VSS	AC27
VSS	AC29
VSS	AC31
VSS	AC32
VSS	AD11
VSS	AD13
VSS	AD16
VSS	AD19
VSS	AD20
VSS	AD22
VSS	AD25
VSS	AD26
VSS	AD34
VSS	AE12
VSS	AE21
VSS	AE22
VSS	AE23
VSS	AE24
VSS	AE28
VSS	AE32

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VSS	AE4
VSS	AE6
VSS	AE9
VSS	AF1
VSS	B18
VSS	B2
VSS	B24
VSS	B28
VSS	B5
VSS	B6
VSS	B7
VSS	B8
VSS	B9
VSS	C1
VSS	C11
VSS	C13
VSS	C17
VSS	C18
VSS	C23
VSS	C3
VSS	C35
VSS	C4
VSS	D10
VSS	D11
VSS	D15
VSS	D16
VSS	D18
VSS	D23
VSS	D25
VSS	D26
VSS	D28
VSS	D3
VSS	D30
VSS	D31
VSS	D32
VSS	D4
VSS	D6
VSS	D7

Table 12-1. MCH Ballout Sorted By Signal Name

Signal Name	Ball #
VSS	D8
VSS	D9
VSS	E1
VSS	E10
VSS	E17
VSS	K6
VSS	K9
VSS	L11
VSS	L13
VSS	L15
VSS	L16
VSS	L17
VSS	L18
VSS	L2
VSS	L20
VSS	L21
VSS	L22
VSS	L24
VSS	L27
VSS	L30
VSS	L32
VSS	L4
VSS	L7
VSS	L8
VSS	L9
VSS	M10
VSS	M11
VSS	M17
VSS	M2
VSS	M20
VSS	M24
VSS	M25
VSS	M27
VSS	M29
VSS	M34
VSS	M4
VSS	M5
VSS	M6

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Signal Name	Ball #
VSS	M9
VSS	N10
VSS	N11
VSS	N17
VSS	N19
VSS	N2
VSS	W19
VSS	W21
VSS	W23
VSS	W25
VSS	W28
VSS	W30
VSS	W32
VSS	Y11
VSS	Y18
VSS	Y22
VSS	Y25
VSS	Y27
VSS	Y29
VSS	Y31
VSS	AF10
VSS	AF18
VSS	AF21
VSS	AF26
VSS	AF29
VSS	AF31
VSS	AF32
VSS	AF35
VSS	AF4
VSS	AF6
VSS	AF8
VSS	AG12
VSS	AG13
VSS	AG15
VSS	AG16
VSS	AG18
VSS	AG19
VSS	AG21

Signal Name	Ball #
VSS	AG22
VSS	AG5
VSS	AG9
VSS	AH1
VSS	AH11
VSS	AH14
VSS	AH18
VSS	AH20
VSS	AH22
VSS	AH26
VSS	AH29
VSS	AH32
VSS	AH33
VSS	AH6
VSS	AJ10
VSS	AJ13
VSS	AJ15
VSS	AJ16
VSS	AJ19
VSS	AJ22
VSS	AJ27
VSS	E18
VSS	E2
VSS	E23
VSS	E26
VSS	E29
VSS	E4
VSS	E6
VSS	E8
VSS	F10
VSS	F16
VSS	F18
VSS	F2
VSS	F23
VSS	F25
VSS	F29
VSS	F30
VSS	F32

Signal Name	Ball #
VSS	F35
VSS	F4
VSS	F5
VSS	F6
VSS	F8
VSS	G10
VSS	G11
VSS	G13
VSS	G15
VSS	G17
VSS	G19
VSS	G2
VSS	G20
VSS	G23
VSS	G26
VSS	G27
VSS	G28
VSS	G4
VSS	G7
VSS	G8
VSS	G9
VSS	H10
VSS	N25
VSS	N28
VSS	N30
VSS	N32
VSS	N4
VSS	N7
VSS	N8
VSS	N9
VSS	P11
VSS	P16
VSS	P18
VSS	P2
VSS	P20
VSS	P25
VSS	P27
VSS	P29

**Table 12-1. MCH Ballout
Sorted By Signal Name**

Signal Name	Ball #
VSS	P31
VSS	P32
VSS	P35
VSS	P4
VSS	P5
VSS	P6
VSS	P9
VSS	R11
VSS	R17
VSS	R19
VSS	R2
VSS	R21
VSS	R25
VSS	R26
VSS	R27
VSS	R4
VSS	R7
VSS	R8
VSS	R9
VSS	T10
VSS	T11
VSS	T18
VSS	T2
VSS	Y32
VSS	Y34
VSS	A10
VSS	A18
VSS	A26
VSS	A3
VSS	A30
VSS	A33
VSS	A5
VSS	AA1
VSS	AA10
VSS	AA11
VSS	AA15
VSS	AA17
VSS	AA19

Signal Name	Ball #
VSS	AA2
VSS	AA25
VSS	AJ30
VSS	AJ32
VSS	AJ35
VSS	AJ4
VSS	AJ9
VSS	AK1
VSS	AK11
VSS	AK14
VSS	AK17
VSS	AK20
VSS	AK23
VSS	AK25
VSS	AK26
VSS	AK30
VSS	AK4
VSS	AK6
VSS	AK8
VSS	AL10
VSS	AL13
VSS	AL16
VSS	AL19
VSS	AL24
VSS	AL32
VSS	AM28
VSS	AM31
VSS	AM4
VSS	AM6
VSS	AN1
VSS	AR13
VSS	AR17
VSS	AR21
VSS	AR25
VSS	AR3
VSS	AR30
VSS	AR6
VSS	B10

Signal Name	Ball #
VSS	B12
VSS	B14
VSS	B16
VSS	H13
VSS	H2
VSS	H21
VSS	H24
VSS	H25
VSS	H27
VSS	H30
VSS	H32
VSS	H34
VSS	H4
VSS	H5
VSS	H6
VSS	H9
VSS	J10
VSS	J15
VSS	J16
VSS	J17
VSS	J18
VSS	J2
VSS	J20
VSS	J23
VSS	J30
VSS	J4
VSS	J7
VSS	J8
VSS	J9
VSS	K10
VSS	K11
VSS	K14
VSS	K2
VSS	K20
VSS	K24
VSS	K26
VSS	K28
VSS	K31

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**Table 12-1. MCH Ballout
Sorted By Signal Name**

Signal Name	Ball #
VSS	K32
VSS	K35
VSS	K4
VSS	K5
VSS	T22
VSS	T25
VSS	T28
VSS	T30
VSS	T32
VSS	T34
VSS	T4
VSS	T5
VSS	T6
VSS	T7
VSS	U11
VSS	U15
VSS	U17
VSS	U19
VSS	U2
VSS	U21
VSS	U23
VSS	U25
VSS	U27
VSS	U29
VSS	U31
VSS	U32
VSS	U4
VSS	U7
VSS	U8
VSS	U9
VSS	V1
VSS	V11
VSS	V16
VSS	V18
VSS	V2
VSS	V20
VSS	V22
VSS	V25

Signal Name	Ball #
VSS	V26
VSS	V27
VSS	V35
VSS	V4
VSS	V6
VTT	A19
VTT	A20
VTT	A21
VTT	A22
VTT	B19
VTT	B20
VTT	B21
VTT	B22
VTT	C19
VTT	C20
VTT	C21
VTT	C22
VTT	D19
VTT	D20
VTT	D21
VTT	D22
VTT	E19
VTT	E20
VTT	E21
VTT	E22
VTT	F20
VTT	F21
VTT	F22
VTT	G21
VTT	G22
VTT	H22

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
A1	—
A2	NC
A3	VSS
A4	—
A5	VSS
A6	EXP_TXN3
A7	EXP_TXP3
A8	EXP_TXN1
A9	EXP_TXP1
A10	VSS
A11	GCLKP
A12	VCCA_DPLLA
A13	VCC2
A14	VCCA_EXPPLL
A15	RSV
A16	RSV
A17	VCCA_HPLL
A18	VSS
A19	VTT
A20	VTT
A21	VTT
A22	VTT
A23	HSWING
A24	HVREF
A25	HD48
A26	VSS
A27	HD61
A28	HD57
A29	HD55
A30	VSS
A31	HD53
A32	—

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
A33	VSS
A34	NC
A35	NC
B1	NC
B2	VSS
B3	EXP_RXP4
B4	EXP_RXN4
B5	VSS
B6	VSS
B7	VSS
B8	VSS
B9	VSS
B10	VSS
B11	GCLKN
B12	VSS
B13	VCCA_DPLLB
B14	VSS
B15	RSV
B16	VSS
B17	VCCA_SMPLL
B18	VSS
B19	VTT
B20	VTT
B21	VTT
B22	VTT
B23	HRCOMP
B24	VSS
B25	HD63
B26	HDINV3#
B27	HD54
B28	VSS
B29	HDSTBP3#
B30	HD51

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
B31	HD52
B32	HD15
B33	HD13
B34	HD11
B35	NC
C1	VSS
C2	EXP_TXP5
C3	VSS
C4	VSS
C5	EXP_TXN4
C6	EXP_TXP4
C7	EXP_TXN2
C8	EXP_TXP2
C9	EXP_TXN0
C10	EXP_TXP0
C11	VSS
C12	—
C13	VSS
C14	RSV
C15	MTYPE
C16	NC
C17	VSS
C18	VSS
C19	VTT
C20	VTT
C21	VTT
C22	VTT
C23	VSS
C24	—
C25	HD58
C26	HD59
C27	HD49
C28	HD56

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Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
C29	HDSTBN3#
C30	HD17
C31	HD50
C32	HD14
C33	HD9
C34	HD12
C35	VSS
D1	—
D2	EXP_TXN5
D3	VSS
D4	VSS
D5	EXP_RXP5
D6	VSS
D7	VSS
D8	VSS
D9	VSS
D10	VSS
D11	VSS
D12	RSV
D13	RSV
D14	RSV
D15	VSS
D16	VSS
D17	BSEL2
D18	VSS
D19	VTT
D20	VTT
D21	VTT
D22	VTT
D23	VSS
D24	HSCOMP
D25	VSS
D26	VSS

Ball #	Signal Name
D27	HD60
D28	VSS
D29	HD18
D30	VSS
D31	VSS
D32	VSS
D33	HD10
D34	HD8
D35	—
E1	VSS
E2	VSS
E3	EXP_TXP6
E4	VSS
E5	EXP_RXN5
E6	VSS
E7	EXP_RXN3
E8	VSS
E9	EXP_RXN2
E10	VSS
E11	EXP_RXP0
E12	RSV
E13	RSV
E14	RSV
E15	BSEL1
E16	NC
E17	VSS
E18	VSS
E19	VTT
E20	VTT
E21	VTT
E22	VTT
E23	VSS
E24	HD62

Ball #	Signal Name
E25	HD25
E26	VSS
E27	HD24
E28	HD16
E29	VSS
E30	HBPRI#
E31	HPCREQ#
E32	HREQ1#
E33	HDSTBP0#
E34	HDINV0#
E35	HDSTBN0#
F1	EXP_TXP7
F2	VSS
F3	EXP_TXN6
F4	VSS
F5	VSS
F6	VSS
F7	EXP_RXP3
F8	VSS
F9	EXP_RXP2
F10	VSS
F11	EXP_RXN0
F12	NC
F13	RSV
F14	RSV
F15	RSV
F16	VSS
F17	HD47
F18	VSS
F19	HDSTBN2#
F20	VTT
F21	VTT
F22	VTT

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
F23	VSS
F24	NC
F25	VSS
F26	HDSTBN1#
F27	HD23
F28	HD22
F29	VSS
F30	VSS
F31	HREQ4#
F32	VSS
F33	HREQ0#
F34	HD6
F35	VSS
G1	EXP_TXN7
G2	VSS
G3	EXP_TXP8
G4	VSS
G5	EXP_RXN6
G6	EXP_RXP6
G7	VSS
G8	VSS
G9	VSS
G10	VSS
G11	VSS
G12	NC
G13	VSS
G14	RSV
G15	VSS
G16	RSV
G17	VSS
G18	HD45
G19	VSS
G20	VSS

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
G21	VTT
G22	VTT
G23	VSS
G24	HCPURST#
G25	HD26
G26	VSS
G27	VSS
G28	VSS
G29	HD20
G30	HA6#
G31	HREQ3#
G32	HA7#
G33	HD7
G34	HD5
G35	HD3
H1	EXP_TXP9
H2	VSS
H3	EXP_TXN8
H4	VSS
H5	VSS
H6	VSS
H7	EXP_RXN7
H8	EXP_RXP7
H9	VSS
H10	VSS
H11	EXP_RXN1
H12	NC
H13	VSS
H14	RSV
H15	NC
H16	BSEL0
H17	NC
H18	HD46

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
H19	HD41
H20	HD40
H21	VSS
H22	VTT
H23	HD37
H24	VSS
H25	VSS
H26	HDSTBP1#
H27	VSS
H28	HD19
H29	HA3#
H30	VSS
H31	HREQ2#
H32	VSS
H33	HD1
H34	VSS
H35	HD4
J1	EXP_TXN9
J2	VSS
J3	EXP_TXP10
J4	VSS
J5	EXP_RXN8
J6	EXP_RXP8
J7	VSS
J8	VSS
J9	VSS
J10	VSS
J11	EXP_RXP1
J12	NC
J13	RSV
J14	RSV
J15	VSS
J16	VSS

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Ball #	Signal Name
J17	VSS
J18	VSS
J19	HDSTBP2#
J20	VSS
J21	HD35
J22	HD32
J23	VSS
J24	HD33
J25	HD27
J26	HDINV1#
J27	HD21
J28	HA13#
J29	HA5#
J30	VSS
J31	HADSTB0#
J32	HRS2#
J33	HD0
J34	HD2
J35	HDEFER#
K1	EXP_TXP11
K2	VSS
K3	EXP_TXN10
K4	VSS
K5	VSS
K6	VSS
K7	EXP_RXN9
K8	EXP_RXP9
K9	VSS
K10	VSS
K11	VSS
K12	NC
K13	RSV
K14	VSS

Ball #	Signal Name
K15	RSV
K16	EXTTS#
K17	HD44
K18	HD43
K19	HDINV2#
K20	VSS
K21	HD39
K22	HD34
K23	HD31
K24	VSS
K25	HD28
K26	VSS
K27	HA14#
K28	VSS
K29	HA4#
K30	HA8#
K31	VSS
K32	VSS
K33	HA15#
K34	HRS0#
K35	VSS
L1	EXP_TXN11
L2	VSS
L3	EXP_TXP12
L4	VSS
L5	EXP_RXN10
L6	EXP_RXP10
L7	VSS
L8	VSS
L9	VSS
L10	VCC
L11	VSS
L12	NC

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
L13	VSS
L14	RSV
L15	VSS
L16	VSS
L17	VSS
L18	VSS
L19	NC
L20	VSS
L21	VSS
L22	VSS
L23	HD30
L24	VSS
L25	HD29
L26	HA18#
L27	VSS
L28	HA12#
L29	HA9#
L30	VSS
L31	HA11#
L32	VSS
L33	HLOCK#
L34	HHIT#
L35	HDBSY#
M1	EXP_TXP13
M2	VSS
M3	EXP_TXN12
M4	VSS
M5	VSS
M6	VSS
M7	EXP_RXN12
M8	EXP_RXP12
M9	VSS
M10	VSS

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
M11	VSS
M12	DREFCLKN
M13	DREFCLKP
M14	ICH_SYNC#
M15	RSV
M16	RSV
M17	VSS
M18	HD42
M19	HD38
M20	VSS
M21	HD36
M22	HCLKN
M23	HCLKP
M24	VSS
M25	VSS
M26	HA20#
M27	VSS
M28	HA16#
M29	VSS
M30	HA10#
M31	HADS#
M32	HDRDY#
M33	—
M34	VSS
M35	HBNR#
N1	EXP_TXN13
N2	VSS
N3	EXP_TXP14
N4	VSS
N5	EXP_RXN13
N6	EXP_RXP13
N7	VSS
N8	VSS

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
N9	VSS
N10	VSS
N11	VSS
N12	NC
N13	VCC
N14	VCC
N15	VCC
N16	VCC
N17	VSS
N18	VCC
N19	VSS
N20	VCC
N21	VCC
N22	NC
N23	NC
N24	NC
N25	VSS
N26	HA19#
N27	HADSTB1#
N28	VSS
N29	HA23#
N30	VSS
N31	HA21#
N32	VSS
N33	HA26#
N34	HTRDY#
N35	HHITM#
P1	EXP_TXP15
P2	VSS
P3	EXP_TXN14
P4	VSS
P5	VSS
P6	VSS

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
P7	EXP_RXP14
P8	EXP_RXN14
P9	VSS
P10	EXP_RXP11
P11	VSS
P12	NC
P13	VCC
P14	VCC
P15	VCC
P16	VSS
P17	VCC
P18	VSS
P19	VCC
P20	VSS
P21	VCC
P22	VCC
P23	NC
P24	NC
P25	VSS
P26	HA22#
P27	VSS
P28	HA24#
P29	VSS
P30	NC
P31	VSS
P32	VSS
P33	HEDRDY#
P34	HRS1#
P35	VSS
R1	EXP_TXN15
R2	VSS
R3	DMI_TXP0
R4	VSS

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Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
R5	EXP_RXN15
R6	EXP_RXP15
R7	VSS
R8	VSS
R9	VSS
R10	EXP_RXN11
R11	VSS
R12	NC
R13	VCC
R14	VCC
R15	VCC
R16	VCC
R17	VSS
R18	VCC
R19	VSS
R20	VCC
R21	VSS
R22	VCC
R23	VCC
R24	NC
R25	VSS
R26	VSS
R27	VSS
R28	HA25#
R29	HA17#
R30	SCB_A4
R31	SCB_A5
R32	SDQ_A58
R33	HBREQ0#
R34	SDQ_A59
R35	RSV
T1	DMI_TXP1
T2	VSS

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
T3	DMI_TXN0
T4	VSS
T5	VSS
T6	VSS
T7	VSS
T8	DMI_RXN1
T9	DMI_RXP1
T10	VSS
T11	VSS
T12	NC
T13	VCC
T14	VCC
T15	VCC
T16	VCC
T17	VCC
T18	VSS
T19	VCC
T20	VCC
T21	VCC
T22	VSS
T23	VCC
T24	VCC
T25	VSS
T26	HA30#
T27	HA27#
T28	VSS
T29	HA31#
T30	VSS
T31	HA28#
T32	VSS
T33	SDQ_A62
T34	VSS
T35	SDQ_A63

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
U1	DMI_TXN1
U2	VSS
U3	DMI_TXP2
U4	VSS
U5	DMI_RXP0
U6	DMI_RXN0
U7	VSS
U8	VSS
U9	VSS
U10	DMI_RXN3
U11	VSS
U12	NC
U13	VCC
U14	VCC
U15	VSS
U16	VCC
U17	VSS
U18	VCC
U19	VSS
U20	VCC
U21	VSS
U22	VCC
U23	VSS
U24	VCC
U25	VSS
U26	SDQ_B63
U27	VSS
U28	HA29#
U29	VSS
U30	SDQS_A8#
U31	VSS
U32	VSS
U33	SDM_A7

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
U34	SDQS_A7
U35	SDQS_A7#
V1	VSS
V2	VSS
V3	DMI_TXN2
V4	VSS
V5	DMI_TXP3
V6	VSS
V7	DMI_RXP2
V8	DMI_RXN2
V9	VSS
V10	DMI_RXP3
V11	VSS
V12	NC
V13	VCC
V14	VCC
V15	VCC
V16	VSS
V17	VCC
V18	VSS
V19	VCC
V20	VSS
V21	VCC
V22	VSS
V23	VCC
V24	VCC
V25	VSS
V26	VSS
V27	VSS
V28	SDQ_B58
V29	SDQ_B59
V30	SDQS_A8
V31	SCB_A1

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
V32	SCB_A0
V33	SDQ_A57
V34	SDQ_A56
V35	VSS
W1	VCC_EXP
W2	VCC_EXP
W3	VCC_EXP
W4	VCC_EXP
W5	DMI_TXN3
W6	VCC_EXP
W7	VCC_EXP
W8	VCC_EXP
W9	VCC_EXP
W10	EXP_COMPI
W11	VSS
W12	NC
W13	VCC
W14	VCC
W15	VSS
W16	VCC
W17	VSS
W18	VCC
W19	VSS
W20	VCC
W21	VSS
W22	VCC
W23	VSS
W24	VCC
W25	VSS
W26	SDQ_B62
W27	SDQS_B7
W28	VSS
W29	SDQ_B57

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
W30	VSS
W31	SDM_B7
W32	VSS
W33	SDQ_A61
W34	SDQ_A51
W35	SDQ_A60
Y1	VCC_EXP
Y2	VCC_EXP
Y3	VCC_EXP
Y4	VCC_EXP
Y5	VCC_EXP
Y6	VCC_EXP
Y7	VCC_EXP
Y8	VCC_EXP
Y9	VCC_EXP
Y10	EXP_COMPO
Y11	VSS
Y12	NC
Y13	VCC
Y14	VCC
Y15	VCC
Y16	VCC
Y17	VCC
Y18	VSS
Y19	VCC
Y20	VCC
Y21	VCC
Y22	VSS
Y23	VCC
Y24	VCC
Y25	VSS
Y26	SDQ_B60
Y27	VSS

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Ball #	Signal Name
Y28	SDQS_B7#
Y29	VSS
Y30	SCB_A6
Y31	VSS
Y32	VSS
Y33	SDQ_A50
Y34	VSS
Y35	SDQ_A55
AA1	VSS
AA2	VSS
AA3	VSS
AA4	VSS
AA5	VSS
AA6	VSS
AA7	VSS
AA8	VSS
AA9	VSS
AA10	VSS
AA11	VSS
AA12	NC
AA13	VCC
AA14	VCC
AA15	VSS
AA16	VCC
AA17	VSS
AA18	VCC
AA19	VSS
AA20	VCC
AA21	VCC
AA22	VCC
AA23	VCC
AA24	VCC
AA25	VSS

Ball #	Signal Name
AA26	VSS
AA27	VSS
AA28	SDQ_B56
AA29	SDQ_B61
AA30	SCB_A3
AA31	SCB_A2
AA32	SDQ_A54
AA33	SDM_A6
AA34	SDQS_A6
AA35	SDQS_A6#
AB1	VCC
AB2	VCC
AB3	VCC
AB4	VCC
AB5	VCC
AB6	VCC
AB7	VCC
AB8	VCC
AB9	VCC
AB10	VCC
AB11	VCC
AB12	NC
AB13	VCC
AB14	VCC
AB15	VCC
AB16	VCC
AB17	VCC
AB18	VCC
AB19	VCC
AB20	VCC
AB21	VCC
AB22	VCC
AB23	VCC

Ball #	Signal Name
AB24	VCC
AB25	VSS
AB26	SDQ_B51
AB27	SDQ_B55
AB28	VSS
AB29	SCB_A7
AB30	VSS
AB31	SDQS_B6
AB32	VSS
AB33	RSV
AB34	SCLK_A5#
AB35	VSS
AC1	VCC
AC2	VCC
AC3	VCC
AC4	VCC
AC5	VCC
AC6	VCC
AC7	VCC
AC8	VCC
AC9	VCC
AC10	VCC
AC11	VCC
AC12	RSV
AC13	RSV
AC14	RSV
AC15	RSV
AC16	RSV
AC17	RSV
AC18	RSV
AC19	RSV
AC20	RSV
AC21	RSV

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AC22	RSV
AC23	NC
AC24	NC
AC25	VSS
AC26	SDQ_B50
AC27	VSS
AC28	SDQ_B54
AC29	VSS
AC30	SDQS_B6#
AC31	VSS
AC32	VSS
AC33	SCLK_A5
AC34	SCLK_A2
AC35	SCLK_A2#
AD1	VCC
AD2	VCC
AD3	VCC
AD4	VCC
AD5	VCC
AD6	VCC
AD7	VCC
AD8	VCC
AD9	VCC
AD10	VCC
AD11	VSS
AD12	SDQ_B20
AD13	VSS
AD14	SDQ_B17
AD15	SDQ_B29
AD16	VSS
AD17	SDQ_A29
AD18	SDQ_B24
AD19	VSS

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AD20	VSS
AD21	NC
AD22	VSS
AD23	SDQ_B37
AD24	SDM_B6
AD25	VSS
AD26	VSS
AD27	SDQ_A35
AD28	SCLK_B5
AD29	SCLK_B5#
AD30	NC
AD31	SDQ_A48
AD32	RSV
AD33	—
AD34	VSS
AD35	SDQ_A49
AE1	SDQ_A5
AE2	SDQ_A4
AE3	SDQ_A0
AE4	VSS
AE5	SOCOMP1
AE6	VSS
AE7	SVREF0
AE8	SVREF1
AE9	VSS
AE10	SM_SLEWOUT1
AE11	SDQ_B4
AE12	VSS
AE13	SDQ_B21
AE14	SDQ_B19
AE15	SDQ_A28
AE16	RSV_TP0
AE17	SDQ_A24

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AE18	NC
AE19	SDQ_B25
AE20	SDM_B3
AE21	VSS
AE22	VSS
AE23	VSS
AE24	VSS
AE25	SCLK_B2#
AE26	SCLK_B2
AE27	SDQ_B49
AE28	VSS
AE29	SDQ_B53
AE30	NC
AE31	SDQ_B52
AE32	VSS
AE33	SDQ_A43
AE34	SDQ_A53
AE35	SDQ_A52
AF1	VSS
AF2	SDM_A0
AF3	SDQ_A1
AF4	VSS
AF5	SOCOMP0
AF6	VSS
AF7	RSTIN#
AF8	VSS
AF9	SM_SLEWIN1
AF10	VSS
AF11	SDQ_B5
AF12	SDQ_B11
AF13	SDQ_B16
AF14	SDQ_B18
AF15	SDQ_B28

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Ball #	Signal Name
AF16	SDQ_A25
AF17	SDM_A3
AF18	VSS
AF19	NC
AF20	SDQS_B3#
AF21	VSS
AF22	NC
AF23	SDQ_B36
AF24	SDQ_B32
AF25	SDM_B4
AF26	VSS
AF27	SDQ_B48
AF28	SDQ_A39
AF29	VSS
AF30	SDQ_B43
AF31	VSS
AF32	VSS
AF33	SDQ_A42
AF34	SDQ_A47
AF35	VSS
AG1	SDQS_A0
AG2	SDQS_A0#
AG3	SDQ_A6
AG4	SRCOMP0
AG5	VSS
AG6	NC
AG7	PWROK
AG8	SRCOMP1
AG9	VSS
AG10	SDQ_B1
AG11	SDQ_B0
AG12	VSS
AG13	VSS

Ball #	Signal Name
AG14	SDQS_B2#
AG15	VSS
AG16	VSS
AG17	SDQS_A3#
AG18	VSS
AG19	VSS
AG20	SDQS_B3
AG21	VSS
AG22	VSS
AG23	SCLK_B0#
AG24	SDQ_B33
AG25	NC
AG26	SDQS_B4#
AG27	SDQ_A38
AG28	SDQ_B47
AG29	NC
AG30	SDQ_B46
AG31	SDQ_B42
AG32	SDQ_A46
AG33	SDQS_A5#
AG34	SDM_A5
AG35	SDQS_A5
AH1	VSS
AH2	SDQ_A7
AH3	SDQ_A2
AH4	SDQ_B12
AH5	NC
AH6	VSS
AH7	SDQ_B7
AH8	SDQS_B0
AH9	SDQS_B0#
AH10	SDM_B0
AH11	VSS

Ball #	Signal Name
AH12	SDM_B2
AH13	SDQS_B2
AH14	VSS
AH15	RSV_TP1
AH16	SDQS_A3
AH17	SDQ_A27
AH18	VSS
AH19	SDQ_B30
AH20	VSS
AH21	SDQ_B31
AH22	VSS
AH23	SCLK_B0
AH24	NC
AH25	SDQS_B4
AH26	VSS
AH27	SDQ_A34
AH28	SDQS_B5
AH29	VSS
AH30	SDQS_B5#
AH31	SDM_B5
AH32	VSS
AH33	VSS
AH34	SDQ_A40
AH35	SDQ_A41
AJ1	SDQ_A12
AJ2	SDQ_A3
AJ3	SDQ_A13
AJ4	VSS
AJ5	SDQ_B13
AJ6	SDQ_B3
AJ7	SDQ_B2
AJ8	SDQ_B6
AJ9	VSS

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AJ10	VSS
AJ11	SCLK_B4
AJ12	SM_SLEWIN0
AJ13	VSS
AJ14	NC
AJ15	VSS
AJ16	VSS
AJ17	SDQ_A31
AJ18	SCB_B1
AJ19	VSS
AJ20	SCB_B0
AJ21	SDQS_B8#
AJ22	VSS
AJ23	SCB_B2
AJ24	SCB_B3
AJ25	SDQ_B39
AJ26	SDQ_B35
AJ27	VSS
AJ28	SDQS_A4#
AJ29	SDQ_B44
AJ30	VSS
AJ31	SDQ_B41
AJ32	VSS
AJ33	SDM_A4
AJ34	SDQ_A45
AJ35	VSS
AK1	VSS
AK2	SDQ_A8
AK3	SDQ_A9
AK4	VSS
AK5	SDM_B1
AK6	VSS
AK7	SDQ_A17

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AK8	VSS
AK9	SCLK_B1
AK10	SDQ_B8
AK11	VSS
AK12	SM_SLEWOUT0
AK13	SDQ_B22
AK14	VSS
AK15	RSV_TP3
AK16	SDQ_A30
AK17	VSS
AK18	SCB_B5
AK19	SDQ_B27
AK20	VSS
AK21	SDQS_B8
AK22	SCLK_B3#
AK23	VSS
AK24	NC
AK25	VSS
AK26	VSS
AK27	SDQS_A4
AK28	SCLK_A3#
AK29	SDQ_A32
AK30	VSS
AK31	SDQ_A33
AK32	SDQ_B40
AK33	SDQ_B45
AK34	SDQ_A44
AK35	VCCSM
AL1	SDM_A1
AL2	SDQS_A1#
AL3	SDQS_A1
AL4	SDQ_B9
AL5	SDQS_B1#

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AL6	SDQ_B14
AL7	SDQ_A19
AL8	SDQ_B10
AL9	SCLK_B1#
AL10	VSS
AL11	SCLK_B4#
AL12	VCCSM
AL13	VSS
AL14	SDQ_B23
AL15	RSV_TP2
AL16	VSS
AL17	SDQ_A26
AL18	SDQ_B26
AL19	VSS
AL20	SCB_B4
AL21	SCB_B6
AL22	SCB_B7
AL23	SCLK_B3
AL24	VSS
AL25	SDQ_B38
AL26	SDQ_B34
AL27	NC
AL28	SCLK_A3
AL29	SCLK_A0
AL30	SDQ_A36
AL31	SDQ_A37
AL32	VSS
AL33	SODT_B3
AL34	SODT_B1
AL35	SODT_B2
AM1	—
AM2	SCLK_A4#
AM3	SCLK_A4

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Ball #	Signal Name
AM4	VSS
AM5	SDQS_B1
AM6	VSS
AM7	SDQ_A22
AM8	SDQ_A23
AM9	SDQ_A18
AM10	VCCSM
AM11	VCCSM
AM12	NC
AM13	VCCSM
AM14	VCCSM
AM15	NC
AM16	VCCSM
AM17	VCCSM
AM18	NC
AM19	VCCSM
AM20	VCCSM
AM21	NC
AM22	VCCSM
AM23	VCCSM
AM24	NC
AM25	VCCSM
AM26	VCCSM
AM27	VCCSM
AM28	VSS
AM29	VCCSM
AM30	SCLK_A0#
AM31	VSS
AM32	VCCSM
AM33	SCS_B1#
AM34	SMA_B13
AM35	—
AN1	VSS

Ball #	Signal Name
AN2	SCLK_A1
AN3	SCLK_A1#
AN4	SDQ_A10
AN5	SDQ_A21
AN6	SDQ_B15
AN7	SDQS_A2#
AN8	SCKE_B3
AN9	SBS_B2
AN10	SMA_B12
AN11	SMA_B5
AN12	—
AN13	SMA_B4
AN14	SMA_B2
AN15	SMA_B0
AN16	SBS_B1
AN17	SRAS_B#
AN18	SCKE_A2
AN19	SCKE_A1
AN20	SMA_A12
AN21	SMA_A7
AN22	SMA_A5
AN23	SMA_A8
AN24	—
AN25	SMA_A2
AN26	SMA_A0
AN27	SBS_A0
AN28	SWE_A#
AN29	SODT_A2
AN30	SMA_A13
AN31	SCS_A1#
AN32	SODT_A3
AN33	SCS_B2#
AN34	SODT_B0

Ball #	Signal Name
AN35	VCCSM
AP1	NC
AP2	SDQ_A14
AP3	SDQ_A15
AP4	SDQ_A11
AP5	SDQ_A16
AP6	SDM_A2
AP7	SDQS_A2
AP8	VCCSM
AP9	SCKE_B1
AP10	SMA_B11
AP11	SMA_B9
AP12	VCCSM
AP13	SMA_B6
AP14	SMA_B3
AP15	SMA_B10
AP16	VCCSM
AP17	SWE_B#
AP18	SCAS_B#
AP19	SCKE_A0
AP20	VCCSM
AP21	SMA_A11
AP22	SMA_A9
AP23	SMA_A4
AP24	VCCSM
AP25	SMA_A1
AP26	SMA_A10
AP27	SRAS_A#
AP28	VCCSM
AP29	SCAS_A#
AP30	SODT_A0
AP31	SCS_A3#
AP32	SODT_A1

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AP33	SCS_B0#
AP34	SCS_B3#
AP35	NC
AR1	NC
AR2	NC
AR3	VSS
AR4	—
AR5	SDQ_A20
AR6	VSS
AR7	VCCSM
AR8	SCKE_B2
AR9	SCKE_B0
AR10	VCCSM

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AR11	SMA_B7
AR12	SMA_B8
AR13	VSS
AR14	VCCSM
AR15	SMA_B1
AR16	SBS_B0
AR17	VSS
AR18	VCCSM
AR19	SCKE_A3
AR20	SBS_A2
AR21	VSS
AR22	VCCSM
AR23	SMA_A6

Table 12-2. MCH Ballout Sorted By Ball Number

Ball #	Signal Name
AR24	SMA_A3
AR25	VSS
AR26	VCCSM
AR27	SBS_A1
AR28	SCS_A2#
AR29	SCS_A0#
AR30	VSS
AR31	VCCSM
AR32	—
AR33	VCCSM
AR34	NC
AR35	NC

12.2   Package Information

The MCH package measures 37.5 mm $\times$ 37.5 mm. The 1210 balls are located in a non-grid pattern. For example, the ball pitch varies from 31.8 mils to 43.0 mils, depending on the X-axis or Y-axis direction. Figure 12-3 shows the physical dimensions of the package and **Error! Reference source not found.** shows the MCH keep-out regions.

Figure 12-3. MCH Package Dimensions
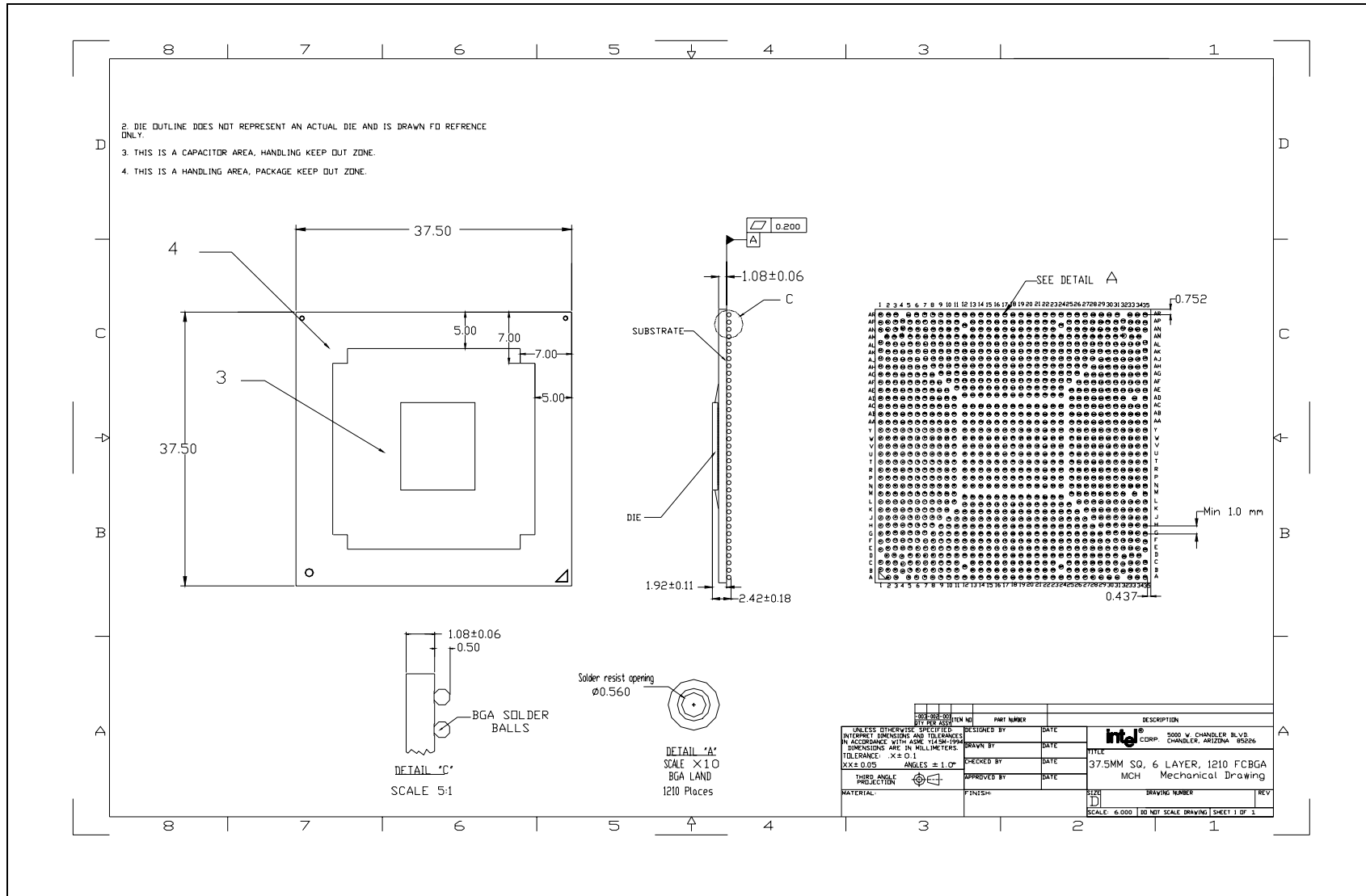
13   *Testability*

In the 82925X MCH, testability for Automated Test Equipment (ATE) board level testing has been implemented as an XOR chain. An XOR-tree is a chain of XOR gates each with one input pin connected to it.

13.1   Complimentary Pins

Table 13-1 contains pins which must remain complimentary while performing XOR testing. The first and third columns contain the pin and its compliment. The second and fourth columns specify which chain the associated pins are on.

Note: In non ECC systems, SDQS_A8, SDQS_A8#, SDQS_B8 and SDQS_B8# do not need to be driven.

Table 13-1. Complimentary Pins to Drive

Complimentary Pin	XOR Chain	Complimentary Pin	XOR Chain
SDQS_A0	SM XOR 6	SDQS_A0#	SM XOR 4
SDQS_A1	SM XOR 6	SDQS_A1#	SM XOR 4
SDQS_A2	SM XOR 6	SDQS_A2#	SM XOR 4
SDQS_A3	SM XOR 4	SDQS_A3#	SM XOR 6
SDQS_A4	SM XOR 4	SDQS_A4#	SM XOR 2
SDQS_A5	SM XOR 2	SDQS_A5#	SM XOR 4
SDQS_A6	SM XOR 2	SDQS_A6#	SM XOR 4
SDQS_A7	SM XOR 2	SDQS_A7#	SM XOR 4
SDQS_A8	SM XOR 2	SDQS_A8#	SM XOR 4
SDQS_B0	SM XOR 7	SDQS_B0#	SM XOR 5
SDQS_B1	SM XOR 7	SDQS_B1#	SM XOR 5
SDQS_B2	SM XOR 7	SDQS_B2#	SM XOR 5
SDQS_B3	SM XOR 7	SDQS_B3#	SM XOR 5
SDQS_B4	SM XOR 7	SDQS_B4#	SM XOR 5
SDQS_B5	SM XOR 3	SDQS_B5#	SM XOR 5
SDQS_B6	SM XOR 3	SDQS_B6#	SM XOR 5
SDQS_B7	SM XOR 3	SDQS_B7#	SM XOR 5
SDQS_B8	SM XOR 7	SDQS_B8#	SM XOR 5

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13.2   XOR Test Mode Initialization

XOR test mode can be entered by pulling reserved ballout RSV (located at F15) and MTYPE low through the de-assertion of external reset (RSTIN#). It is recommended that customers use the following sequence.

After power up, hold PWROK, PCIRST#, and reserved ballout RSV (located at F15) and MTYPE low and start external clocks. After 20 cycles, pull PWROK high. After 15 clocks, de-assert PCIRST# (pull it high). Release reserved ballout RSV (located at F15) and MTYPE. No external drive. Allow the clocks to run for an additional 32 clocks. Begin testing the XOR chains.

13.3   XOR Chain Definition

The 82925X MCH has 10 XOR chains. The XOR chain outputs are driven out on the following output pins. During full-width testing, XOR chain outputs will be visible on both pins. For example xor_out0 will be visible on BSEL2.

Table 13-2. XOR Chain Outputs

XOR Chain	Output Pins	Coordinate Location
xor_out0	BSEL2	D17
xor_out1	RSV	M16
xor_out2	RSV	F15
xor_out3	MTYPE	C15
xor_out4	RSV	A16
xor_out5	RSV	B15
xor_out6	RSV	C14
xor_out7	RSV	K15
xor_out8	BSEL1	E15
xor_out9	BSEL0	H16

13.4   XOR Chains

The following tables show the XOR chains. The last section in this chapter has a pin exclusion list. The chain files are golden, if there is a pin missing from the chain files and exclusion list, it should be added to the exclusion list.

Table 13-3. XOR Chain #0

Chain	Pin Count	Ball Number	Signal Name
0	1	M14	ICH_SYNC#
0	2	K16	EXTTS#
0	3	G24	HCPURST#
0	4	K17	HD44
0	5	M18	HD42
0	6	K18	HD43
0	7	F17	HD47
0	8	M19	HD38
0	9	K21	HD39
0	10	K19	HDINV2#
0	11	H18	HD46
0	12	J19	HDSTBP2#
0	13	F19	HDSTBN2#
0	14	G18	HD45
0	15	K22	HD34
0	16	M21	HD36
0	17	J21	HD35
0	18	H20	HD40
0	19	H19	HD41
0	20	J24	HD33
0	21	J22	HD32
0	22	H23	HD37
0	23	A25	HD48
0	24	A29	HD55
0	25	D27	HD60
0	26	B26	HDINV3#
0	27	B29	HDSTBP3#
0	28	C29	HDSTBN3#
0	29	C25	HD58
0	30	B30	HD51
0	31	E27	HD24
0	32	C30	HD17
0	33	E25	HD25
0	34	H28	HD19

Chain	Pin Count	Ball Number	Signal Name
0	35	F27	HD23
0	36	F28	HD22
0	37	H26	HDSTBP1#
0	38	F26	HDSTBN1#
0	39	J27	HD21
0	40	J25	HD27
0	41	K25	HD28
0	42	K23	HD31
0	43	L23	HD30
0	44	J26	HDINV1#
0	45	G25	HD26
0	46	L25	HD29
0	47	B32	HD15
0	48	G33	HD7
0	49	H33	HD1
0	50	H35	HD4
0	51	J34	HD2
0	52	G30	HA6#
0	53	H29	HA3#
0	54	J28	HA13#
0	55	J29	HA5#
0	56	K33	HA15#
0	57	F31	HREQ4#
0	58	K29	HA4#
0	59	L31	HA11#
0	60	K27	HA14#
0	61	M30	HA10#
0	62	F33	HREQ0#
0	63	E30	HBPRI#
0	64	J35	HDEFER#
0	65	P33	HEDRDY#
XOR Chain #0 Output		**D17**	**BSEL2**

Table 13-4. XOR Chain #1

Chain	Pin Count	Ball Number	Signal Name
1	1	A28	HD57
1	2	A27	HD61
1	3	B27	HD54
1	4	B25	HD63
1	5	E24	HD62
1	6	C26	HD59
1	7	C27	HD49
1	8	C28	HD56
1	9	A31	HD53
1	10	C31	HD50
1	11	B31	HD52
1	12	D29	HD18
1	13	E28	HD16
1	14	G29	HD20
1	15	B34	HD11
1	16	B33	HD13
1	17	C32	HD14
1	18	C33	HD9
1	19	C34	HD12
1	20	D34	HD8
1	21	D33	HD10
1	22	E34	HDINV0#
1	23	E33	HDSTBP0#
1	24	E35	HDSTBN0#
1	25	F34	HD6
1	26	G34	HD5
1	27	G35	HD3
1	28	J33	HD0
1	29	G32	HA7#
1	30	H31	HREQ2#
1	31	K30	HA8#
1	32	J31	HADSTB0#
1	33	G31	HREQ3#
1	34	E31	HPCREQ#

Chain	Pin Count	Ball Number	Signal Name
1	35	L29	HA9#
1	36	L28	HA12#
1	37	J32	HRS2#
1	38	K34	HRS0#
1	39	L33	HLOCK#
1	40	M32	HDRDY#
1	41	M31	HADS#
1	42	L34	HHIT#
1	43	M35	HBNR#
1	44	L35	HDBSY#
1	45	N35	HHITM#
1	46	P34	HRS1#
1	47	N34	HTRDY#
1	48	R33	HBREQ0#
1	49	N31	HA21#
1	50	N33	HA26#
1	51	T31	HA28#
1	52	E32	HREQ1#
1	53	T27	HA27#
1	54	M26	HA20#
1	55	N26	HA19#
1	56	P28	HA24#
1	57	U28	HA29#
1	58	N27	HADSTB1#
1	59	L26	HA18#
1	60	M28	HA16#
1	61	T29	HA31#
1	62	R28	HA25#
1	63	N29	HA23#
1	64	T26	HA30#
1	65	P26	HA22#
1	66	R29	HA17#
XOR Chain #1 Output		**M16**	**RSV_M16**

Table 13-5. XOR Chain #2

Chain	Pin Count	Ball Number	Signal Name
2	1	R32	SDQ_A58
2	2	R34	SDQ_A59
2	3	T35	SDQ_A63
2	4	W35	SDQ_A60
2	5	T33	SDQ_A62
2	6	V34	SDQ_A56
2	7	V33	SDQ_A57
2	8	U33	SDM_A7
2	9	W33	SDQ_A61
2	10	U34	SDQS_A7
2	11	V30	SDQS_A8
2	12	AA31	SCB_A2
2	13	AA30	SCB_A3
2	14	Y30	SCB_A6
2	15	AB29	SCB_A7
2	16	V31	SCB_A1
2	17	V32	SCB_A0
2	18	R31	SCB_A5
2	19	R30	SCB_A4
2	20	AA34	SDQS_A6
2	21	W34	SDQ_A51
2	22	Y35	SDQ_A55
2	23	Y33	SDQ_A50
2	24	AD35	SDQ_A49
2	25	AE35	SDQ_A52
2	26	AE34	SDQ_A53
2	27	AA33	SDM_A6
2	28	AA32	SDQ_A54
2	29	AD31	SDQ_A48
2	30	AC35	SCLK_A2#
2	31	AB34	SCLK_A5#
2	32	AC33	SCLK_A5
2	33	AF34	SDQ_A47
2	34	AH35	SDQ_A41

Chain	Pin Count	Ball Number	Signal Name
2	35	AJ34	SDQ_A45
2	36	AG34	SDM_A5
2	37	AE33	SDQ_A43
2	38	AF33	SDQ_A42
2	39	AG32	SDQ_A46
2	40	AH34	SDQ_A40
2	41	AK34	SDQ_A44
2	42	AG35	SDQS_A5
2	43	AR29	SCS_A0#
2	44	AN32	SODT_A3
2	45	AN29	SODT_A2
2	46	AP32	SODT_A1
2	47	AP30	SODT_A0
2	48	AJ28	SDQS_A4#
XOR Chain #2 Output		**F15**	**RSV_F15**

Table 13-6. XOR Chain #3

Chain	Pin Count	Ball Number	Signal Name
3	1	W26	SDQ_B62
3	2	U26	SDQ_B63
3	3	V28	SDQ_B58
3	4	V29	SDQ_B59
3	5	W29	SDQ_B57
3	6	W31	SDM_B7
3	7	AA29	SDQ_B61
3	8	AA28	SDQ_B56
3	9	Y26	SDQ_B60
3	10	W27	SDQS_B7
3	11	AB31	SDQS_B6
3	12	AB27	SDQ_B55
3	13	AE31	SDQ_B52
3	14	AC26	SDQ_B50
3	15	AE27	SDQ_B49
3	16	AE29	SDQ_B53
3	17	AF27	SDQ_B48
3	18	AB26	SDQ_B51
3	19	AC28	SDQ_B54
3	20	AD24	SDM_B6
3	21	AN33	SCS_B2#
3	22	AD29	SCLK_B5#
3	23	AE25	SCLK_B2#
3	24	AE26	SCLK_B2
3	25	AP34	SCS_B3#
3	26	AP33	SCS_B0#
3	27	AM33	SCS_B1#
3	28	AL33	SODT_B3
3	29	AL34	SODT_B1
3	30	AL35	SODT_B2
3	31	AN34	SODT_B0
3	32	AF30	SDQ_B43
3	33	AK32	SDQ_B40
3	34	AH31	SDM_B5

Chain	Pin Count	Ball Number	Signal Name
3	35	AK33	SDQ_B45
3	36	AJ31	SDQ_B41
3	37	AG28	SDQ_B47
3	38	AJ29	SDQ_B44
3	39	AG31	SDQ_B42
3	40	AH28	SDQS_B5
3	41	AM34	SMA_B13
3	42	AJ25	SDQ_B39
3	43	AL25	SDQ_B38
3	44	AJ26	SDQ_B35
3	45	AL26	SDQ_B34
3	46	AF23	SDQ_B36
3	47	AG24	SDQ_B33
XOR Chain #3 Output		**C15**	**MTYPE**

Table 13-7. XOR Chain #4

Chain	Pin Count	Ball Number	Signal Name
4	1	U35	SDQS_A7#
4	2	U30	SDQS_A8#
4	3	AA35	SDQS_A6#
4	4	AC34	SCLK_A2
4	5	AG33	SDQS_A5#
4	6	AN31	SCS_A1#
4	7	AP31	SCS_A3#
4	8	AK27	SDQS_A4
4	9	AD27	SDQ_A35
4	10	AL30	SDQ_A36
4	11	AJ33	SDM_A4
4	12	AK31	SDQ_A33
4	13	AF28	SDQ_A39
4	14	AH27	SDQ_A34
4	15	AG27	SDQ_A38
4	16	AL31	SDQ_A37
4	17	AK29	SDQ_A32
4	18	AP29	SCAS_A#
4	19	AN28	SWE_A#
4	20	AR28	SCS_A2#
4	21	AR27	SBS_A1
4	22	AP27	SRAS_A#
4	23	AN27	SBS_A0
4	24	AM30	SCLK_A0#
4	25	AL29	SCLK_A0
4	26	AL28	SCLK_A3
4	27	AK28	SCLK_A3#
4	28	AN25	SMA_A2
4	29	AP26	SMA_A10
4	30	AN26	SMA_A0
4	31	AN30	SMA_A13
4	32	AP25	SMA_A1
4	33	AP23	SMA_A4
4	34	AR24	SMA_A3

Chain	Pin Count	Ball Number	Signal Name
4	35	AR23	SMA_A6
4	36	AN23	SMA_A8
4	37	AH16	SDQS_A3
4	38	AH17	SDQ_A27
4	39	AL17	SDQ_A26
4	40	AF16	SDQ_A25
4	41	AE17	SDQ_A24
4	42	AD17	SDQ_A29
4	43	AN18	SCKE_A2
4	44	AN7	SDQS_A2#
4	45	AN3	SCLK_A1#
4	46	AL2	SDQS_A1#
4	47	AG2	SDQS_A0#
XOR Chain #4 Output		**A16**	**RSV_A16**

Table 13-8. XOR Chain #5

Chain	Pin Count	Ball Number	Signal Name
5	1	Y28	SDQS_B7#
5	2	AC30	SDQS_B6#
5	3	AD28	SCLK_B5
5	4	AG30	SDQ_B46
5	5	AH30	SDQS_B5#
5	6	AF25	SDM_B4
5	7	AD23	SDQ_B37
5	8	AF24	SDQ_B32
5	9	AG26	SDQS_B4#
5	10	AF20	SDQS_B3#
5	11	AH19	SDQ_B30
5	12	AD15	SDQ_B29
5	13	AD18	SDQ_B24
5	14	AE20	SDM_B3
5	15	AK19	SDQ_B27
5	16	AH21	SDQ_B31
5	17	AL18	SDQ_B26
5	18	AF15	SDQ_B28
5	19	AE19	SDQ_B25
5	20	AK22	SCLK_B3#
5	21	AG23	SCLK_B0#
5	22	AH23	SCLK_B0
5	23	AL21	SCB_B6
5	24	AK18	SCB_B5
5	25	AJ23	SCB_B2
5	26	AB29	SCB_A7
5	27	AJ24	SCB_B3
5	28	AL20	SCB_B4
5	29	AJ20	SCB_B0
5	30	AJ18	SCB_B1
5	31	AJ21	SDQS_B8#
5	32	AN17	SRAS_B#
5	33	AP18	SCAS_B#
5	34	AP17	SWE_B#

Chain	Pin Count	Ball Number	Signal Name
5	35	AR16	SBS_B0
5	36	AN16	SBS_B1
5	37	AN14	SMA_B2
5	38	AN15	SMA_B0
5	39	AP15	SMA_B10
5	40	AR15	SMA_B1
5	41	AP14	SMA_B3
5	42	AN13	SMA_B4
5	43	AR9	SCKE_B0
5	44	AG14	SDQS_B2#
5	45	AL9	SCLK_B1#
5	46	AL5	SDQS_B1#
5	47	AH9	SDQS_B0#
XOR Chain #5 Output		**B15**	**RSV_B15**

Table 13-9. XOR Chain #6

Chain	Pin Count	Ball Number	Signal Name
6	1	AG17	SDQS_A3#
6	2	AF17	SDM_A3
6	3	AJ17	SDQ_A31
6	4	AK16	SDQ_A30
6	5	AE15	SDQ_A28
6	6	AN19	SCKE_A1
6	7	AP21	SMA_A11
6	8	AP22	SMA_A9
6	9	AN22	SMA_A5
6	10	AR20	SBS_A2
6	11	AN21	SMA_A7
6	12	AN20	SMA_A12
6	13	AP19	SCKE_A0
6	14	AR19	SCKE_A3
6	15	AP7	SDQS_A2
6	16	AM9	SDQ_A18
6	17	AL7	SDQ_A19
6	18	AM8	SDQ_A23
6	19	AM7	SDQ_A22
6	20	AP6	SDM_A2
6	21	AK7	SDQ_A17
6	22	AP5	SDQ_A16
6	23	AN5	SDQ_A21
6	24	AR5	SDQ_A20
6	25	AM2	SCLK_A4#
6	26	AM3	SCLK_A4
6	27	AN2	SCLK_A1
6	28	AP4	SDQ_A11
6	29	AP3	SDQ_A15
6	30	AP2	SDQ_A14
6	31	AN4	SDQ_A10
6	32	AK3	SDQ_A9
6	33	AK2	SDQ_A8
6	34	AJ3	SDQ_A13

Chain	Pin Count	Ball Number	Signal Name
6	35	AJ1	SDQ_A12
6	36	AL1	SDM_A1
6	37	AL3	SDQS_A1
6	38	AG1	SDQS_A0
6	39	AG3	SDQ_A6
6	40	AF2	SDM_A0
6	41	AH2	SDQ_A7
6	42	AH3	SDQ_A2
6	43	AJ2	SDQ_A3
6	44	AF3	SDQ_A1
6	45	AE3	SDQ_A0
6	46	AE2	SDQ_A4
6	47	AE1	SDQ_A5
XOR Chain #6 Output		**C14**	**RSV_C14**

Table 13-10. XOR Chain #7

Chain	Pin Count	Ball Number	Signal Name
7	1	AH25	SDQS_B4
7	2	AG20	SDQS_B3
7	3	AL23	SCLK_B3
7	4	AK21	SDQS_B8
7	5	AP13	SMA_B6
7	6	AP11	SMA_B9
7	7	AR12	SMA_B8
7	8	AR11	SMA_B7
7	9	AN10	SMA_B12
7	10	AP10	SMA_B11
7	11	AN9	SBS_B2
7	12	AN11	SMA_B5
7	13	AR8	SCKE_B2
7	14	AP9	SCKE_B1
7	15	AN8	SCKE_B3
7	16	AE14	SDQ_B19
7	17	AF14	SDQ_B18
7	18	AK13	SDQ_B22
7	19	AH12	SDM_B2
7	20	AD14	SDQ_B17
7	21	AL14	SDQ_B23
7	22	AD12	SDQ_B20
7	23	AF13	SDQ_B16
7	24	AE13	SDQ_B21
7	25	AH13	SDQS_B2
7	26	AL11	SCLK_B4#
7	27	AJ11	SCLK_B4
7	28	AK9	SCLK_B1
7	29	AL4	SDQ_B9
7	30	AJ5	SDQ_B13
7	31	AH4	SDQ_B12
7	32	AK10	SDQ_B8
7	33	AL8	SDQ_B10
7	34	AN6	SDQ_B15

Chain	Pin Count	Ball Number	Signal Name
7	35	AL6	SDQ_B14
7	36	AK5	SDM_B1
7	37	AF12	SDQ_B11
7	38	AM5	SDQS_B1
7	39	AH8	SDQS_B0
7	40	AE11	SDQ_B4
7	41	AF11	SDQ_B5
7	42	AG10	SDQ_B1
7	43	AJ7	SDQ_B2
7	44	AJ6	SDQ_B3
7	45	AJ8	SDQ_B6
7	46	AH10	SDM_B0
7	47	AG11	SDQ_B0
7	48	AH7	SDQ_B7
XOR Chain #7 Output		**K15**	**RSV_K15**

Table 13-11. XOR Chain #8

Chain	Pin Count	Ball Number	Signal Name
8	1	F11	EXP_RXN0
8	2	C9	EXP_TXN0
8	3	H11	EXP_RXN1
8	4	A8	EXP_TXN1
8	5	E9	EXP_RXN2
8	6	C7	EXP_TXN2
8	7	E7	EXP_RXN3
8	8	A6	EXP_TXN3
8	9	B4	EXP_RXN4
8	10	C5	EXP_TXN4
8	11	E5	EXP_RXN5
8	12	D2	EXP_TXN5
8	13	G5	EXP_RXN6
8	14	F3	EXP_TXN6
8	15	H7	EXP_RXN7
8	16	G1	EXP_TXN7
8	17	J5	EXP_RXN8
8	18	H3	EXP_TXN8
8	19	K7	EXP_RXN9
8	20	J1	EXP_TXN9
8	21	L5	EXP_RXN10
8	22	K3	EXP_TXN10
8	23	R10	EXP_RXN11
8	24	L1	EXP_TXN11
8	25	M7	EXP_RXN12
8	26	M3	EXP_TXN12
8	27	N5	EXP_RXN13
8	28	N1	EXP_TXN13
8	29	P8	EXP_RXN14
8	30	P3	EXP_TXN14
8	31	R5	EXP_RXN15
8	32	R1	EXP_TXN15
8	33	E11	EXP_RXP0
8	34	C10	EXP_TXP0

Chain	Pin Count	Ball Number	Signal Name
8	35	J11	EXP_RXP1
8	36	A9	EXP_TXP1
8	37	F9	EXP_RXP2
8	38	C8	EXP_TXP2
8	39	F7	EXP_RXP3
8	40	A7	EXP_TXP3
8	41	B3	EXP_RXP4
8	42	C6	EXP_TXP4
8	43	D5	EXP_RXP5
8	44	C2	EXP_TXP5
8	45	G6	EXP_RXP6
8	46	E3	EXP_TXP6
8	47	H8	EXP_RXP7
8	48	F1	EXP_TXP7
8	49	J6	EXP_RXP8
8	50	G3	EXP_TXP8
8	51	K8	EXP_RXP9
8	52	H1	EXP_TXP9
8	53	L6	EXP_RXP10
8	54	J3	EXP_TXP10
8	55	P10	EXP_RXP11
8	56	K1	EXP_TXP11
8	57	M8	EXP_RXP12
8	58	L3	EXP_TXP12
8	59	N6	EXP_RXP13
8	60	M1	EXP_TXP13
8	61	P7	EXP_RXP14
8	62	N3	EXP_TXP14
8	63	R6	EXP_RXP15
8	64	P1	EXP_TXP15
XOR Chain #8 Output		**E15**	**BSEL1**

Table 13-12. XOR Chain #9

Chain	Pin Count	Ball Number	Signal Name
9	1	U6	DMI_RXN0
9	2	U5	DMI_RXP0
9	3	T3	DMI_TXN0
9	4	R3	DMI_TXP0
9	5	T8	DMI_RXN1
9	6	T9	DMI_RXP1
9	7	U1	DMI_TXN1
9	8	T1	DMI_TXP1
9	9	V8	DMI_RXN2
9	10	V7	DMI_RXP2
9	11	V3	DMI_TXN2
9	12	U3	DMI_TXP2
9	13	U10	DMI_RXN3
9	14	V10	DMI_RXP3
9	15	W5	DMI_TXN3
9	16	V5	DMI_TXP3
XOR Chain #9 Output		**H16**	**BSEL0**

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13.5 Pads Excluded from XOR Mode(s)

A large number of pads do not support XOR testing. The majority of the pads that fall into this category are analog related pins. refer to the Table 13-13.

Table 13-13. XOR Pad Exclusion List

3GIO	FSB	SM	Misc
GCLKN	HCLKN	SRCOMP1	DREFCLKN
GCLKP	HCLKP	SRCOMP0	DREFCLKP
EXP_COMPO	HRCOMP	SMVREF1	BLUE
EXP_COMPI	HSCOMP	SMVREF0	BLUE#
	HVREF	SOCOMP1	GREEN
	HSWING	SOCOMP0	GREEN#
		SM_SLEWOUT1	RED
		SM_SLEWOUT0	RED#
		SM_SLEWIN1	RSTIN#
		SM_SLEWIN0	HSYNC
			VSYNC
			REFSET