

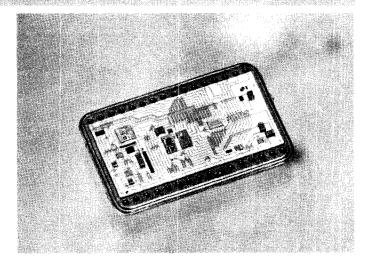
Ultra-Fast Hybrid Analog to Digital Converters

FEATURES

- Conversion Times as Low as 1.2μs
- Resolution: 8, 10 and 12 Bits
- Exceptional Accuracy, 0.012% of F.S.
- Low Power
- Contained in Glass or Metal 32-Pin DIP
- Adjustment-Free Operation

APPLICATIONS

- Waveform Analysis
- Fast Fourier Transforms
- Radar



GENERAL DESCRIPTION

With a typical conversion time of only 2.2µs for complete 12-bit conversion, the Analog Devices' HAS series hybrid A/D converters are the fastest, smallest, most complete successive-approximation A/D's available. Housed in 32-pin DIP packages, these converters feature laser trimming for accuracy and linearity surpassing the best modular competitive A/D's. This series offers a unique combination of flexibility and simplicity which allows them to be used as stand-alone A/D converters requiring no additional external potentiometers and needing only an analog input signal and encode command for operation.

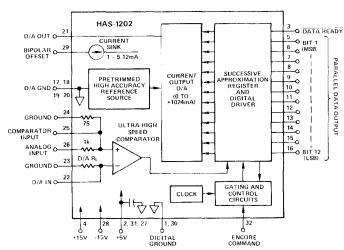
The HAS-1202 A/D features an accuracy of 0.012% and when combined with an HTC-0300 track-and-hold, forms an A/D conversion system capable of up to 350kHz sampling rates.

The HAS series A/D's are ideally suited for applications requiring excellent performance characteristics, small size, low power consumption and adjustment-free operation. Some of these applications include radar, PCM, data-acquisition, and digital-signal-processing systems where FFT's and other digital processing techniques are to be performed on analog input data.

For the ultra-high reliability requirements of military and aerospace applications these A/D's are optionally available with hermetically sealed metal cases and with MIL-STD-883 processing.

Extreme care in circuit layout should be exercised when using these hybrids in order to obtain rated performance. In particular, input and output runs should be as short as possible, a ground plane should be used to tie all ground pins together, and power supplies should be bypassed as close to the hybrid

circuit power supply pins as possible. Do not allow input or other analog signal lines to be in close proximity to or cross over any digital output line.



NOTES: 1 FUNCTIONAL CONFIGURATION SHOWN IS FOR THE HAS 1202
FOR THE HAS 1002 PINS 15 AND 16 ARE NOT CONNECTED IN
TERNALLY FOR HAS 0802 PINS 13, 14, 15 AND 16 ARE NOT CON
NECTED INTERNALLY.

Block Diagram - HAS Series

^{2.} FOR BIPOLAR OPERATION, CONNECT PIN 21 TO PIN 29. FOR UNIPOLAR OPERATION, LEAVE PIN 21 OPEN AND GROUND PIN 29.

SPECIFICATIONS (typical @ +25°C with nominal voltages unless otherwise noted)

MODEL	UNITS	HAS-0802	HAS-1002	HAS-1202
RESOLUTION	BITS	8	10	12
LSB Weight	% Full Scale	0.4	0.1	0.025
	ınV	40	10	2.5
RELATIVE ACCURACY (INCLUDING LINEARITY)	'6 Full Scale	0.05	0.025	0.012
Quantization Error	LSB	±1/2	*	*
LINEARITY VS. TEMPERATURE	ppm/°C	3	*	*
ENVERTED VO. TEM EIGHT ORE	ppin/ C	(No Missing Codes over Temperature Range)		
INDUT OFFCET VOLTAGE		(140 Hilliaming	Godes over Tel	inperature ivange)
INPUT OFFSET VOLTAGE	.,,			
Initial (Trimmable to Zero)	ɪnV μV/°C	10		
Zero Offset vs. Temperature	μν/ C μν/°C	15		
Bipolar Offset vs. Temperature	µV/ C	100		
GAIN ERROR			_	
Initial (Trimmable to Zero)	% Full Scale	0.1	*	•
Gain vs. Temperature	l _i bm/ _o C	30		*
INPUT				
Ranges (Full Scale)				
"Built-In" Standard Unipolar	V ±0.1%	+10.24	*	*
Bipolar	V ±0.05%	±5.12		
Resistor Programmable (See Figure 3)	V, 0 to:		5, +20, ±2.5, ±3	3.75, ±7.5, ±10
Impedance	Ωmin	1000	. 11.0	-
Overvoltage		Two Times F	ull Scale + or -	-
CONVERSION TIME (COMPLETE CYCLE TIME)	µs max (typ)	1.5 (1.2)	1.7 (1.4)	2.8 (2.2)
CONVERSION RATE	kHz max	667	558	357
ENCODE COMMAND - TTL LOGIC INPUT				***
Logic Levels (Positive Logic)	V	"0" = 0 to +0	0.4, "1" = +2 t	0.+5
Function ¹	*		esets Converter	
			arts Conversion	
Loading		1 Standard T		•
•		"0" = -1.6		
		"1" = 40µ		
Pulse Width	ns min	100	*	*
Repetition Rate			m Conversion	Rate
LOGIC OUTPUTS				
Data Ready (DR)				
Data Many (DIV)		Cinnale comus	reion is comple	
Function		Signals conversion is complete when low. After DR goes low, data is valid. A new con-		
Function				
Function		After DR goo	s low, data is v	alid. A new con-
Function		After DR goo version may	es low, data is v	ralid. A new con- this time. DR may
Function		After DR god version may be used to str	es low, data is vote initiated at the coole data into	valid. A new con- this time. DR may external register if
		After DR good version may be used to stradequate region	es low, data is v	valid. A new con- this time. DR may external register if
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Timing Loading		After DR god version may be used to stradequate regisee Figure 1	es low, data is vote initiated at the coole data into	valid. A new con- this time. DR may external register if e is allowed.
Timing Loading Parallel Data		After DR god version may be used to stradequate reg. See Figure 1 5 Standard T	es low, data is vote initiated at the control of th	valid. A new con- this time. DR may external register if e is allowed.
Timing Loading		After DR god version may be used to stradequate reg See Figure 1 5 Standard T 8-, 10-, or 12	es low, data is vobe initiated at the cooled data into the cooled at the	valid. A new con- this time. DR may external register if e is allowed.
Timing Loading Parallel Data		After DR god version may be used to stradequate reg. See Figure 1 5 Standard T 8-, 10-, or 12 DR output ge	es low, data is vote initiated at tooke data into officer setup time. TL Loads, manifests parallel dates low until 20	valid. A new con- this time. DR may external register if e is allowed.
Timing Loading Parallel Data Format		After DR god version may be used to stradequate reg See Figure 1 5 Standard T 8-, 10-, or 12 DR output gencode comm	es low, data is vobe initiated at too be data into o ister setup time. TL Loads, manuellits parallel dates low until 20 nand.	valid. A new con- this time. DR may external register if e is allowed.
Timing Loading Parallel Data		After DR goversion may be used to sused to sused to sused see Figure 1 5 Standard T 8-, 10-, or 12 DR output gencode comm	es low, data is vote initiated at a crobe data into a steed at the crobe data into a steed at the crobe data into a steed at the crobe data in the crobe data and a steed at the crobe data into a steed at the crobe data and a steed at the cr	valid. A new con- this time. DR may external register if e is allowed.
Timing Loading Parallel Data Format		After DR goversion may be used to stradequate reg See Figure 1 5 Standard T 8-, 10-, or 12 DR output gencode community to the compatition of the	es low, data is vote initiated at too be data into o dister setup time. TL Loads, manifold parallel data of the setup time of the setup time. TL add, ible: to +0.4V	valid. A new con- this time. DR may external register if e is allowed.
Timing Loading Parallel Data Format Logic Levels		After DR goversion may be used to stradequate regisee Figure 1 5 Standard T 8-, 10-, or 12 DR output gencode commun TTL Compat "0" = 0V "1" = +2.	es low, data is vote initiated at too be data into o ister setup time. TL Loads, may bits parallel dates low until 20 mand. ible: to +0.4V 4V to +5V	valid. A new con- this time. DR may external register if e is allowed.
Timing Loading Parallel Data Format		After DR goversion may be used to sued to sued to stadequate reg See Figure 1 5 Standard T 8-, 10-, or 12 DR output gencode comm TTL Compati "0" = 0V "1" = +2.4 Will drive up	es low, data is we be initiated at the cobe data into the cobe data in the cobe dat	valid. A new con- this time. DR may external register if e is allowed. Ata. Valid from time Ons after receipt of next
Timing Loading Parallel Data Format Logic Levels		After DR goversion may be used to sused	es low, data is we be initiated at a crobe data into a cister setup time. TL Loads, manually be low until 20 and. ible: to +0.4V 4V to +5V to 5 Standard Loads.	valid. A new conthistime. DR may external register if is allowed. At a. Valid from time one after receipt of next
Timing Loading Parallel Data Format Logic Levels Loading		After DR goversion may be used to sus adequate reg. See Figure 1 5 Standard T 8-, 10-, or 12 DR output gencode comm TTL Compat "0" = 0V "1" = +2.4 Will drive up "S" or "H" I Offset Binary	es low, data is we be initiated at a crobe data into a cister setup time. TL Loads, man-bits parallel dates low until 20 nand. ible: to +0.4V 4V to +5V to 5 Standard coads. (BIN) for Unitiation of the coads.	valid. A new con- this time. DR may external register if is allowed. Ata. Valid from time Ons after receipt of next TTL Loads or 2 TTL polar Inputs:
Timing Loading Parallel Data Format Logic Levels Loading		After DR goversion may be used to stradequate regisee Figure 1 5 Standard T 8-, 10-, or 12 DR output gencode comm TTL Compat "0" = 0V "1" = +2.4 Will drive up "S" or "H" I Offset Binary +10.24	es low, data is vote initiated at a cobe data into a cister setup time. TL Loads, manuallel data and a cister setup time. TL Loads, manuallel data and a cister setup time and a cister setup time. TL Loads, manuallel data and a cister setup time. TL Loads, manuallel data and a cister setup time. TL Loads, manuallel data and a cister setup time. TL Loads, manuallel data and a cister setup time. TL Loads, manuallel data and a cister setup time.	valid. A new conthistime. DR may external register if e is allowed. Ata. Valid from time Ons after receipt of next TTL Loads or 2 TTL polar Inputs: . 1
Timing Loading Parallel Data Format Logic Levels Loading		After DR goversion may be used to stradequate reg See Figure 1 5 Standard T 8-, 10-, or 12 DR output gencode commode compation of the standard commode commode commode commode compation of the standard commode commode compation of the standard commode commode commode compation compation compatible compatible commode commode compatible compatible compatible commode commode compatible comp	es low, data is vote initiated at too be initiated at too be data into o dister setup time. TL Loads, mand-bits parallel date be slow until 20 mand. ible: to +0.4V 4V to +5V to 5 Standard loads. v(BIN) for Univ. V = 0 0 0 0 0	valid. A new conthistime. DR may external register if e is allowed. Ata. Valid from time ons after receipt of next TTL Loads or 2 TTL polar Inputs: . 1 . 0
Timing Loading Parallel Data Format Logic Levels Loading		After DR goversion may be used to save the used to save to save the used t	es low, data is we be initiated at a robe data into a robe data a r	valid. A new con- this time. DR may external register if e is allowed. Atta. Valid from time Ons after receipt of next TTL Loads or 2 TTL polar Inputs: . 1 . 0 polar Inputs:
Timing Loading Parallel Data Format Logic Levels Loading		After DR goversion may be used to suse	es low, data is we be initiated at a crobe data into a crobe data	valid. A new conthistime. DR may external register if e is allowed. At a. Valid from time on after receipt of next of the control of the con
Timing Loading Parallel Data Format Logic Levels Loading		After DR goversion may be used to sus adequate reg See Figure 1 5 Standard T 8-, 10-, or 12 DR output gencode comm TTL Compat "0" = 0V "1" = +2.4 Will drive up "S" or "H" I Offset Binary +5.12V 0V	es low, data is we be initiated at a robe data into a robe data a r	valid. A new conthistime. DR may external register if e is allowed. Ata. Valid from time one after receipt of next of the control of the con
Timing Loading Parallel Data Format Logic Levels Loading Coding ²		After DR goversion may be used to sus adequate reg See Figure 1 5 Standard T 8-, 10-, or 12 DR output gencode comm TTL Compat "0" = 0V "1" = +2.4 Will drive up "S" or "H" I Offset Binary +5.12V 0V	es low, data is we be initiated at a crobe data into a crobe data	valid. A new conthistime. DR may external register if e is allowed. Ata. Valid from time one after receipt of next of the control of the con
Timing Loading Parallel Data Format Logic Levels Loading Coding ²		After DR goversion may be used to sure adequate regiser 15 Standard T 8-, 10-, or 12 DR output gencode community of the sure	es low, data is we be initiated at a crobe data into a crobe data	valid. A new conthistime. DR may external register if e is allowed. Ata. Valid from time one after receipt of next of the control of the con
Timing Loading Parallel Data Format Logic Levels Loading Coding ² POWER REQUIREMENTS +14.5V to +15.5V (+18V Absolute Max)	mA	After DR goversion may be used to strain adequate regiser Figure 1 5 Standard T 8-, 10-, or 12 DR output gencode community and the strain a	es low, data is we be initiated at a crobe data into a crobe data	valid. A new conthistime. DR may external register if e is allowed. Ata. Valid from time one after receipt of next of the control of the con
Timing Loading Parallel Data Format Logic Levels Loading Coding ² POWER REQUIREMENTS +14.5V to +15.5V (+18V Absolute Max) -14.5V to -15.5V (-18V Absolute Max)	mιA	After DR goversion may be used to stradequate reg See Figure 1 5 Standard T 8-, 10-, or 12 DR output gencode community of the service of th	es low, data is we be initiated at a crobe data into a crobe data	valid. A new conthistime. DR may external register if e is allowed. Ata. Valid from time one after receipt of next of the control of the con
Timing Loading Parallel Data Format Logic Levels Loading Coding ² POWER REQUIREMENTS +14.5V to +15.5V (+18V Absolute Max)		After DR goversion may be used to strain adequate regiser Figure 1 5 Standard T 8-, 10-, or 12 DR output gencode community and the strain a	es low, data is we be initiated at a crobe data into a crobe data	valid. A new conthistime. DR may external register if e is allowed. Ata. Valid from time one after receipt of next of the control of the con
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Timing Loading Parallel Data Format Logic Levels Loading Coding ² POWER REQUIREMENTS +14.5V to +15.5V (+18V Absolute Max) -14.5V to -15.5V (-18V Absolute Max) +4.75V to +5.25V (+7V Absolute Max)	mιA	After DR goversion may be used to stradequate reg See Figure 1 5 Standard T 8-, 10-, or 12 DR output gencode community of the service of th	es low, data is we be initiated at a crobe data into a crobe data	valid. A new conthistime. DR may external register if e is allowed. Ata. Valid from time one after receipt of next of the control of the con

NOTES:

After converter is reset, all other logic signals, including clock, are internally generated.

When HAS series A/D's are used with HTC-0300 track/hold, output coding is complementary binary (CBN) for unipolar inputs and complementary offset binary (COB) for bipolar inputs (see Table 1).

^{*}Specifications same as model HAS-0802. Specifications subject to change without notice.

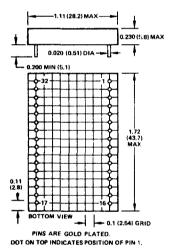
Table 1. Output Coding*

SCALE	INPUT OF HTC-0300	INPUT OF HAS-1202	DIGITAL OUTPUT
UNIPOLAR OPERATION			
FS-1LSB	-10.2375V	+10.2375V	111111111111
3/4 FS	- 7.6800V	+ 7.6800V	110000000000
1/2 FS	- 5.1200V	+ 5.1200V	100000000000
1/4 FS	- 2.5600V	+ 2.5600V	010000000000
+1LSB	- 0.0025V	+ 0.0025V	000000000001
0	0.0000V	0.0000V	000000000000
BIPOLAR OPERATION			
+FS-1LSB	- 5.1175V	+ 5.1175V	111111111111
0	0.0000V	0.0000V	1000000000000
-FS+1LSB	+ 5.1175V	- 5.1175V	000000000001
-FS	+ 5.1200V	- 5.1200V	000000000000

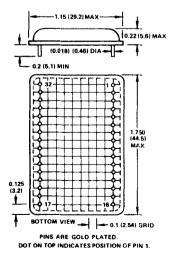
^{*}Coding and input levels shown are for HAS-1202. For 8- and 10-bit A/D's the input levels are less by the values of the LSB weight for each type, and the digital output will show only 8 or 10 bits, respectively.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



GLASS PACKAGE

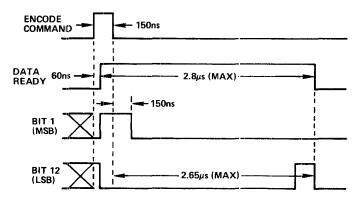


METAL PACKAGE (M) (OPTIONAL)

PIN DESIGNATIONS HAS-1202*

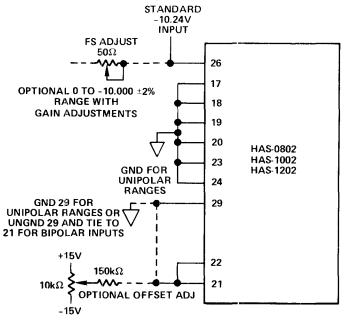
PIN	FUNCTION
1, 30	DIGITAL GROUND
2, 27, 31	+5V
3	DATA READY
4	+15V
5	BIT 1 OUTPUT (MSB)
6	BIT 2 OUTPUT
7	BIT 3 OUTPUT
8	BIT 4 OUTPUT
9	BIT 5 OUTPUT
10	BIT 6 OUTPUT
11	BIT 7 OUTPUT
12	BIT 8 OUTPUT
13	BIT 9 OUTPUT
14	BIT 10 OUTPUT
15	BIT 11 OUTPUT
16	BIT 12 OUTPUT (LSB)
17, 18, 19	ANALOG GROUND
20, 23, 24	ANALOG GROUND
25	COMP INPUT
26	ANALOG INPUT
28	-15V
29	BIPOLAR OFFSET
32	ENCODE COMMAND

*HAS-1002, PINS 15 AND 16 ARE NOT CONNECTED INTERNALLY. HAS-0802, PINS 13, 14, 15 AND 16 ARE NOT CONNECTED INTERNALLY.



TIMING SHOWN FOR HAS-1202. TIMING IS SIMILAR FOR HAS-1002 AND HAS-0802 EXCEPT LSB IS BIT 10 AND 8, RESPECTIVELY, AND TOTAL TYPICAL CONVERSION TIME IS $1.4\mu s$ AND $1.2\mu s$, RESPECTIVELY.

Figure 1. Timing Diagram (Typical)



NOTES:

- 1. THIS CIRCUIT SHOWN FOR UNIPOLAR (0 TO -10.24V) INPUT. 0V INPUT = 00000000000; -10.24 INPUT = 111111111111.
- FOR BIPOLAR (±5.12V) INPUT, UNGROUND PIN 29 AND CONNECT PIN 29 TO PIN 21.
- 3. FOR EXTRA-PRECISE GAIN (FULL-SCALE) ADJUSTMENT, CONNECT A 50Ω VARIABLE RESISTANCE IN SERIES WITH PIN 20 OF HAS-1202. THIS WILL RESULT IN 0 TO -10.000V INPUT WITH ADJUSTMENT RANGE OF ±2% OF FULL SCALE.
- 4. FOR EXTRA-PRECISE ZERO OFFSET ADJUSTMENT, CONNECT 150k RESISTOR FROM PIN 21 TO THE TAP OF A 10k POTEN-TIOMETER. END TERMINATIONS OF POTENTIOMETER CONNECT TO +15V AND -15V. THIS ZERO OFFSET ADJUSTMENT WILL HAVE A RANGE OF APPROXIMATELY ±100m¹V.

Figure 2. Input Connections For Standard Input Ranges

Input Connections For Optional Input Ranges

INPUT RANGE	R1	R2	Z _{IN}	ABSOLUTE MAXIMUM SIGNAL
0 to $+5V$, $\pm 2.5V$	SHORT	1000	500	±10V
0 to $+7.5V$, $\pm 3.75V$	SHORT	3000	750	±15V
0 to $+15V$, $\pm 7.5V$	500	OPEN	1500	±30V
0 to $+20V$, $\pm 10V$	1000	OPEN	2000	±40V

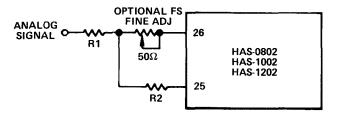


Figure 3. Full Scale Trim

APPLICATION CIRCUIT

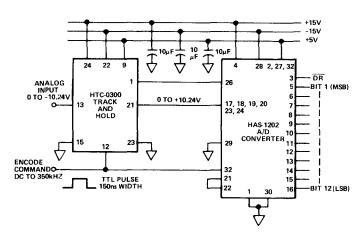


Figure 4. DC to 350kHz, 12-Bit, A/D Conversion System

ORDERING INFORMATION

Order model number HAS-0802, HAS-1002, or HAS-1202 for 8-, 10-, or 12-bit operation, respectively. Mating connector for the HAS series A/D's is model number HSA-2. Metal cased versions of this A/D with extended operating temperature range, and MIL-STD processing are also available. Consult the factory or nearest Analog Devices' sales office for further information.