

0.25 μm CMOS Gate Array **CMOS-10HD Family**



*High-density, high-speed 0.25 μm CMOS gate array
Supporting low internal power-supply voltage of 2.5/1.8V*

INTRODUCTION

This pamphlet summarizes information for learning about NEC Electronics' CMOS-10HD Family of high-speed, high-density CMOS gate arrays.

The following abbreviations are used for the package names in this pamphlet.

Abbreviation	Standard Package Name
QFP	Plastic QFP
PBGA	Plastic BGA
TBGA	Tape BGA
FPBGA™	Fine pitch plastic BGA

FEATURES

The CMOS-10HD family is a channel-less gate array to which a 0.25 μm CMOS process has been applied. This family supports a low internal power-supply voltage of 2.5/1.8 V and provides two types of power-line master; single power-supply and dual power-supply. This family can be applied to medium or large sized systems with a 2.5/1.8 V single drive or a 3.3/2.5 V and 3.3/1.8 V mixed interface.

High-Speed Operation

- 1.8 V operation (1.8 V interface, 3.3 V interface)

$t_{PD} = 129$ ps (2-input NAND, fan-out: 1, wiring length: 0 mm)

$t_{PD} = 163$ ps (2-input NAND, fan-out: 1, standard wiring length)

$t_{PD} = 146$ ps (2-input NAND, standard load)

$t_{PD} = 139$ ps (2-input NAND (power gate), fan-out: 1, standard wiring length)

$t_{PD} = 126$ ps (2-input NAND (power gate), standard load)

$t_{PD} = 243$ ps (1.8 V input buffer, fan-out: 1, standard wiring length)

$t_{PD} = 239$ ps (1.8 V input buffer, standard load)

$t_{PD} = 353$ ps (3.3 V input buffer, fan-out: 1, standard wiring length)

$t_{PD} = 342$ ps (3.3 V input buffer, standard load)

$t_{PD} = 1246$ ps (1.8 V output buffer, $C_L = 15$ pF, $I_{OL} = 12$ mA)

$t_{PD} = 1524$ ps (3.3 V output buffer, $C_L = 15$ pF, $I_{OL} = 12$ mA)

- 2.5 V operation (2.5 V interface, 3.3 V interface)

$t_{PD} = 85$ ps (2-input NAND, fan-out: 1, wiring length: 0 mm)

$t_{PD} = 113$ ps (2-input NAND, fan-out: 1, standard wiring length)

$t_{PD} = 99$ ps (2-input NAND, standard load)

$t_{PD} = 91$ ps (2-input NAND (power gate), fan-out: 1, standard wiring length)

$t_{PD} = 83$ ps (2-input NAND (power gate), standard load)

$t_{PD} = 173$ ps (2.5 V input buffer, fan-out: 1, standard wiring length)

$t_{PD} = 169$ ps (2.5 V input buffer, standard load)

$t_{PD} = 294$ ps (3.3 V input buffer, fan-out: 1, standard wiring length)

$t_{PD} = 289$ ps (3.3 V input buffer, standard load)

$t_{PD} = 776$ ps (2.5 V output buffer, $C_L = 15$ pF, $I_{OL} = 12$ mA)

$t_{PD} = 1169$ ps (3.3 V output buffer, $C_L = 15$ pF, $I_{OL} = 12$ mA)

Internal Blocks

- High-speed block
- Low power block
- Scan path block
- Driver for clock tree synthesis

Memory Blocks

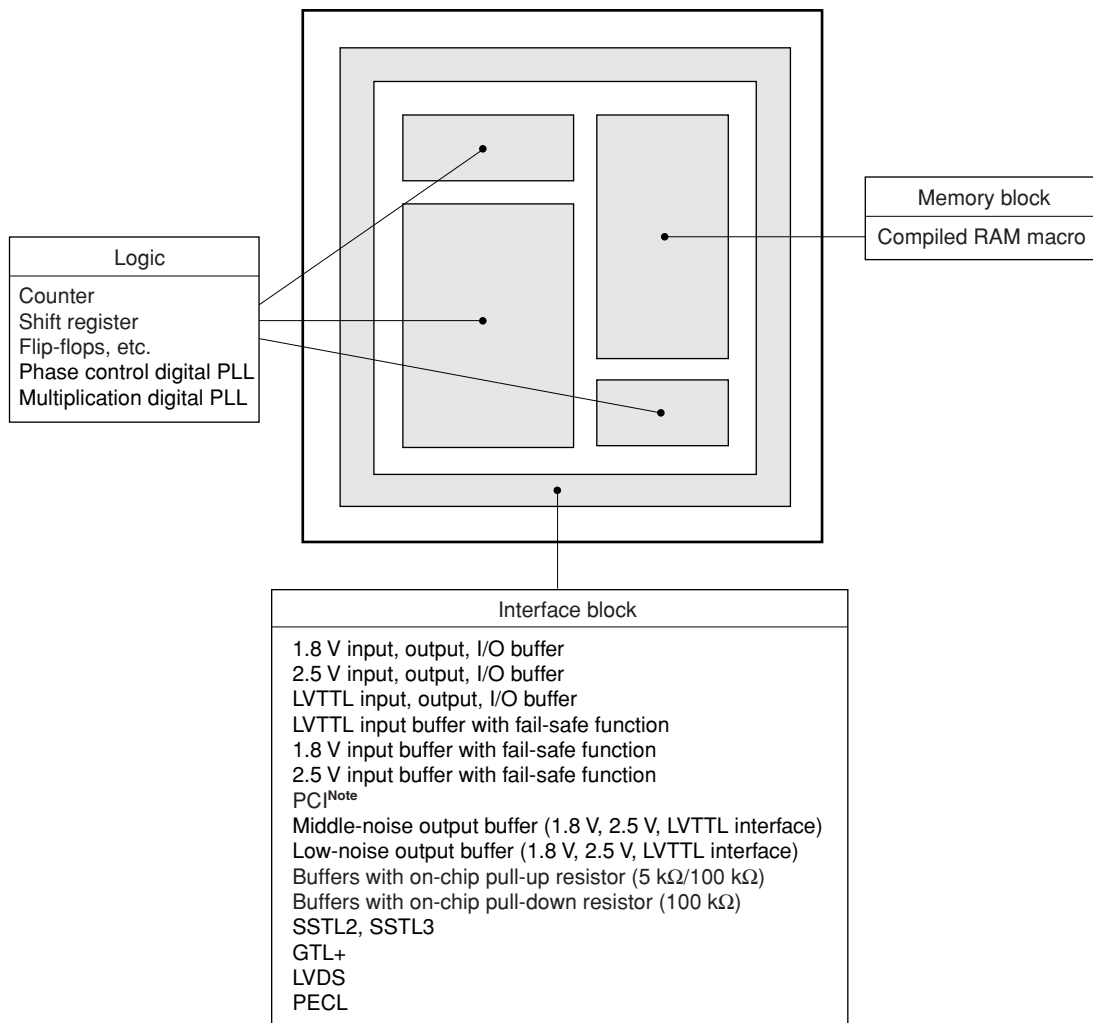
- Synchronous compiled single-port RAM
- Synchronous compiled dual-port RAM

Abundance of Peripheral Blocks

- 1.8 V input, output, I/O buffer
- 2.5 V input, output, I/O buffer
- LVTTTL input, output, I/O buffer
- LVTTTL input buffer with fail-safe function
- 1.8 V input buffer with fail-safe function
- 2.5 V input buffer with fail-safe function
- Buffer for PCI bus specification
- Middle-noise output buffer (1.8 V, 2.5 V, LVTTTL interface)
- Low-noise output buffer (1.8 V, 2.5 V, LVTTTL interface)
- Buffer with on-chip pull-up resistor (5 k Ω /100 k Ω)
- Buffer with on-chip pull-down resistor (100 k Ω)
- Phase control digital PLL
- Multiplication digital PLL
- SSTL2, SSTL3
- GTL+
- LVDS
- PECL

Multifarious Function Block Mounting Capability

The function blocks ensure functional compatibility with conventional products and facilitate transfer or appropriation of existing design data.



Note Standard interface recommended by Intel Corp. (PCI = Peripheral Component Interconnect)

PRODUCT OUTLINE

List of Product Types

3-layer master	Single power supply	μ PD65301 μ PD65321	μ PD65302 μ PD65322	μ PD65303 μ PD65323	μ PD65304 μ PD65324	μ PD65305 μ PD65325
	Dual power supply	μ PD65341 μ PD65361	μ PD65342 μ PD65362	μ PD65343 μ PD65363	μ PD65344 μ PD65364	μ PD65345 μ PD65365
Number of cells placed		58682	128338	192058	299472	409920
Number of usable gates		38143	83420	124837	194657	245952
4-layer master	Single power supply	μ PD65501 μ PD65521	μ PD65502 μ PD65522	μ PD65503 μ PD65523	μ PD65504 μ PD65524	μ PD65505 μ PD65525
	Dual power supply	μ PD65541 μ PD65561	μ PD65542 μ PD65562	μ PD65543 μ PD65563	μ PD65544 μ PD65564	μ PD65545 μ PD65565
Number of cells placed		58682	128338	192058	299472	409920
Number of usable gates		41077	89837	134441	209630	266448

3-layer master	Single power supply	μ PD65306 μ PD65326	μ PD65307 μ PD65327	μ PD65308 μ PD65328	μ PD65309 μ PD65329	μ PD65310 μ PD65330	μ PD65311 μ PD65331
	Dual power supply	μ PD65346 μ PD65366	μ PD65347 μ PD65367	μ PD65348 μ PD65368	μ PD65349 μ PD65369	μ PD65350 μ PD65370	μ PD65351 μ PD65371
Number of cells placed		545008	721224	1014542	1404790	1974700	2605764
Number of usable gates		299754	396673	557998	702395	987350	1302882
4-layer master	Single power supply	μ PD65506 μ PD65526	μ PD65507 μ PD65527	μ PD65508 μ PD65528	μ PD65509 μ PD65529	μ PD65510 μ PD65530	μ PD65511 μ PD65531
	Dual power supply	μ PD65546 μ PD65566	μ PD65547 μ PD65567	μ PD65548 μ PD65568	μ PD65549 μ PD65569	μ PD65550 μ PD65570	μ PD65551 μ PD65571
Number of cells placed		545008	721224	1014542	1404790	1974700	2605764
Number of usable gates		354255	468796	659452	842874	1184820	1563458

List of Packages

Single power supply

(1/4)

Package	Number of Pins	Lead Pitch	Body Size (mm)	Body Thickness	μ PD65301 μ PD65501	μ PD65302 μ PD65502	μ PD65303 μ PD65503	μ PD65304 μ PD65504	μ PD65305 μ PD65505
QFP (fine pitch)	144	0.5 mm	20 × 20	2.70 mm	–				
	160	0.5 mm	24 × 24	2.70 mm	–				
	208	0.5 mm	28 × 28	3.20 mm	–	–			
	240	0.5 mm	32 × 32	3.20 mm	–	–	–		
	304	0.5 mm	40 × 40	3.70 mm	–	–	–	–	–
TQFP	48	0.5 mm	7 × 7	1.00 mm	○	–	–	–	–
	64	0.5 mm	10 × 10	1.00 mm	–			–	–
	80	0.5 mm	12 × 12	1.00 mm	–				
	120	0.4 mm	14 × 14	1.00 mm	–	–	–		
LQFP	44	0.8 mm	10 × 10	1.40 mm					–
	100	0.5 mm	14 × 14	1.40 mm	–	–	–		
	144	0.5 mm	20 × 20	1.40 mm	–		–		
FPBGA	108	0.8 mm, perimeter	11 × 11	1.51 mm					
	144	0.8 mm, perimeter	13 × 13	1.51 mm	–				
	160	0.8 mm, perimeter	13 × 13	1.51 mm	–				
	208	0.8 mm, perimeter	15 × 15	1.51 mm	–	–	–		
	240	0.8 mm, perimeter	19 × 19	1.51 mm	–	–	–		
	304	0.8 mm, perimeter	19 × 19	1.51 mm	–	–	–	–	
PBGA	256	1.27 mm, perimeter	27 × 27	2.13 mm	–	–	–		
	313	1.27 mm, staggered	35 × 35	2.33 mm	–	–	–	–	–
	352	1.27 mm, perimeter	35 × 35	2.33 mm	–	–	–	–	–

- Remarks**
- : Already shifted, Blank: Under study, –: Cannot be used
 - μ PD653xx: 3-layer product, μ PD655xx: 4-layer product

List of Packages

Single power supply

(2/4)

Package	Number of Pins	Lead Pitch	Body Size (mm)	Body Thickness	μ PD65306	μ PD65307	μ PD65308	μ PD65309	μ PD65310	μ PD65311
					μ PD65506	μ PD65507	μ PD65508	μ PD65509	μ PD65510	μ PD65511
QFP (fine pitch)	144	0.5 mm	20 × 20	2.70 mm						
	160	0.5 mm	24 × 24	2.70 mm					○	
	208	0.5 mm	28 × 28	3.20 mm						
	240	0.5 mm	32 × 32	3.20 mm						
	304	0.5 mm	40 × 40	3.70 mm	–					
TQFP	48	0.5 mm	7 × 7	1.00 mm	–	–	–	–	–	–
	64	0.5 mm	10 × 10	1.00 mm	–	–	–	–	–	–
	80	0.5 mm	12 × 12	1.00 mm				–	–	–
	120	0.4 mm	14 × 14	1.00 mm					–	–
LQFP	44	0.8 mm	10 × 10	1.40 mm	–	–	–	–	–	–
	100	0.5 mm	14 × 14	1.40 mm					–	–
	144	0.5 mm	20 × 20	1.40 mm						
FPBGA	108	0.8 mm, perimeter	11 × 11	1.51 mm		–	–	–	–	–
	144	0.8 mm, perimeter	13 × 13	1.51 mm	–		–	–	–	–
	160	0.8 mm, perimeter	13 × 13	1.51 mm					–	–
	208	0.8 mm, perimeter	15 × 15	1.51 mm						–
	240	0.8 mm, perimeter	19 × 19	1.51 mm						
	304	0.8 mm, perimeter	19 × 19	1.51 mm						
PBGA	256	1.27 mm, perimeter	27 × 27	2.13 mm						–
	313	1.27 mm, staggered	35 × 35	2.33 mm						
	352	1.27 mm, perimeter	35 × 35	2.33 mm						

- Remarks**
1. ○: Already shifted, Blank: Under study, –: Cannot be used
 2. μ PD653xx: 3-layer product, μ PD655xx: 4-layer product

List of Packages

Single power supply

(3/4)

Package	Number of Pins	Lead Pitch	Body Size (mm)	Body Thickness	μ PD65321	μ PD65322	μ PD65323	μ PD65324	μ PD65325	μ PD65326
					μ PD65521	μ PD65522	μ PD65523	μ PD65524	μ PD65525	μ PD65526
TQFP	64	0.5 mm	10 × 10	1.00 mm		–	–	–	–	–
	80	0.5 mm	12 × 12	1.00 mm		–	–	–	–	–
	100	0.5 mm	14 × 14	1.00 mm				–	–	–
	120	0.4 mm	14 × 14	1.00 mm	–			–	–	–
LQFP	100	0.5 mm	14 × 14	1.40 mm				–	–	–
	144	0.5 mm	20 × 20	1.40 mm	–	–		–	–	–
TBGA ^{Note}	256	1.27 mm, perimeter	27 × 27	1.40 mm	–	–	–			
	352	1.27 mm, perimeter	35 × 35	1.40 mm	–	–	–	–	–	
	420	1.27 mm, perimeter	35 × 35	1.40 mm	–	–	–	–	–	–
	500	1.27 mm, perimeter	40 × 40	1.40 mm	–	–	–	–	–	–
	576	1.27 mm, perimeter	40 × 40	1.40 mm	–	–	–	–	–	–

Note With heat spreader

- Remarks**
- Blank: Under study, –: Cannot be used
 - μ PD653xx: 3-layer product, μ PD655xx: 4-layer product

Single power supply

(4/4)

Package	Number of Pins	Lead Pitch	Body Size (mm)	Body Thickness	μ PD65327	μ PD65328	μ PD65329	μ PD65330	μ PD65331
					μ PD65527	μ PD65528	μ PD65529	μ PD65530	μ PD65531
TQFP	64	0.5 mm	10 × 10	1.00 mm	–	–	–	–	–
	80	0.5 mm	12 × 12	1.00 mm	–	–	–	–	–
	100	0.5 mm	14 × 14	1.00 mm	–	–	–	–	–
	120	0.4 mm	14 × 14	1.00 mm	–	–	–	–	–
LQFP	100	0.5 mm	14 × 14	1.40 mm	–	–	–	–	–
	144	0.5 mm	20 × 20	1.40 mm	–	–	–	–	–
TBGA ^{Note}	256	1.27 mm, perimeter	27 × 27	1.40 mm					
	352	1.27 mm, perimeter	35 × 35	1.40 mm					
	420	1.27 mm, perimeter	35 × 35	1.40 mm					
	500	1.27 mm, perimeter	40 × 40	1.40 mm	–				
	576	1.27 mm, perimeter	40 × 40	1.40 mm	–	–			

Note With heat spreader

- Remarks**
- Blank: Under study, –: Cannot be used
 - μ PD653xx: 3-layer product, μ PD655xx: 4-layer product

List of Packages

Dual power supply

(1/4)

Package	Number of Pins	Lead Pitch	Body Size (mm)	Body Thickness	μ PD65341	μ PD65342	μ PD65343	μ PD65344	μ PD65345
					μ PD65541	μ PD65542	μ PD65543	μ PD65544	μ PD65545
QFP (fine pitch)	144	0.5 mm	20 × 20	2.70 mm	–	○			
	160	0.5 mm	24 × 24	2.70 mm	–				
	208	0.5 mm	28 × 28	3.20 mm	–	–		○	
	304	0.5 mm	40 × 40	3.70 mm	–	–	–	–	–
TQFP	48	0.5 mm	7 × 7	1.00 mm		–	–	–	–
	64	0.5 mm	10 × 10	1.00 mm	–			–	–
	80	0.5 mm	12 × 12	1.00 mm	–				
	120	0.4 mm	14 × 14	1.00 mm	–	–	–		
LQFP	44	0.8 mm	10 × 10	1.40 mm					–
	100	0.5 mm	14 × 14	1.40 mm	–	–	–		
	144	0.5 mm	20 × 20	1.40 mm	–		–		
FPBGA	108	0.8 mm, perimeter	11 × 11	1.51 mm	○				○
	144	0.8 mm, perimeter	13 × 13	1.51 mm	–				
	160	0.8 mm, perimeter	13 × 13	1.51 mm	–				
	208	0.8 mm, perimeter	15 × 15	1.51 mm	–	–	–	○	○
	240	0.8 mm, perimeter	19 × 19	1.51 mm	–	–	–		○
	304	0.8 mm, perimeter	19 × 19	1.51 mm	–	–	–	–	
PBGA	256	1.27 mm, perimeter	27 × 27	2.13 mm	–	–	–		
	313	1.27 mm, staggered	35 × 35	2.33 mm	–	–	–	–	–
	352	1.27 mm, perimeter	35 × 35	2.33 mm	–	–	–	–	–

Remarks 1. ○: Already shifted, Blank: Under study, –: Cannot be used
 2. μ PD653xx: 3-layer product, μ PD655xx: 4-layer product

List of Packages

Dual power supply

(2/4)

Package	Number of Pins	Lead Pitch	Body Size (mm)	Body Thickness	μ PD65346	μ PD65347	μ PD65348	μ PD65349	μ PD65350	μ PD65351
					μ PD65546	μ PD65547	μ PD65548	μ PD65549	μ PD65550	μ PD65551
QFP (fine pitch)	144	0.5 mm	20 × 20	2.70 mm						
	160	0.5 mm	24 × 24	2.70 mm						
	208	0.5 mm	28 × 28	3.20 mm			○			
	304	0.5 mm	40 × 40	3.70 mm	–	○				
TQFP	48	0.5 mm	7 × 7	1.00 mm	–	–	–	–	–	–
	64	0.5 mm	10 × 10	1.00 mm	–	–	–	–	–	–
	80	0.5 mm	12 × 12	1.00 mm				–	–	–
	120	0.4 mm	14 × 14	1.00 mm					–	–
LQFP	44	0.8 mm	10 × 10	1.40 mm	–	–	–	–	–	–
	100	0.5 mm	14 × 14	1.40 mm	○	○	○	○	–	–
	144	0.5 mm	20 × 20	1.40 mm						
FPBGA	108	0.8 mm, perimeter	11 × 11	1.51 mm		–	–	–	–	–
	144	0.8 mm, perimeter	13 × 13	1.51 mm	–		–	–	–	–
	160	0.8 mm, perimeter	13 × 13	1.51 mm					–	–
	208	0.8 mm, perimeter	15 × 15	1.51 mm						–
	240	0.8 mm, perimeter	19 × 19	1.51 mm						
	304	0.8 mm, perimeter	19 × 19	1.51 mm				○	○	
PBGA	256	1.27 mm, perimeter	27 × 27	2.13 mm						–
	313	1.27 mm, staggered	35 × 35	2.33 mm					–	–
	352	1.27 mm, perimeter	35 × 35	2.33 mm						

Remarks 1. ○: Already shifted, Blank: Under study, –: Cannot be used
 2. μ PD653xx: 3-layer product, μ PD655xx: 4-layer product

List of Packages

Dual power supply

(3/4)

Package	Number of Pins	Lead Pitch	Body Size (mm)	Body Thickness	μ PD65361	μ PD65362	μ PD65363	μ PD65364	μ PD65365	μ PD65366
					μ PD65561	μ PD65562	μ PD65563	μ PD65564	μ PD65565	μ PD65566
TQFP	64	0.5 mm	10 × 10	1.00 mm	○	–	–	–	–	–
	80	0.5 mm	12 × 12	1.00 mm		–	–	–	–	–
	100	0.5 mm	14 × 14	1.00 mm				–	–	–
	120	0.4 mm	14 × 14	1.00 mm	–			–	–	–
LQFP	100	0.5 mm	14 × 14	1.40 mm			○	–	–	–
	144	0.5 mm	20 × 20	1.40 mm	–	–		–	–	–
TBGA ^{Note}	256	1.27 mm, perimeter	27 × 27	1.40 mm	–	–	–			
	352	1.27 mm, perimeter	35 × 35	1.40 mm	–	–	–	–	–	
	420	1.27 mm, perimeter	35 × 35	1.40 mm	–	–	–	–	–	–
	500	1.27 mm, perimeter	40 × 40	1.40 mm	–	–	–	–	–	–
	576	1.27 mm, perimeter	40 × 40	1.40 mm	–	–	–	–	–	–

Note With heat spreader

- Remarks** 1. ○: Already shifted, Blank: Under study, –: Cannot be used
 2. μ PD653xx: 3-layer product, μ PD655xx: 4-layer product

Dual power supply

(4/4)

Package	Number of Pins	Lead Pitch	Body Size (mm)	Body Thickness	μ PD65367	μ PD65368	μ PD65369	μ PD65370	μ PD65371
					μ PD65567	μ PD65568	μ PD65569	μ PD65570	μ PD65571
TQFP	64	0.5 mm	10 × 10	1.00 mm	–	–	–	–	–
	80	0.5 mm	12 × 12	1.00 mm	–	–	–	–	–
	100	0.5 mm	14 × 14	1.00 mm	–	–	–	–	–
	120	0.4 mm	14 × 14	1.00 mm	–	–	–	–	–
LQFP	100	0.5 mm	14 × 14	1.40 mm	–	–	–	–	–
	144	0.5 mm	20 × 20	1.40 mm	–	–	–	–	–
TBGA ^{Note}	256	1.27 mm, perimeter	27 × 27	1.40 mm					
	352	1.27 mm, perimeter	35 × 35	1.40 mm	○	○		○	○
	420	1.27 mm, perimeter	35 × 35	1.40 mm	○				
	500	1.27 mm, perimeter	40 × 40	1.40 mm	–	○	○	○	○
	576	1.27 mm, perimeter	40 × 40	1.40 mm	–	–	○		

Note With heat spreader

- Remarks** 1. ○: Already shifted, Blank: Under study, –: Cannot be used
 2. μ PD653xx: 3-layer product, μ PD655xx: 4-layer product

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Internal 1.8 V

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	1.8 V	-0.5 to +2.5	V
		3.3 V	-0.5 to +4.6	V
I/O voltage	V_I/V_O	$V_I/V_O < V_{DD} + 0.15 \text{ V}$ $V_I/V_O < V_{DD} + 0.5 \text{ V}$	-0.5 to +2.5	V
1.8 V input buffer 3.3 V input buffer			-0.5 to +4.6	V
Output current	I_O		10	mA
$I_{OL} = 3.0 \text{ mA}$			20	mA
$I_{OL} = 6.0 \text{ mA}$			30	mA
$I_{OL} = 9.0 \text{ mA}$ $I_{OL} = 12.0 \text{ mA}$			40	mA
Operating ambient temperature	T_A		-40 to +85	°C
Storage temperature	T_{stg}		-65 to +150	°C

Internal 2.5 V

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}	2.5 V	-0.5 to +3.6	V
		3.3 V	-0.5 to +4.6	V
I/O voltage	V_I/V_O	$V_I/V_O < V_{DD} + 0.3 \text{ V}$ $V_I/V_O < V_{DD} + 0.5 \text{ V}$	-0.5 to +3.6	V
2.5 V input buffer 3.3 V input buffer			-0.5 to +4.6	V
Output current	I_O		10	mA
$I_{OL} = 3.0 \text{ mA}$			20	mA
$I_{OL} = 6.0 \text{ mA}$			30	mA
$I_{OL} = 9.0 \text{ mA}$			40	mA
$I_{OL} = 12.0 \text{ mA}$			55	mA
$I_{OL} = 18.0 \text{ mA}$ $I_{OL} = 24.0 \text{ mA}$			70	mA
Operating ambient temperature	T_A		-40 to +85	°C
Storage temperature	T_{stg}		-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Except for buffers with the fail-safe function, 1.8 V, 2.5 V or 3.3 V must be applied to the I/O pins only after applying the power supply voltage.

Recommended Operating Range

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Power supply voltage	V _{DD}	1.8 V	1.65	1.8	1.95	V	
		2.5 V	2.3	2.5	2.7	V	
		3.3 V	3.0	3.3	3.6	V	
High-level input voltage	V _{IH}	1.8 V input buffer	0.65V _{DD}		V _{DD}	V	
Low-level input voltage	V _{IL}		0		0.35V _{DD}	V	
Positive trigger voltage	V _P		Schmitt input	0.7		1.5	V
Negative trigger voltage	V _N			0.4		1.1	V
Hysteresis voltage	V _H			0.1		0.6	V
High-level input voltage	V _{IH}	2.5 V input buffer	1.7		V _{DD}	V	
Low-level input voltage	V _{IL}			0		0.7	V
Positive trigger voltage	V _P		Schmitt input	0.9		1.7	V
Negative trigger voltage	V _N			0.6		1.4	V
Hysteresis voltage	V _H			0.1		0.6	V
High-level input voltage	V _{IH}	3.3 V input buffer	0.5V _{DD}		V _{DD}	V	
Low-level input voltage	V _{IL}			0		0.3V _{DD}	V
Positive trigger voltage	V _P		Schmitt input	1.5		2.4	V
Negative trigger voltage	V _N			0.8		1.8	V
Hysteresis voltage	V _H			0.2		1.0	V
Input rise time	t _{ri}	Normal input	0		200	ns	
Input fall time	t _{fi}			0		200	ns
Input rise time	t _{ri}	Schmitt input	0		10	ms	
Input fall time	t _{fi}			0		10	ms

Remark When a separate parameter is not provided for internal 2.5 V, the value is the same as internal 1.8 V.

DC Characteristics

(1/4)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Static current consumption ^{Note} Internal 1.8 V	μ PD65301, μ PD65341, μ PD65501, μ PD65541 μ PD65321, μ PD65361, μ PD65521, μ PD65561	I _{DD} S	V _I = V _{DD} or GND			180	μ A
	μ PD65302, μ PD65342, μ PD65502, μ PD65542 μ PD65322, μ PD65362, μ PD65522, μ PD65562	I _{DD} S	V _I = V _{DD} or GND			210	μ A
	μ PD65303, μ PD65343, μ PD65503, μ PD65543 μ PD65323, μ PD65363, μ PD65523, μ PD65563	I _{DD} S	V _I = V _{DD} or GND			270	μ A
	μ PD65304, μ PD65344, μ PD65504, μ PD65544 μ PD65324, μ PD65364, μ PD65524, μ PD65564	I _{DD} S	V _I = V _{DD} or GND			330	μ A
	μ PD65305, μ PD65345, μ PD65505, μ PD65545 μ PD65325, μ PD65365, μ PD65525, μ PD65565 μ PD65306, μ PD65346, μ PD65506, μ PD65546 μ PD65326, μ PD65366, μ PD65526, μ PD65566	I _{DD} S	V _I = V _{DD} or GND			420	μ A
	μ PD65307, μ PD65347, μ PD65507, μ PD65547 μ PD65327, μ PD65367, μ PD65527, μ PD65567	I _{DD} S	V _I = V _{DD} or GND			540	μ A
	μ PD65308, μ PD65348, μ PD65508, μ PD65548 μ PD65328, μ PD65368, μ PD65528, μ PD65568	I _{DD} S	V _I = V _{DD} or GND			660	μ A
	μ PD65309, μ PD65349, μ PD65509, μ PD65549 μ PD65329, μ PD65369, μ PD65529, μ PD65569	I _{DD} S	V _I = V _{DD} or GND			750	μ A
	μ PD65310, μ PD65350, μ PD65510, μ PD65550 μ PD65330, μ PD65370, μ PD65530, μ PD65570	I _{DD} S	V _I = V _{DD} or GND			870	μ A
	μ PD65311, μ PD65351, μ PD65511, μ PD65551 μ PD65331, μ PD65371, μ PD65531, μ PD65571	I _{DD} S	V _I = V _{DD} or GND				

Note When using I/O blocks (etc.) with pull-up/pull-down resistors incorporated, the static current consumption increases.

Remark The + and – signs of the current values in the table indicate the direction of the current. Current flowing into a device is indicated by +; current flowing out is indicated by –.

DC Characteristics

(2/4)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Static current consumption ^{Note} Internal 2.5 V	μ PD65301, μ PD65341, μ PD65501, μ PD65541	I_{DD5}	$V_i = V_{DD}$ or GND			180	μ A
	μ PD65321, μ PD65361, μ PD65521, μ PD65561						
	μ PD65302, μ PD65342, μ PD65502, μ PD65542						
	μ PD65322, μ PD65362, μ PD65522, μ PD65562						
	μ PD65303, μ PD65343, μ PD65503, μ PD65543	I_{DD5}	$V_i = V_{DD}$ or GND			240	μ A
	μ PD65323, μ PD65363, μ PD65523, μ PD65563						
	μ PD65304, μ PD65344, μ PD65504, μ PD65544	I_{DD5}	$V_i = V_{DD}$ or GND			300	μ A
	μ PD65324, μ PD65364, μ PD65524, μ PD65564						
	μ PD65305, μ PD65345, μ PD65505, μ PD65545	I_{DD5}	$V_i = V_{DD}$ or GND			360	μ A
	μ PD65325, μ PD65365, μ PD65525, μ PD65565						
	μ PD65306, μ PD65346, μ PD65506, μ PD65546						
	μ PD65326, μ PD65366, μ PD65526, μ PD65566						
	μ PD65307, μ PD65347, μ PD65507, μ PD65547	I_{DD5}	$V_i = V_{DD}$ or GND			480	μ A
	μ PD65327, μ PD65367, μ PD65527, μ PD65567						
μ PD65308, μ PD65348, μ PD65508, μ PD65548	I_{DD5}	$V_i = V_{DD}$ or GND			600	μ A	
μ PD65328, μ PD65368, μ PD65528, μ PD65568							
μ PD65309, μ PD65349, μ PD65509, μ PD65549	I_{DD5}	$V_i = V_{DD}$ or GND			750	μ A	
μ PD65329, μ PD65369, μ PD65529, μ PD65569							
μ PD65310, μ PD65350, μ PD65510, μ PD65550	I_{DD5}	$V_i = V_{DD}$ or GND			870	μ A	
μ PD65330, μ PD65370, μ PD65530, μ PD65570							
μ PD65311, μ PD65351, μ PD65511, μ PD65551	I_{DD5}	$V_i = V_{DD}$ or GND			1020	μ A	
μ PD65331, μ PD65371, μ PD65531, μ PD65571							

Note When using I/O blocks (etc.) with pull-up/pull-down resistors incorporated, the static current consumption increases.

Remark The + and – signs of the current values in the table indicate the direction of the current. Current flowing into a device is indicated by +; current flowing out is indicated by –.

DC Characteristics

(3/4)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
OFF-state output current	1.8 V output	loz	$V_O = V_{DD}$ or GND			±10	μ A	
	2.5 V output	loz	$V_O = V_{DD}$ or GND			±10	μ A	
	3.3 V output	loz	$V_O = V_{DD}$ or GND			±10	μ A	
Output short-circuit current ^{Note 1}		los	$V_O = \text{GND}$			-250	mA	
Input leakage current 1.8 V buffer	Normal input	li	$V_I = V_{DD}$ or GND			±10	μ A	
	With pull-up resistor (100 kΩ)	li	$V_I = \text{GND}$	-5	-18	-49	μ A	
	With pull-up resistor (5 kΩ)	li	$V_I = \text{GND}$	-107	-333	-900	μ A	
	With pull-down resistor (100 kΩ)	li	$V_I = V_{DD}$	5	22	39	μ A	
Input leakage current 2.5 V buffer	Normal input	li	$V_I = V_{DD}$ or GND			±10	μ A	
	With pull-up resistor (100 kΩ)	li	$V_I = \text{GND}$	-8	-22	-56	μ A	
	With pull-up resistor (5 kΩ)	li	$V_I = \text{GND}$	-175	-475	-1174	μ A	
	With pull-down resistor (100 kΩ)	li	$V_I = V_{DD}$	7	22	62	μ A	
Input leakage current 3.3 V buffer	Normal input	li	$V_I = V_{DD}$ or GND			±10	μ A	
	With pull-up resistor (100 kΩ)	li	$V_I = \text{GND}$	-14	-41	-58	μ A	
	With pull-up resistor (5 kΩ)	li	$V_I = \text{GND}$	-240	-702	-984	μ A	
	With pull-down resistor (100 kΩ)	li	$V_I = V_{DD}$	12	34	46	μ A	
Pull-up resistor ^{Note 2}	1.8 V buffer	100 kΩ	R _{PU}	$V_I = \text{GND}$	40	102	292	kΩ
		5 kΩ	R _{PU}	$V_I = \text{GND}$	2	5	16	kΩ
	2.5 V buffer	100 kΩ	R _{PU}	$V_I = \text{GND}$	49	111	279	kΩ
		5 kΩ	R _{PU}	$V_I = \text{GND}$	2	5	14	kΩ
	3.3 V buffer	100 kΩ	R _{PU}	$V_I = \text{GND}$	33	81	221	kΩ
		5 kΩ	R _{PU}	$V_I = \text{GND}$	2	5	13	kΩ
Pull-down resistor ^{Note 2}	1.8 V buffer 100 kΩ		R _{PD}	$V_I = V_{DD}$	51	122	319	kΩ
	2.5 V buffer 100 kΩ		R _{PD}	$V_I = V_{DD}$	43	113	297	kΩ
	3.3 V buffer 100 kΩ		R _{PD}	$V_I = V_{DD}$	42	97	240	kΩ

Notes 1. The output short-circuit time is 1 second or less per pin of the LSI.

2. The pull-up and pull-down resistances vary depending on the input and output voltages.

Remarks 1. The + and - signs of the current values in the table indicate the direction of the current. Current flowing into a device is indicated by +; current flowing out is indicated by -.

2. When a separate parameter is not provided for internal 2.5 V, the value is the same as internal 1.8 V.

DC Characteristics

(4/4)

	Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Low-level output current ^{Note}	1.8 V buffer	3.0 mA type	I_{OL}	$V_{OL} = 0.4 \text{ V}$	3			mA
		6.0 mA type	I_{OL}	$V_{OL} = 0.4 \text{ V}$	6			mA
		9.0 mA type	I_{OL}	$V_{OL} = 0.4 \text{ V}$	9			mA
		12.0 mA type	I_{OL}	$V_{OL} = 0.4 \text{ V}$	12			mA
	2.5 V buffer	3.0 mA type	I_{OL}	$V_{OL} = 0.4 \text{ V}$	3			mA
		6.0 mA type	I_{OL}	$V_{OL} = 0.4 \text{ V}$	6			mA
		9.0 mA type	I_{OL}	$V_{OL} = 0.4 \text{ V}$	9			mA
		12.0 mA type	I_{OL}	$V_{OL} = 0.4 \text{ V}$	12			mA
		18.0 mA type	I_{OL}	$V_{OL} = 0.4 \text{ V}$	18			mA
		24.0 mA type	I_{OL}	$V_{OL} = 0.4 \text{ V}$	24			mA
	3.3 V buffer	3.0 mA type	I_{OL}	$V_{OL} = 0.4 \text{ V}$	3			mA
		6.0 mA type	I_{OL}	$V_{OL} = 0.4 \text{ V}$	6			mA
9.0 mA type		I_{OL}	$V_{OL} = 0.4 \text{ V}$	9			mA	
12.0 mA type		I_{OL}	$V_{OL} = 0.4 \text{ V}$	12			mA	
High-level output current ^{Note}	1.8 V buffer	3.0 mA type	I_{OH}	$V_{OH} = 1.4 \text{ V}$	-3			mA
		6.0 mA type	I_{OH}	$V_{OH} = 1.4 \text{ V}$	-6			mA
		9.0 mA type	I_{OH}	$V_{OH} = 1.4 \text{ V}$	-9			mA
		12.0 mA type	I_{OH}	$V_{OH} = 1.4 \text{ V}$	-12			mA
	2.5 V buffer	3.0 mA type	I_{OH}	$V_{OH} = 1.4 \text{ V}$	-3			mA
		6.0 mA type	I_{OH}	$V_{OH} = 1.4 \text{ V}$	-6			mA
		9.0 mA type	I_{OH}	$V_{OH} = 1.4 \text{ V}$	-9			mA
		12.0 mA type	I_{OH}	$V_{OH} = 1.4 \text{ V}$	-12			mA
		18.0 mA type	I_{OH}	$V_{OH} = 1.4 \text{ V}$	-18			mA
		24.0 mA type	I_{OH}	$V_{OH} = 1.4 \text{ V}$	-24			mA
	3.3 V buffer	3.0 mA type	I_{OH}	$V_{OH} = 2.6 \text{ V}$	-3			mA
		6.0 mA type	I_{OH}	$V_{OH} = 2.6 \text{ V}$	-6			mA
9.0 mA type		I_{OH}	$V_{OH} = 2.6 \text{ V}$	-9			mA	
12.0 mA type		I_{OH}	$V_{OH} = 2.6 \text{ V}$	-12			mA	
Low-level output voltage	1.8 V buffer		V_{OL}	$I_{OL} = 0 \text{ mA}$			0.1	V
	2.5 V buffer		V_{OL}	$I_{OL} = 0 \text{ mA}$			0.1	V
	3.3 V buffer		V_{OL}	$I_{OL} = 0 \text{ mA}$			0.1	V
High-level output voltage	1.8 V buffer		V_{OH}	$I_{OH} = 0 \text{ mA}$	$V_{DD}-0.1$			V
	2.5 V buffer		V_{OH}	$I_{OH} = 0 \text{ mA}$	$V_{DD}-0.1$			V
	3.3 V buffer		V_{OH}	$I_{OH} = 0 \text{ mA}$	$V_{DD}-0.1$			V

Note All the buffers with the same output drive capability have the same specifications.

Remarks 1. The + and – signs of the current values in the table indicate the direction of the current. Current flowing into a device is indicated by +; current flowing out is indicated by –.

2. When a separate parameter is not provided for internal 2.5 V, the value is the same as internal 1.8 V.

AC Characteristics

The values in the table below refer to when the supply voltage of the internal gate array block is 1.8 ± 0.15 V.

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Maximum toggle frequency	f_{tog}	Internal toggle F/F (fan-out = 2)	436			MHz	
Maximum operating frequency	f_{MAX}				66 ^{Note}	MHz	
Propagation delay time	t_{PD}	Internal gate					
		Fan-out = 1, wiring length = 0 mm		129		ps	
		Fan-out = 1, standard wiring length		163		ps	
		Standard load		146		ps	
		Internal gate (power gate)					
		Fan-out = 1, standard wiring length		139		ps	
		Standard load		126		ps	
		1.8 V input buffer					
Fan-out = 1, standard wiring length		243		ps			
Standard load		239		ps			
3.3 V input buffer		Fan-out = 1, standard wiring length		352		ps	
		Standard load		342		ps	
1.8 V output buffer (FO0111)		$C_L = 15$ pF, $I_{OL} = 9$ mA		1289		ps	
		3.3 V output buffer (FO0113)					
		$C_L = 15$ pF, $I_{OL} = 9$ mA		1556		ps	
Output rise time	t_r	1.8 V output buffer (FO0111)					
		$C_L = 15$ pF, $I_{OL} = 9$ mA		1415		ps	
		3.3 V output buffer (FO0113)					
		$C_L = 15$ pF, $I_{OL} = 9$ mA		1123		ps	
Output fall time	t_f	1.8 V output buffer (FO0111)					
		$C_L = 15$ pF, $I_{OL} = 9$ mA		1526		ps	
		3.3 V output buffer (FO0113)					
		$C_L = 15$ pF, $I_{OL} = 9$ mA		1114		ps	

Note Contact NEC Electronics if this value is exceeded.

Remark Standard load : Fan-out = 2, wiring length = 0 mm
Standard wiring length : 145 μm /1 pin-pair

AC Characteristics

The values in the table below refer to when the supply voltage of the internal gate array block is 2.5 ± 0.2 V.

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Maximum toggle frequency	f_{tog}	Internal toggle F/F (fan-out = 2)	826			MHz	
Maximum operating frequency	f_{MAX}				133 ^{Note}	MHz	
Propagation delay time	t_{PD}	Internal gate					
		Fan-out = 1, wiring length = 0 mm		85		ps	
		Fan-out = 1, standard wiring length		113		ps	
		Standard load		99		ps	
		Internal gate (power gate)					
		Fan-out = 1, standard wiring length		91		ps	
		Standard load		83		ps	
		2.5 V input buffer					
Fan-out = 1, standard wiring length		173		ps			
Standard load		169		ps			
3.3 V input buffer	Fan-out = 1, standard wiring length		294		ps		
		Standard load	289		ps		
2.5 V output buffer (FO0122)	$C_L = 15$ pF, $I_{OL} = 9$ mA		905		ps		
		3.3 V output buffer (FO0123)		1224		ps	
3.3 V output buffer (FO0123)	$C_L = 15$ pF, $I_{OL} = 9$ mA						
Output rise time	t_r	2.5 V output buffer (FO0122)					
		$C_L = 15$ pF, $I_{OL} = 9$ mA		1359		ps	
3.3 V output buffer (FO0123)	$C_L = 15$ pF, $I_{OL} = 9$ mA						
				1059		ps	
Output fall time	t_f	2.5 V output buffer (FO0122)					
		$C_L = 15$ pF, $I_{OL} = 9$ mA		1441		ps	
3.3 V output buffer (FO0123)	$C_L = 15$ pF, $I_{OL} = 9$ mA						
				983		ps	

Note Contact NEC Electronics if this value is exceeded.

Remark Standard load : Fan-out = 2, wiring length = 0 mm
Standard wiring length : 145 μ m/1 pin-pair

DEVELOPMENT TOOLS

Easy interface with your EWS or PC

Users can choose the following tools to their environment.

Caution Some functions may not be supported. Make it sure before use.

OPENCAD™ Configuration Tool

Function	NEC Tool	Interface Data	Commercially Available Tool Interface
Function simulator	–	• Netlist PWC/EDIF(2.0.0)/	ModelSim™/Verilog-XL™/ NC-Verilog™/VCS™
Schematic editor	Vdraw	Verilog™ HDL	–
Logic synthesis	–		Design Compiler®
Gate level simulator ^{Note 1}	V.sim	• Test pattern ALBA	ModelSim/Verilog-XL/NC-Verilog/ VCS
Formal verifier	–		Formality®/Tuxedo™-LEC/ Conformal™-LEC
STA ^{Note 1}	Tiara	• Delay information file	PrimeTime®
Fault simulator ^{Note 2}	C.FGRADE		–
Design for test	NEC_SCAN2/ NEC_BSCAN2/ NEC_BIST/TESTBUS	• Constraints file	DFTCompiler/TetraMAX®
Floor planner ^{Note 3}	CBIC : ace_floorplan GA : Galet		–
Placement and Routing ^{Note 3}	Galet		Silicon Ensemble™

Notes 1. Sign-off tool

2. Tool not supported in the HP™ version

3. Stand-alone tool

Remark Platform : SUN™(Solaris™)/HP(HP-UX™)

GUI : X11R5/Motif™ 1.2

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