Synchronous buck PWM DC/DC with Dual Voltage Control Mode

General Description

The RT8100A is an advanced DC/DC synchronous buck PWM controller with several innovative functions for specific customer' s ASIC only. The part features RichTek' s innovative design and topology say "analogous current mode" for current sensing and full functions for various applications including adjustable soft start, free-run and adjustable operation frequency and enable; the part is with design of 12V+12V boot strapped driver which is capable to drive up to 20Amp output current; moreover the part is with implementation of accuracy DCR current sensing topology. There are several specific features implemented and reserved for the specific customer' s special applications including dual V_{CORE} control mode including tracking and stand-alone mode, and output current indication. The part is proposed with a small footprint of VQFN-16L 3x3 package.

Ordering Information

RT8100A □ □

- Package Type
  QV : VQFN-16L 3x3 (V-Type)
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)

Note :

Richtek Pb-free and Green products are :

- ▸RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▸Suitable for use in SnPb or Pb-free soldering processes.
- ▸100% matte tin (Sn) plating.

Features

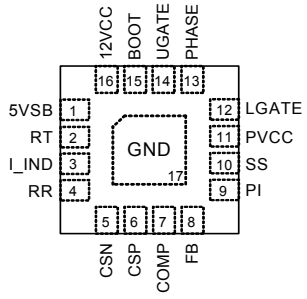
- **Analogous Current Mode Design**
- **2.5V to 12V Switching Source Power**
- **0.8V to 3.3V Output Voltage Regulation**
- **Adjustable V_{IN} Feed-Forward Ramp Slope**
- **Adjustable Operation Frequency**
- **Precise Core Voltage Regulation**
- **Precise DCR Current Sensing with High Quality Capacitor, X7R**
- **± 1.5% System Accuracy**
- **Input Voltage : 12V and 5V Bias**
- **Enable Function**
- **RoHS Compliant and 100% Lead (Pb)-Free**
- **Over Current Protection**
- **External Soft Start Setting**
- **Operation Frequency up to 1.0MHz**
- **Dual Mode Voltage Control**
  - ▸**Tracking Mode**
  - ▸**Stand-Alone Mode**
- **Output Current Indication**
- **16-Lead VQFN Package**

Applications

- MB memory and chipset core power
- Middle-high graphic card GPU and memory core power
- General-purpose fields including server, NB, bare-bone and mini-system

Pin Configurations

(TOP VIEW)



VQFN-16L 3X3

Typical Application Circuit

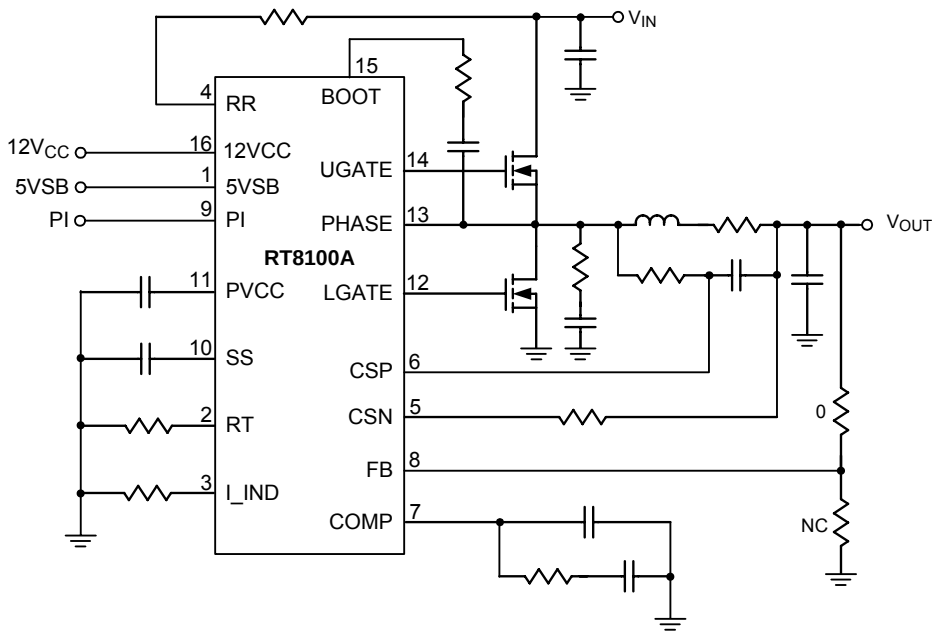


Figure 1. 12V-5V PI Application Circuit

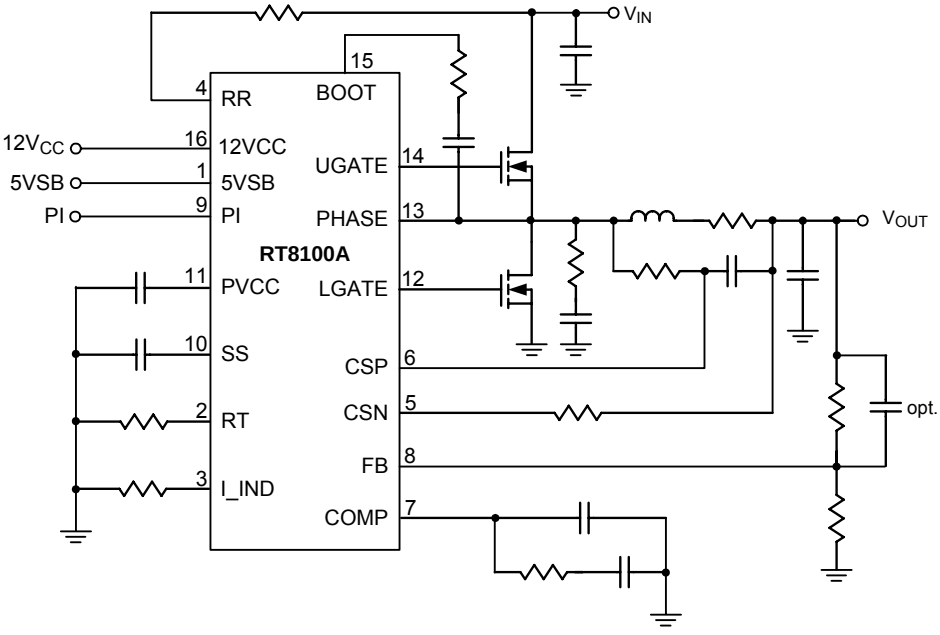


Figure 2. 12V-5V Internal V_{REF} Application Circuit

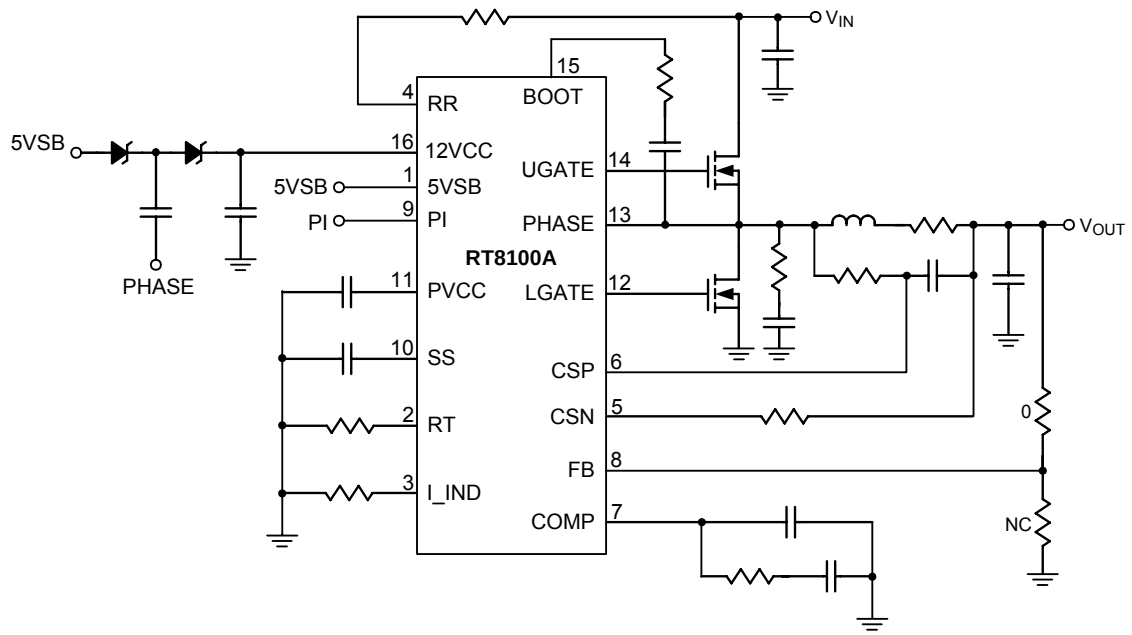


Figure 3. Single 5V PI Application Circuit

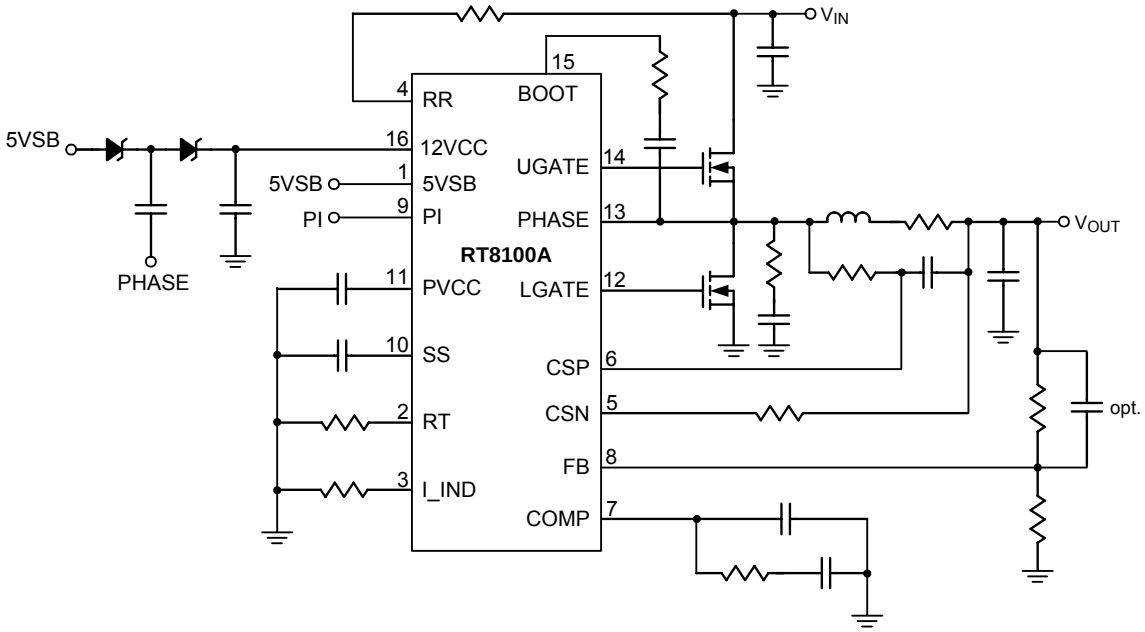


Figure 4. Single 5V Internal V_{REF} Application Circuit

Functional Pin Description

5VSB(Pin 1), 12VCC (Pin 16)

The 5VSB pin is the external standby 5V power. The 12VCC pin is the external 12V power.

RT (Pin 2)

Timing Resistor. Connect a resistor from RT to GND to set the clock frequency. The free running frequency is 200kHz.

I_IND (Pin 3)

Current indicating pin. This pin uses voltage level to indicate the current of inductor. Connect this pin with a resistor to ground to set the voltage.

$I_{\_IND} = 4 \times I_X$

I_X : Internal GM sensed current, please refer to the Application Information.

RR (Pin 4)

Ramp resistor. This pin is used to set the ramp voltage. Connecting a resistor from this pin to the converter input power sets the ramping slope of the control loop of the converter. Since it is connected to the converter input power, the ramp slope is input-feed-forwarded. As V_{IN} > 1.8V, RR pin is enabled for ramp setting.

CSN (Pin 5)

Current Sense Negative Input. This pin is negative input node of the current sense amplifier used for DCR current sensing. Connect this pin with a resistor to the output node.

CSP (Pin 6)

Current Sense Positive Input. This pin is positive input nodes of the current sense amplifier used for DCR current sensing. Connect this pin to the junction of the filter resistor and capacitor.

COMP (Pin 7)

Compensation Pin. This pin is the output node of the error amplifier.

FB (Pin 8)

Feedback Pin. This pin is negative input pin of the error amplifier.

PI (Pin 9)

External reference voltage pin. This pin sets the voltage of FB pin when close loop.

Stand_Alone : Pull high to 5VSB

Tracking : Connect to external reference voltage. The PI pin will sink 4mA for 15μs when the OCP function acts.

SS (Pin 10)

Soft-start Pin. This pin provides soft-start function for its controller. The COMP voltage of the converter follows the ramping voltage on the SS pin.

PVCC (Pin 11)

Driver Power.

LGATE (Pin 12)

Lower Gate Drive. This pin drives the gate of the lowside MOSFET.

PHASE (Pin 13)

This pin is return node of the high-side driver. Connect this pin to high-side MOSFET source together with the low-side MOSFET drain and the inductor.

UGATE (Pin 14)

Upper Gate Drive. This pin drives the gate of the highside MOSFET.

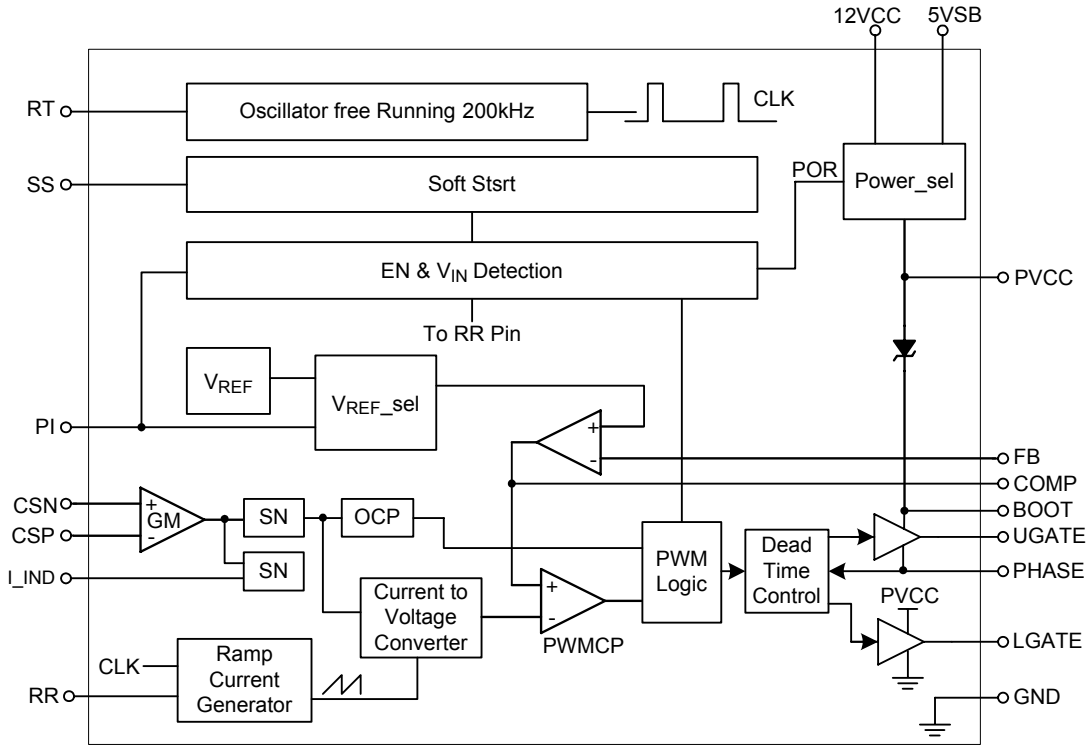
BOOT (Pin 15)

Bootstrap Power Pin. This pin powers the high-side MOSFET driver. Connect this pin to the junction of the bootstrap capacitor.

GND [Exposed Pad (17)]

The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Operation

RT8100A is a highly flexible, high performance and high precision synchronous buck controller specifically designed for high-end graphic core power supply as well as DDR applications, with highly reduced external components and costs.

RT8100A uses RichTek proprietary Analogous Current Mode™ topology which mimics the traditional peak current mode by sensing the valley current of the inductor via DCR sensing techniques and simulating the current ramp with an artificial ramp set externally. The Analogous Current Mode topology benefits all the advantages of peak current mode converter with much higher noise immunity than conventional one. Since the compensation is easier and with less constraint than that in voltage mode, using low ESR output capacitor as MLCC is possible, which therefore dramatically reduce the board size as well as the cost and has better transient response due to higher control bandwidth. RT8100A also adopts V_{IN} feedfoward for ramp setting, which decreases the complexity for compensation by keeping the modulator gain constant along line variations.

The wide input voltage range of the converter ranges from 3.3V to 12V. The output voltage can be set from 0.8V to 3.3V with external resistor divider.

The power sequence of RT8100A includes :

1 : POR function

2 : V_{IN} power supply detection

3 : PI pin setting to enable the whole chip.

The external elements selection of RT8100A includes :

1 : RT pin resister to GND to set the operation frequency of the chip.

2 : CSN pin resister to set the current gain(ratio of inductance current I_L and sensed current Ix).

3 : RR pin resister to V_{IN} to set the slope of the V_{IN} feed forward ramp and the effective slope compensation of current mode.

4 : Use R_{CSN} resister to set the over current level.

5 : Capacitor at SS pin to set the soft-start time.

6 : Type two compensation at COMP pin.

Power on reset

The POR circuitry monitors the supply voltage of the chip. When the chip power supply exceeds 4.2V, the chip releases the reset state and works according to the settings. Once the supply voltage is lower than 4.0V, POR circuitry resets the chip.

V_{IN} detection

The V_{IN} detection circuitry monitors the switching power source when power up. As V_{IN} > 1.8V, RR pin is enabled for ramp setting and the chip is in ramp setting mode. The voltage at RR pin will be about 0.5V. Otherwise, the chip will be in V_{IN} detection mode and RR pin is disabled for ramp setting until V_{IN} > 1.8V. In V_{IN} detection mode, the UGATE and LGATE will be off and SS will be pulled low by a constant current of 10uA. The chip will enter the ramp setting mode and SS will re-softstart when V_{IN} > 1.8V.

Enable

After POR reset, the chip monitors the voltage of PI pin. When PI is higher than 0.3V, the chip is enabled. The chip is disabled when V_{PI} is lower than 0.3V. With a precise threshold voltage, the PI pin can be used for power sequence.

Soft-start

A constant current of 10uA starts to charge the capacitor connected to SS pin right after the chip has been powered up and enabled. The ramp voltage on SS pin is also used to clamp the comp voltage during soft-start, which automatically constraints the output current due to the nature of current mode topology. This brings up smaller inrush current and smooth output voltage ramp. The SS pins are also used as the timer during OCP hiccup.

Frequency setting

The converter switching frequency is programmed by connecting a resistor from the RT pin to GND. The frequency vs. R_{RT} plot is shown in “Typical Operating Characteristics”.

Output voltage setting and control

Control loops consist of an error amplifier, a pulse width modulator, current feed back components, a gate driver and power components. The internal high accuracy bias provides the reference voltage of 0.8V at the non-inverting input of both error amplifiers. The output voltage is programmed by using a voltage divider at output and feeding the voltage division back to corresponding error amplifiers. As conventional current mode PWM controller, the output voltage is locked at the V_{REF} of error amplifier and the error signal is used as the control signal of pulse width modulator. The PWM signals are generated by comparison of EA output and current ramp waves. Power stage transforms V_{IN} to output by PWM signal on-time ratio.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- 16V
- BOOT, V_{BOOT} - V_{PHASE} ---------- 16V
- PHASE to GND
  - DC ---------- –5V to 15V
  - < 200ns ---------- –10V to 30V
- BOOT to PHASE ---------- 15V
- BOOT to GND
  - DC ---------- –0.3V to V_{CC}+15V
  - < 200ns ---------- –0.3V to 42V
- UGATE ---------- V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
- LGATE ---------- GND - 0.3V to V_{CC} + 0.3V
- Input, Output or I/O Voltage ---------- GND-0.3V to 7V
- Power Dissipation, P_D @ T_A = 25°C
  - VQFN-16L 3x3 ---------- 1.47W
- Package Thermal Resistance (Note 4)
  - VQFN-16L 3x3, θ_{JA} ---------- 68°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  - HBM (Human Body Mode) ---------- 1.5kV
  - MM (Machine Mode) ---------- 150V

Recommended Operating Conditions (Note 3)

- Supply Voltage, V_{CC} ---------- 12V ± 10%
- Ambient Temperature Range ---------- 0°C to 70°C
- Junction Temperature Range ---------- 0°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input							
Power Supply Voltage		$12V_{CC}$		4.5	12	15	V
		$5V_{SB}$		--	5	--	
Power On Reset		$V_{5VSBRTH}$		3.8	4.2	4.4	V
Power On Reset Hysteresis		$V_{5VSBHYS}$		--	0.3	--	V
PI Threshold	ON	V_{EN}		--	0.3	--	V
	Hysteresis	V_{EN}		--	50	--	mV
Power Supply Current		I_{VCC}	$5V_{SB}$ = 5V, $12V_{CC}$ = 12V, V_{IN} = 0V	--	10	--	mA
Soft Start							
Soft Start Current		I_{SS}		8	10	15	μA

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Oscillator						
Free Running Frequency	f_{OSC}		170	200	230	kHz
Frequency Variation			–15	--	15	%
Frequency Range			50	200	1000	kHz
Maximum Duty Cycle			70	75	80	%
Up-Ramp Setting Pin	V_{RR}	R_{RR} = 120kΩ	0.3	0.5	0.7	V
Reference Voltage						
Feedback Voltage	V_{FB}	V_{FB} = 0.8V	--	1.5	--	%
Error Amplifier						
DC Gain			60	70	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF	6	10	--	MHz
Trans-conductance	GM	R_{LOAD} = 20kΩ	600	660	--	μA/V
MAX Current (Source & Sink)	I_{OUT}	V_{OUT} = 0.5 x V_{5VSB}	300	360	--	μA
Current Sense GM Amplifier						
Input Offset Voltage	V_{VOSGM}	R_{SENSE} = 2kΩ	–5	--	5	mV
I_{OMAX}	$I_{IOMAXGM}$	R_{SENSE} = 2kΩ	90	--	--	μA
Gate Driver						
Upper Drive Source	I_{UGATE}	BOOT – PHASE = 12V, BOOT – V_{UGATE} = 1V	0.15	0.35	--	A
Upper Drive Sink	R_{UGATE}	V_{UGATE} = 1V	--	3.5	7	Ω
Lower Drive Source	I_{LGATE}	PV_{CC} = 12V, PV_{CC} – V_{LGATE} = 1V	0.5	0.35	--	A
Lower Drive Sink	R_{LGATE}	V_{LGATE} = 1V	--	2	4	Ω
Protection						
Over Current	I_{OC}		--	80	--	μA

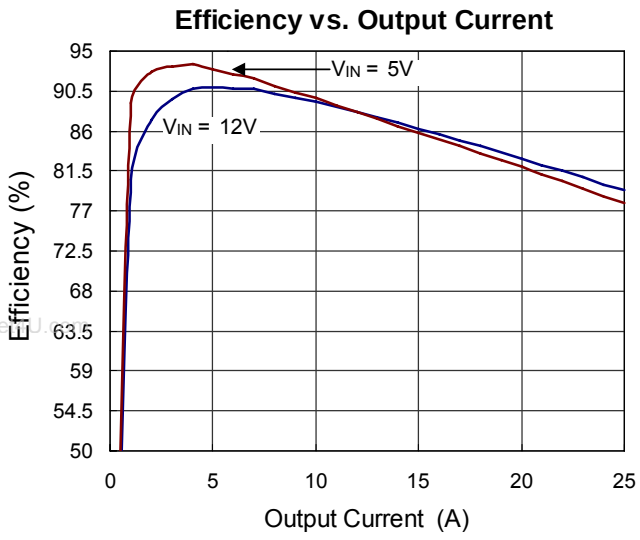
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

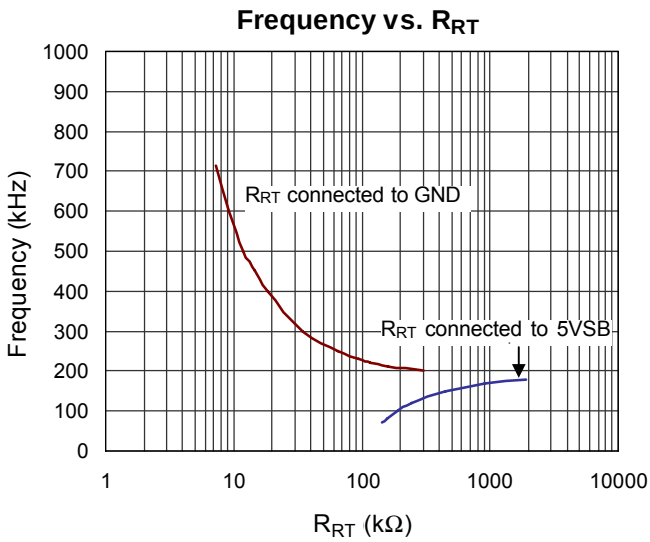
Note 2. Devices are ESD sensitive. Handling precaution recommended.

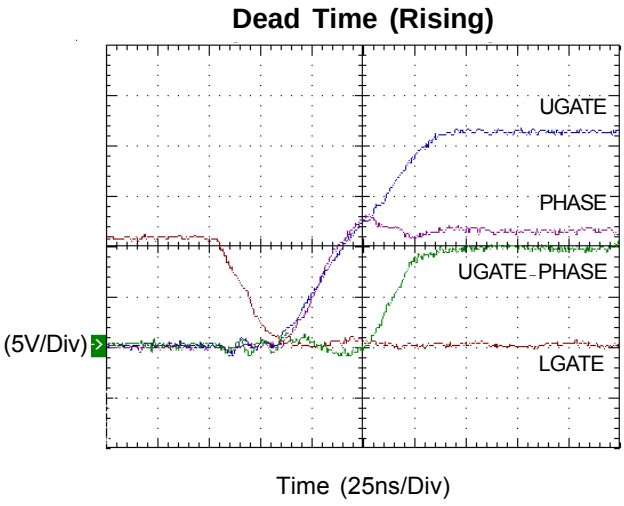
Note 3. The device is not guaranteed to function outside its operating conditions.

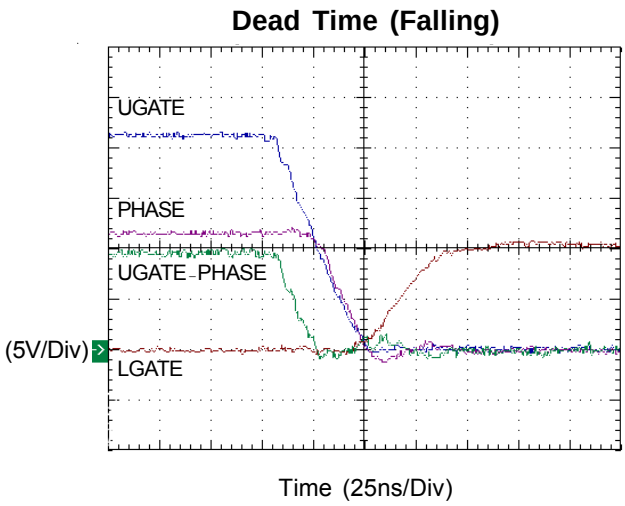
Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

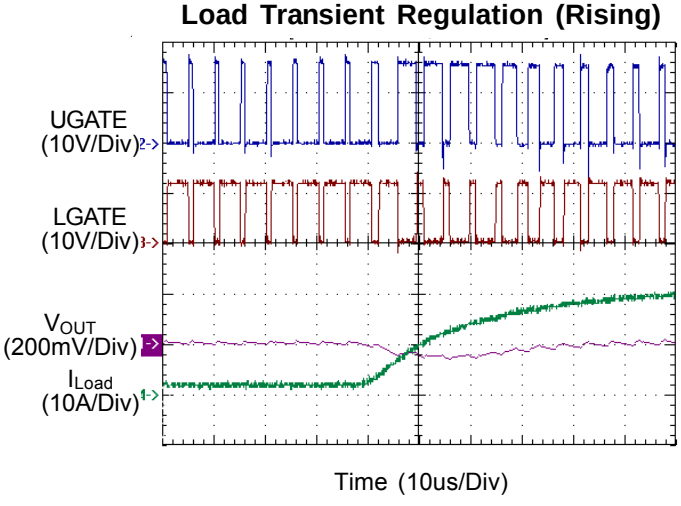
Typical Operating Characteristics

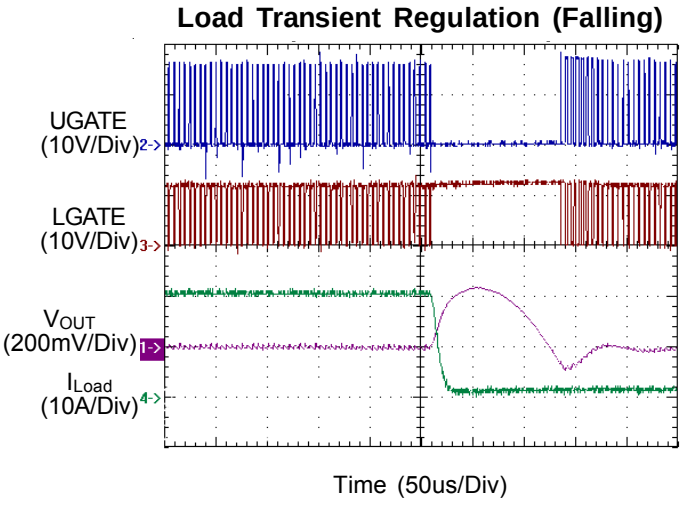




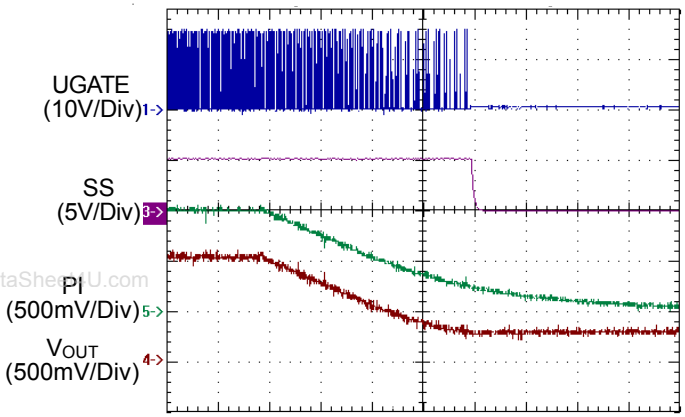




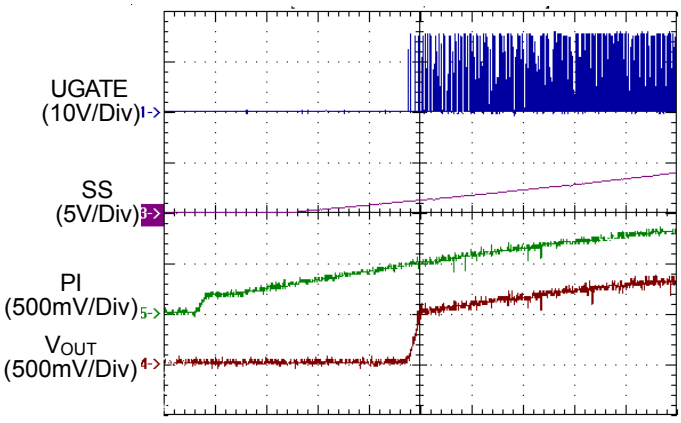




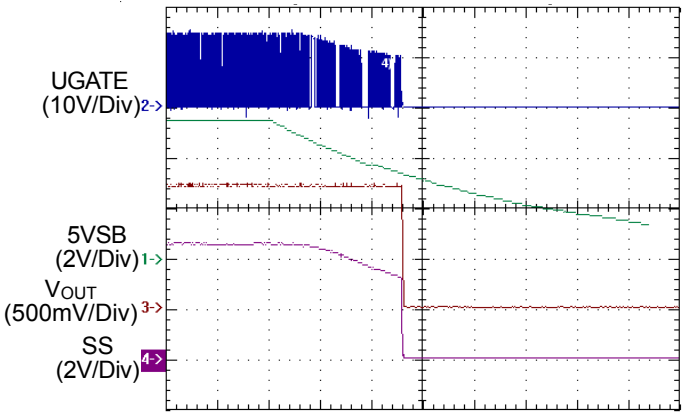
PI Power Off



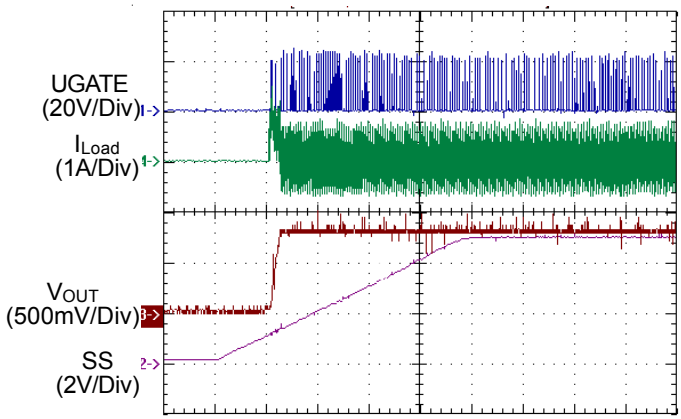
PI Power On



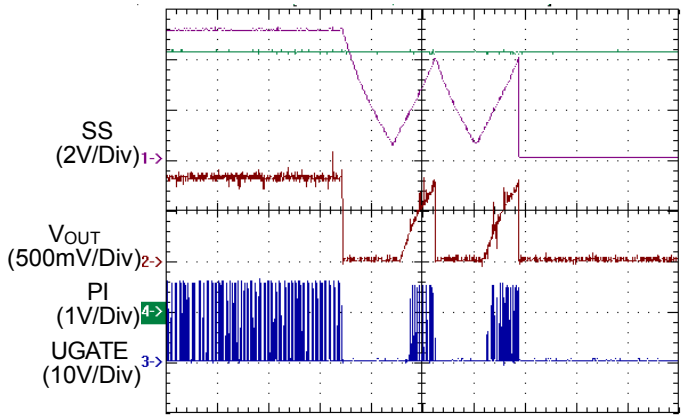
Power Off



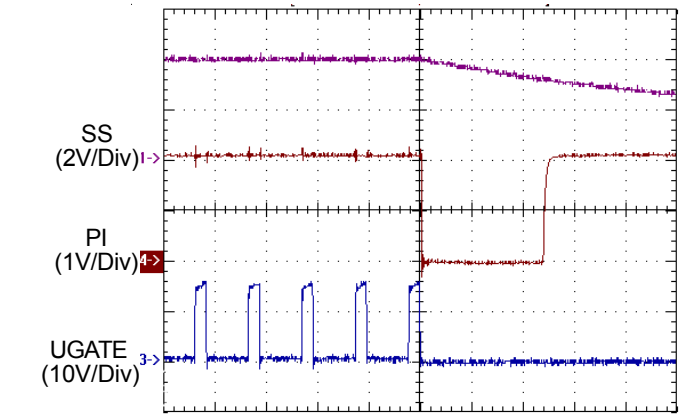
Power On

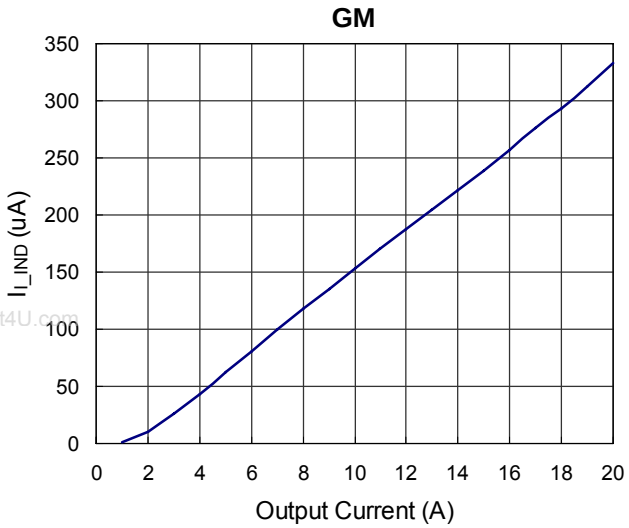


Standalone OCP



Tracking OCP





Application Information

Current Sense, Ramp Setting

RT8100A senses the inductor current through inductor DCR and feeds the current signal back to the control loop. The current sensing circuitry, as in Figure 5 consists of an RC filter, a current sensing GM together with two external resistors. The current flowing the inductor as well as the DCR causes a ripple voltage proportional to inductor ripple current across the equivalent inductor DCR as in Figure 5, The ripple voltage can be obtained using an RC filter in parallel with the inductor, if the component values satisfy the following relationships.

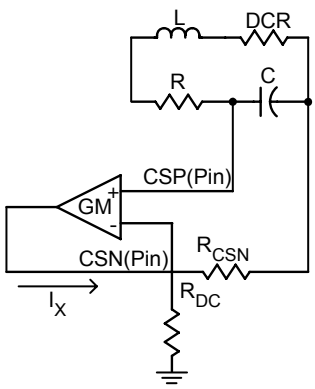


Figure 5

$$\frac{L}{DCR} = R \times C$$

The current sense GM converts the voltage drop on the capacitor in the DCR sensing network together with the resistor R_{CSN} connected from the V_{OUT} to the CSN pin. R_{CSN} defines the trans-conductance of the GM stage. An extra external resistor connected from R_{CSN} to GND is recommended to offer the capability of sensing negative inductor current in applications where negative currents are possible at light load conditions. The sensed current Ix is :

$$I_X = \frac{I_L \times DCR}{R_{CSN}} + \frac{V_{OUT}}{R_{DC}}$$, at steady state.

$$I_X = \frac{I_L \times DCR}{R_{CSN}}$$, provided R_{DC} is left opened.

The valley of the sensed current Ix is sampled and held and converted to a DC voltage as a baseline of the current feedback ramp.

The external resistor RR is used to sets the internal ramp voltage proportional to current. The simulated ramp voltage is also used to implement the slope compensation set together using a single resistor RR. The relationships between RR and the internal voltage ramp is :

$$\left(\frac{V_{IN} - V_{OUT}}{L} + k\frac{V_{OUT}}{L}\right)\frac{DCR}{R_{CSN}}15k$$

$$= \frac{V_{IN} - V_{RR}}{RR} \div 64p$$

$$RR = (V_{IN} - V_{RR}) \times \frac{R_{CSN}}{64p}$$

$$\div \left(\frac{V_{IN} - V_{OUT}}{L} + k\frac{V_{OUT}}{L}\right) \div \frac{DCR}{15k}$$

Where

V_{RR}: the voltage at RR pin to 0.5V

RR : the resistance at RR pin

k : the slope compensation coefficient, which is the ratio of the desired compensation slope to the down ramp slope.

The ramp voltage is summed up with the sensed baseline voltage to form a complete current feedback signal. The simulated ramp signal is fed to the comparator of the PWM modulator, comparing with error amplifier output to generate PWM pulses.

Gate Control

a. Before SS signal reach the bottom of the ramp voltage, UGATE and LGATE will be off.

b. If PI pin is pulled low UGATE and LGATE will be off.

c. When OC function occurs a constant current of 10μA starts to discharge the capacitor connected to SS pin right away. When OC occurs, UGATE and LGATE will be off. When the voltage at the capacitor connected to SS pin pass about 0.4V, a constant current of 10μA starts to charge the capacitor. The PWM signal is enable to pass to UGATE and LGATE.

d. When fault conditions occur or SS < 0.4V, the current sense function will be disable.

Feedback Loop Compensation

First, the ramp signal applied to the PWM comparator is proportional to the input voltage provided via the RR pin. This keeps the modulator gain constant when the input voltage varies. Second, the inductance valley current proportional signal is derived from the voltage drop across the ESR of the inductance is added to the ramp signal. This effectively creates an internal current control loop. The resistor connected to the CSN pin sets the gain in the current feedback loop. The following expression estimates the required value of the current sense resistor depending on the maximum load current and the value of the inductance DCR.

$$R_{CSN} = I_{MAX} \times \frac{DCR}{80\mu A}$$

1) Modulator Frequency Equations

RT8100A is a analogous current mode buck converter using the high gain error amplifier with transconductance (OTA, Operational Transconductance Amplifier), as Figure 6 shown.

The Transconductance :

$$GM = \frac{\Delta I_{OUT}}{\Delta V_M}$$

ΔV_M = (EA+) - (EA-) ; ΔI_{OUT} = E/A output current.

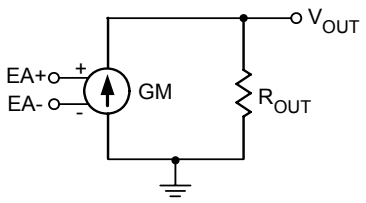


Figure 6. OTA Topology

This transfer function of OTA is dominated by a higher DC gain and the output filter (L_{OUT} and C_{OUT}) with a double pole frequency at F_{LC} and a zero at F_{ESR}. The DC gain of the modulator is the input voltage (V_{IN}) divided by the peak to peak oscillator voltage V_{RAMP}.

The first step is to calculate the complex conjugate poles contributed by the LC output filter.

The output LC filter introduces a double pole, 40dB/decade gain slope above its corner resonant frequency, and a total phase lag of 180 degrees. The resonant frequency of the LC filter expressed as follows :

$$F_{P(LC)} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

The next step of compensation design is to calculate the ESR zero. The ESR zero is contributed by the ESR associated with the output capacitance. Note that this requires that the output capacitor should have enough ESR to satisfy stability requirements. The ESR zero of the output capacitor expressed as follows :

$$F_{Z(ESR)} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

2) Compensation Frequency Equations

The compensation network consists of the error amplifier and the impedance networks Z_C and Z_F as Figure 7 shown.

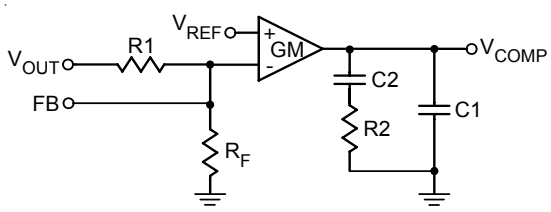


Figure 7. Compensation Loop

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C2}$$

$$F_{P1} = \frac{1}{2\pi \times R1 \times C1}$$

$$F_{P2} = \frac{1}{2\pi \times R2 \times \left(\frac{C1 \times C2}{C1 + C2}\right)}$$

Figure 8 shows the DC-DC converter's gain vs. frequency. The compensation gain uses external impedance networks ZC and ZF to provide a stable, high bandwidth loop. High crossover frequency is desirable for fast transient response, but often jeopardize the system stability. In order to cancel one of the LC filter poles, place F_{Z1} before the LC filter resonant frequency. In the experience, place F_{Z1} at 10% LC filter resonant frequency. Crossover frequency should be higher than the ESR zero but less than 1/5 of the switching frequency. The F_{P2} should be place at half the switching frequency.

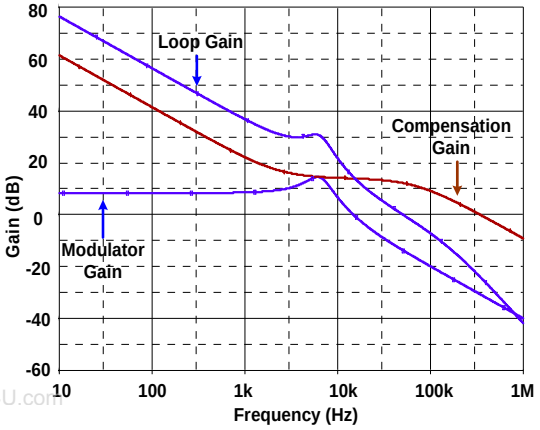


Figure 8. Type 2 Bode Plot

There is another type of compensation called Type 3 compensation that adds a pole-zero pair to the Type 2 network. It's used to compensate output capacitor whose ESR value is much lower (pure MLCC or OSCON Capacitors).

As shown in Figure 9, to insert a network between V_{OUT} and FB in the original Type 2 compensation network can result in Type 3 compensation. Figure 10 shows the difference of their AC response. Type 3 compensation has an additional pole-zero pair that causes a gain boost at the flat gain region. But the gain boosted is limited by the ratio (R1+R4)/R4; if R3 << R4.

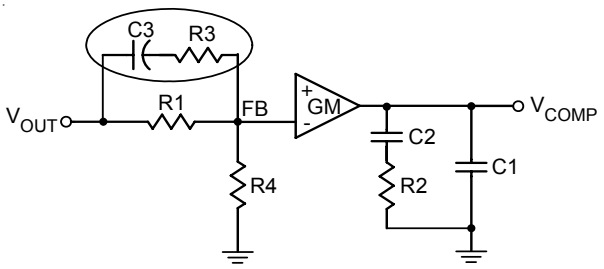


Figure 9. Additional Network of Type 3 Compensation (Add between V_{OUT} and FB)

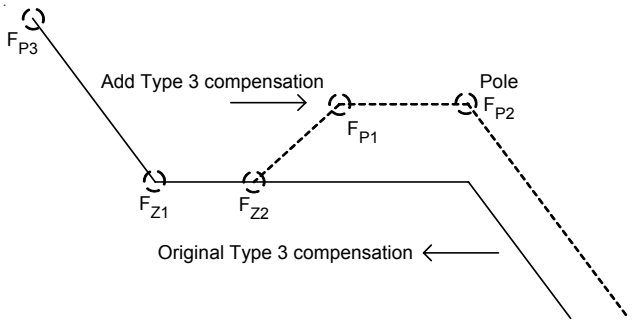


Figure 10. AC Response Curves of Type 2 and 3

Type 3 will induce three poles and two zeros.

Zeros :

$$F_{Z1} = \frac{1}{2\pi \times R2 \times C2}$$

$$F_{Z2} = \frac{1}{2\pi \times (R1+R3) \times C3}$$

Poles :

$$F_{P1} = \frac{1}{2\pi \times R2 \times \left(\frac{C1 \times C2}{C1+C2}\right)}$$

$$F_{P2} = \frac{1}{2\pi \times R3 \times C3}$$

$$F_{P3} = \frac{1}{2\pi \times \left(\frac{R1 \times R3 \times C1}{R1+R3}\right)};$$

which is in the origin.

We recommend F_{Z1} placed in 0.5 x $F_{P(LC)}$; F_{Z2} placed in $F_{P(LC)}$; F_{P1} placed in F_{ESR} and F_{P2} placed in 0.5 x F_{SW}. Figure 11 shows Type 3 Bode Plot.

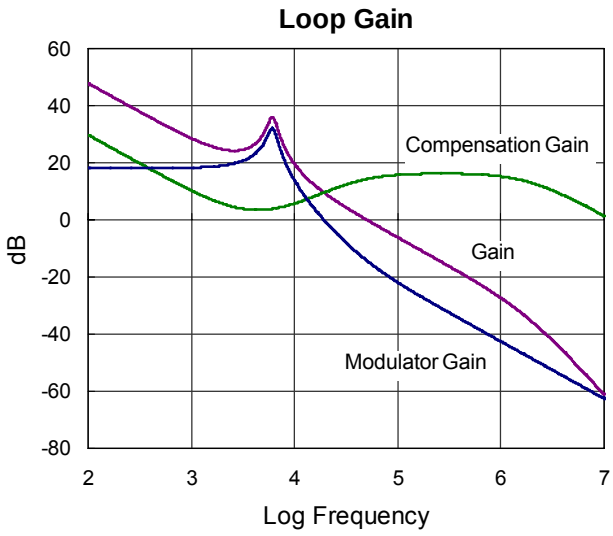


Figure 11. Type 3 Bode Plot

Protection

OCP

The RT8100A use cycle by cycle current comparison. The over current level is set by R_{CSN} resistor. When OC function occurs and SS > (5VSB −1.3), a constant current of 10μA starts to discharge the capacitor connected to SS pin right away. When OC occurs UGATE and LGATE will be off. When the voltage at the capacitor connected to SS pin pass about 0.4V, a constant current of 10μA starts to charge the capacitor.

The PWM signal is enable to pass to the UGATE and LGATE. If the OC protection occurs three times, OCSD will be activated and shut down the chip and pull low PI about 15μs in tracking mode.

RT8100A uses an external resistor R_{CSN} to set a programmable over current trip point. OCP comparator compares inductor current with this reference current. RT8100A uses hiccup mode to eliminate fault detection of OCP or reduce output current when output is shorted to ground.

$$I_X = \frac{DCR \times I_L}{R_{CSN}}$$

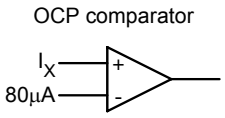


Figure 12

OTP

Monitor the temperature near the driver part within the chip. Shutdown the chip when OTP.

Component Selection

Components should be appropriately selected to ensure stable operation, fast transient response, high efficiency, minimum BOM cost and maximum reliability.

Output Inductor Selection

The selection of output inductor is based on the considerations of efficiency, output power and operating frequency. For a synchronous buck converter, the ripple current of inductor (ΔI_L) can be calculated as follows :

$$\Delta I_L = (V_{IN} - V_{OUT}) \times \frac{V_{OUT}}{V_{IN} \times f_{OSC} \times L}$$

Generally, an inductor that limits the ripple current between 20% and 50% of output current is appropriate. Make sure that the output inductor could handle the maximum output current and would not saturate over the operation temperature range.

Output Capacitor Selection

The output capacitors determine the output ripple voltage (ΔV_{OUT}) and the initial voltage drop after a high slew-rate load transient. The selection of output capacitor depends on the output ripple requirement. The output ripple voltage is described as follows :

$$\Delta V_{OUT} = \Delta I_L \times ESR + \frac{1}{8} \times \frac{V_{OUT}}{f_{OSC}^2 \times L \times C_{OUT}} (1 - D)$$

For electrolytic capacitor application, typically 90~95% of the output voltage ripple is contributed by the ESR of output capacitors. Paralleling lower ESR ceramic capacitor with the bulk capacitors could dramatically reduce the equivalent ESR and consequently the ripple voltage.

Input Capacitor Selection

Use mixed types of input bypass capacitors to control the input voltage ripple and switching voltage spike across the MOSFETs. The buck converter draws pulsewise current from the input capacitor during the on time of upper MOSFET. The RMS value of ripple current flowing through the input capacitor is described as :

$$I_{IN(RMS)} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The input bulk capacitor must be cable of handling this ripple current. Sometime, for higher efficiency the low ESR capacitor is necessarily. Appropriate high frequency ceramic capacitors physically near the MOSFETs effectively reduce the switching voltage spikes.

MOSFET Selection

The selection of MOSFETs is based upon the considerations of $R_{DS(ON)}$, gate driving requirements, and thermal management requirements. The power loss of upper MOSFET consists of conduction loss and switching loss and is expressed as :

$$P_{UPPER} = P_{COND\_UPPER} + P_{SW\_UPPER}$$

$$= I_{OUT} \times R_{DS(ON)} \times D + \frac{1}{2} I_{OUT} \times V_{IN} \times (T_{RISE} + T_{FALL}) \times f_{OSC}$$

where T_{RISE} and T_{FALL} are rising and falling time of V_{DS} of upper MOSFET respectively. $R_{DS(ON)}$ and Q_G should be simultaneously considered to minimize power loss of upper MOSFET.

The power loss of lower MOSFET consists of conduction loss, reverse recovery loss of body diode, and conduction loss of body diode and is express as :

$$P_{LOWER} = P_{COND\_LOWER} + P_{RR} + P_{DIODE}$$

$$= I_{OUT} \times R_{DS(ON)} \times (1 - D) + Q_{RR} \times V_{IN} \times f_{OSC} + \frac{1}{2} \times I_{OUT} \times V_F \times T_{DIODE} \times f_{OSC}$$

where T_{DIODE} is the conducting time of lower body diode.

Special control scheme is adopted to minimize body diode conducting time. As a result, the $R_{DS(ON)}$ loss dominates the power loss of lower MOSFET. Use MOSFET with adequate $R_{DS(ON)}$ to minimize power loss and satisfy thermal requirements.

Bypass Capacitor Notes

Input capacitor C_{IN} is typically chosen based on the ripple current requirements. C_{OUT} is typically selected based on both current ripple rating and ESR requirement.

PWM Layout Considerations

Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability.

First, place the PWM power stage components. Mount all the power components and connections in the top layer with wide copper areas. The MOSFETs of Buck, inductor, and output capacitor should be as close to each other as possible. This can reduce the radiation of EMI due to the high frequency current loop. If the output capacitors are placed in parallel to reduce the ESR of capacitor, equal sharing ripple current should be considered. Place the input capacitor directly to the drain of high-side MOSFET. In multi-layer PCB, use one layer as power ground and have a separate control signal ground as the reference of the all signal. To avoid the signal ground is effect by noise and have best load regulation, it should be connected to the ground terminal of output. Furthermore, follows below guidelines can get better performance of IC :

1. A multi-layer printed circuit board is recommended.
2. Use a middle layer of the PC board as a ground plane and making all critical component ground connections through vias to this layer.
3. Use another solid layer as a power plane and break this plane into smaller islands of common voltage levels.
4. Keep the metal running from the PHASE terminal to the output inductor short.
5. Use copper filled polygons on the top and bottom circuit layers for the phase node.
6. The small signal wiring traces from the LGATE and UGATE pins to the MOSFET gates should be kept short and wide enough to easily handle the several Amperes of drive current.
7. The critical small signal components include any bypass capacitors, feedback components, and compensation components. Position those components close to their pins with a local GND connection, or via directly to the ground plane.
8. R_T resistors should be near the R_T pin respectively, and GND return should be short, and kept away from the noisy MOSFET GND.
9. Place the compensation components close to the FB and COMP pins.
10. The feedback resistors should also be located as close as possible to the relevant FB pin with vias tied straight to the ground plane as required.
11. Minimize the length of the connections between the input capacitors, C_{IN} and the power switches by placing them nearby.
12. Position both the ceramic and bulk input capacitors as close to the upper MOSFET drain as possible, and make the GND returns (From the source of lower MOSFET to V_{IN}, C_{VIN}, GND) short.
13. Position the output inductor and output capacitors between the upper MOSFET and lower MOSFET and the load.
14. Because RT8100A use DCR sense topology, DCR sense point is output inductor from end to end.
15. CSN and FB must be independent path.

Below PCB gerber files are our test board for your reference :

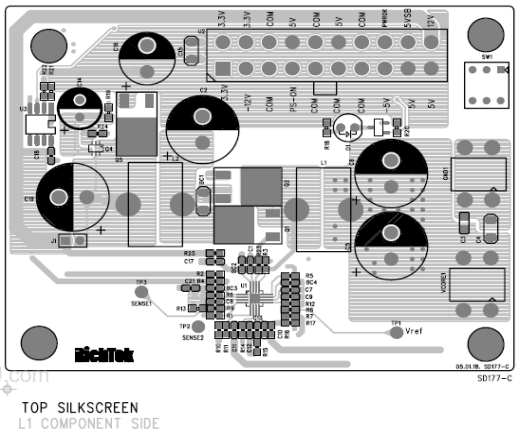


Figure 13. Component Side

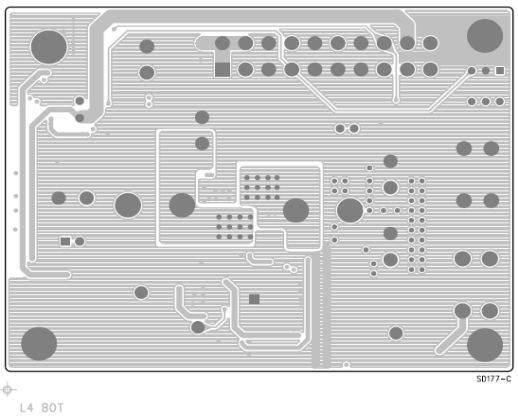
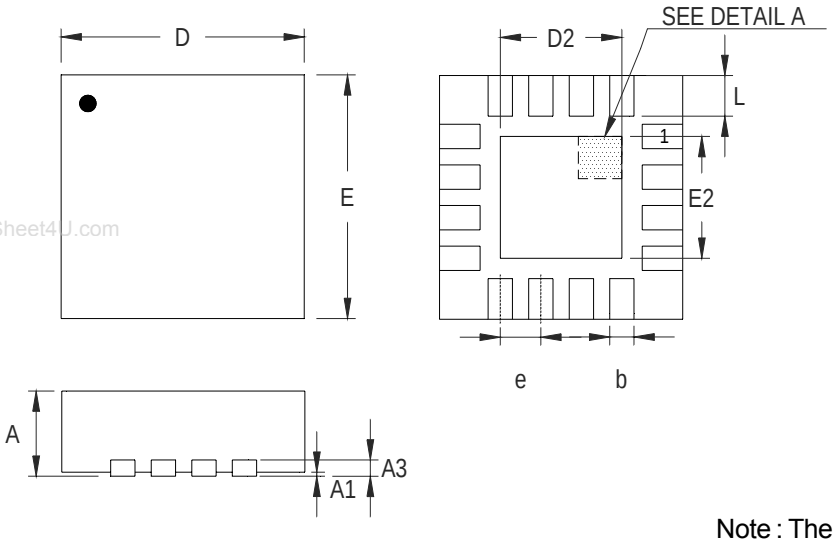
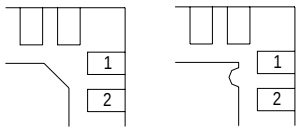


Figure 14. Bottom

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

V-Type 16L QFN 3x3 Package

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