AN-6208

Secondary-Side Synchronous Rectifier (SR) for LLC Resonant Converter Using FAN6208

Introduction

The LLC resonant converter has drawn a lot of attention recently due to its advantages over a conventional series resonant converter and parallel resonant converter: narrow frequency variation over wide load, input variation, and Zero Voltage Switching (ZVS) for the entire load range.

In an LLC resonant converter, rectifier diodes are typically used to obtain DC output voltage from the transformer secondary winding. The conduction loss of diode rectifier contributes significantly to the overall power losses in an LLC resonant converter; especially in low output voltage applications. The conduction loss of a rectifier is proportional to the product of its forward-voltage drop and the forward conduction current. Using synchronous rectification (SR) where the rectifier diode is replaced by MOSFET with a small on resistance (R_{DSON}), the forward-voltage drop of a synchronous rectifier can be lower than that of a diode rectifier and, consequently, the rectifier conduction loss can be reduced.

FAN6208 is a synchronous rectification controller for isolated LLC or LC resonant converters that can drive two individual SR MOSFETs emulating the behavior of rectifier diodes. FAN6208 measures the SR conduction time of each switching cycle by monitoring the drain-to-source voltage of each SR and determines the optimal timing of SR gate drive. FAN6208 also uses the change of opto-coupler diode current to adaptively shrink the duration of SR gate drive signals during load transients to prevent shoot-through. To improve light-load efficiency, Green Mode disables the SR drive signals, minimizing gate drive power consumption at light-load conditions.

This application note describes the design procedure for a SR circuit using FAN6208. The guidelines for printed circuit board (PCB) layout and a design example with experiment results are also presented. Figure 1 shows the typical application circuit of FAN6208.

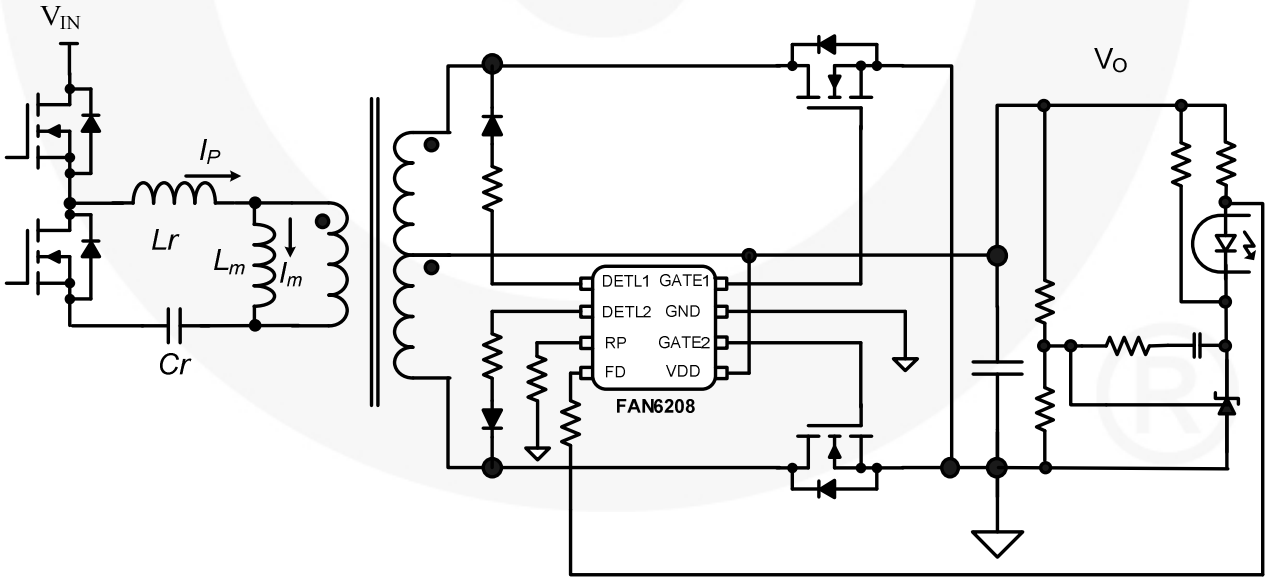

Figure 1. Typical Application

LLC Resonance Converter with SR

Figure 2 shows the simplified schematic of a half-bridge LLC resonant converter, where L_m is the magnetizing inductance that acts as a shunt inductor, L_r is the series resonant inductor, and C_r is the resonant capacitor. Since the magnetizing inductor is relatively small, a considerable amount of magnetizing current (I_m) exists, which freewheels in the primary side without being involved in the power transfer. The primary-side current (I_p) is sum of the magnetizing current and the secondary-side current referred to the primary.

Figure 3 shows the typical gain curve of the half-bridge LLC resonant converter. To allow Zero Voltage Switching (ZVS) for the primary-side switches, gain curves with inductive impedance characteristics should be used, where the gain decreases as frequency increases. The resonant network has a resonant frequency determined by the resonance between L_r and C_r. When the switching frequency is lower than the resonant frequency (below resonance), the half resonance of reflected secondary-side current (diode current) finishes before the primary-side switch is turned off, as shown in Figure 4. When the switching frequency is higher than the resonant frequency (above resonance) the primary-side switch is turned off before the half resonance of reflected secondary-side current (diode current) is completed, as shown in Figure 5.

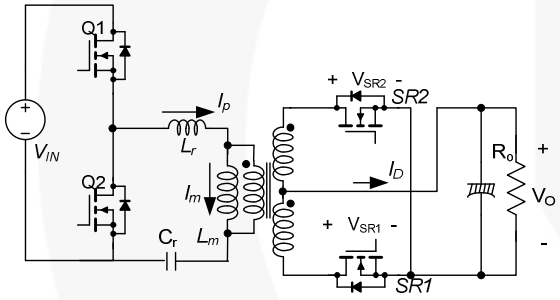

Figure 2. Schematic of LLC Resonant Converter with SR

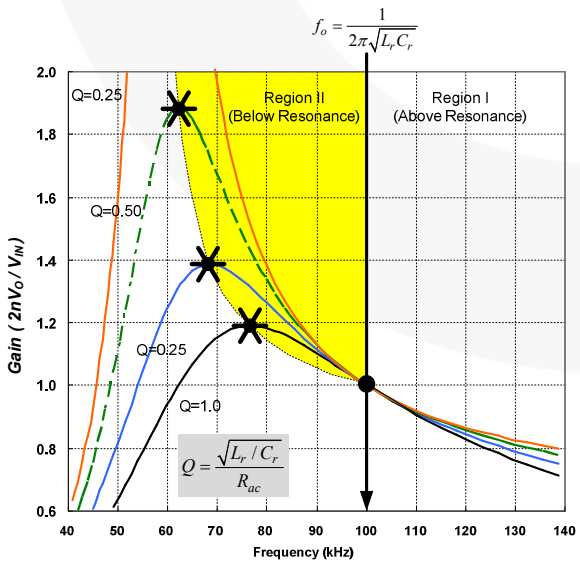

Figure 3. Typical Gain Curves of LLC Resonant Converter

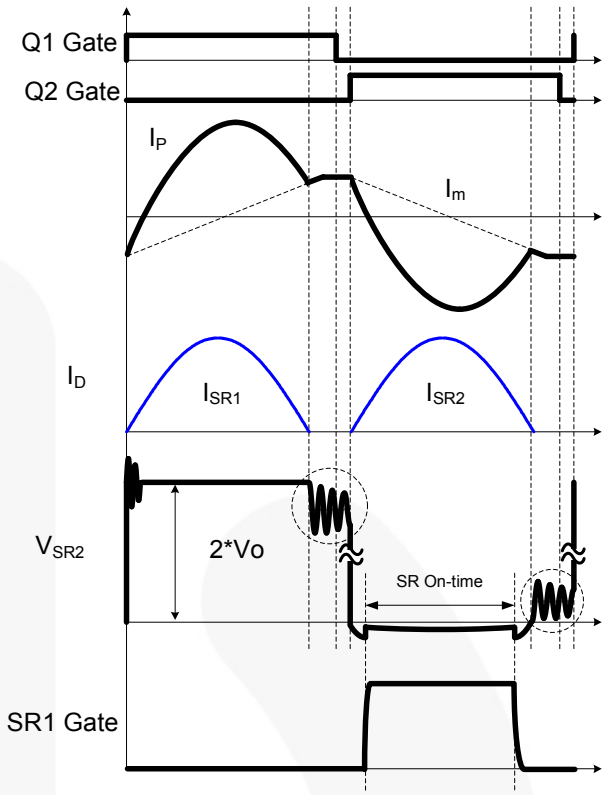

Figure 4. Key Waveforms Below -Resonance Operation

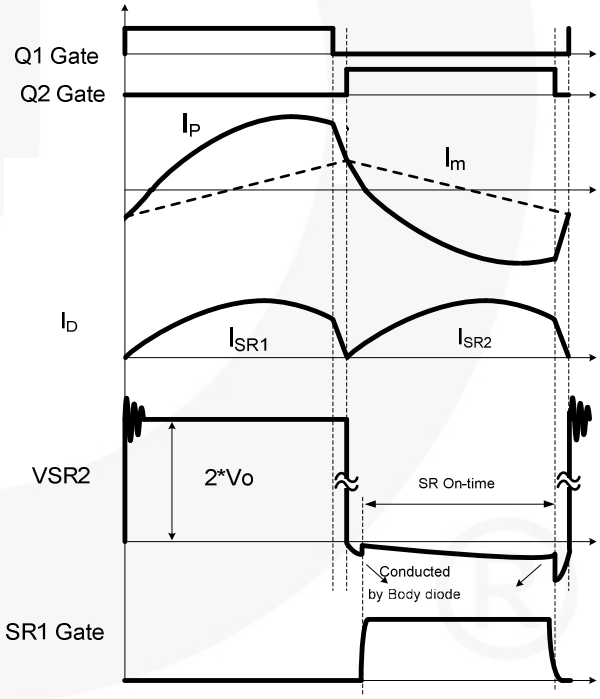

Figure 5. Key Waveforms of Above-Resonance Operation

Application Circuit

Figure 6 shows the typical application circuit of FAN6208 and Figure 7 shows the typical timing diagram of SR gate drive signal. FAN6208 senses the drain-to-source voltage of each SR to determine the gate drive timing. Once the body diode of SR begins conducting, the drain-to-source voltage drops to zero, which causes low detection (DETL) pin voltage to drop to zero. FAN6208 turns on the MOSFET after $t_{ON-ON-DETL}$ (about 350ns), when the voltage on DETL drops below 2V. As depicted in Figure 8, the turn -on delay (after $t_{SR-ON-DETL}$) is a sum of debounce time (150ns) and propagation delay (200ns).

FAN6208 measures the SR conduction duration (t_{DETL}), during which DETL voltage stays lower than 2V, and uses this information to determine the turn-off instant of SR gates of the next switching cycle, as shown in Figure 7. The turn-off instant is obtained by subtracting a dead time (t_{DEAD}) from the measured SR conduction duration of the previous switching cycle.

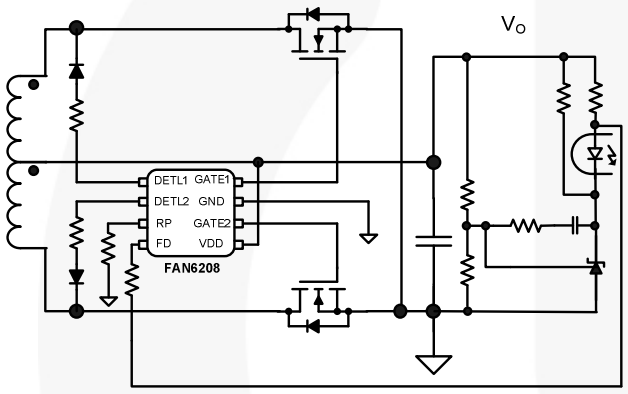

Figure 6. Application Circuit of FAN6208

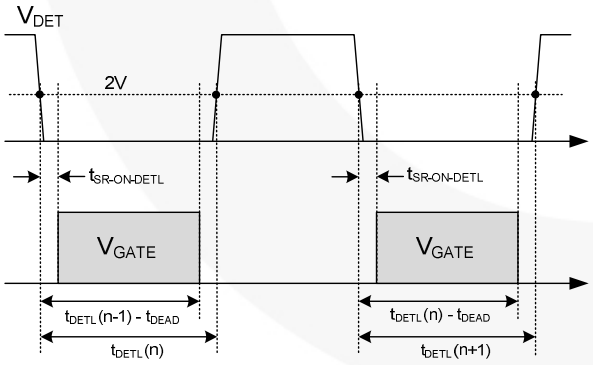

Figure 7. SR Conduction Time Determination

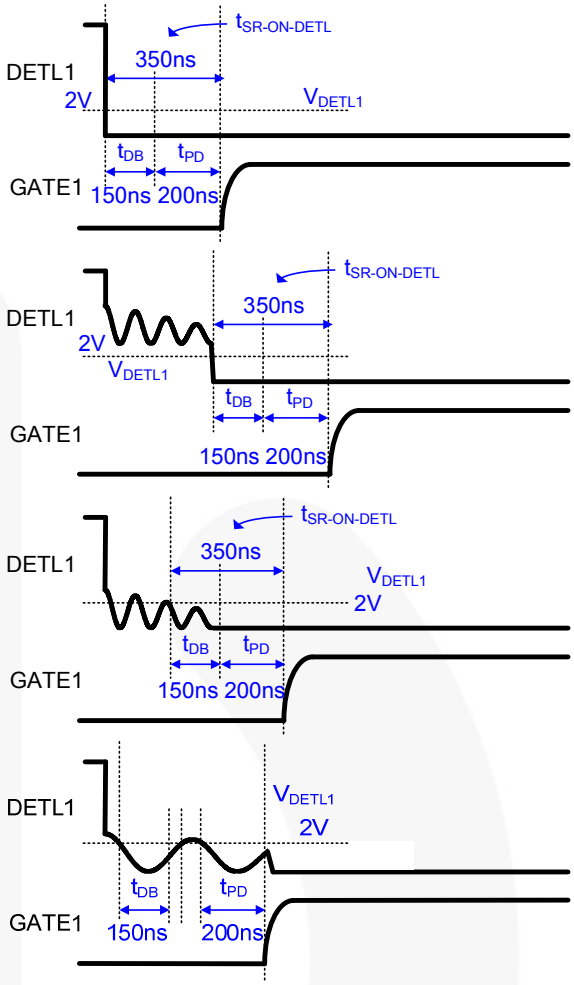

Figure 8. Timing Diagram for Turning On SR

DETL Pin Configuration

Allowable voltage on the DETL pin is from -0.3V to 7V. Since the maximum voltage of the SR drain-to-source voltage is twice that of the output voltage, a diode (D_{DETL}) is required for the DETL pin to prevent high voltage. Diode 1N4148 is typically used for D_{DETL}. Since the DETL internal current source is 50μA, R_{DETL} should be determined such that the DETL voltage is lower than the low detection threshold (2V) with enough margin when the SR conducts. Since the forward-voltage drop of SR can be as low as zero when SR current is small, the DETL resistor should be:

$$R_{DETL} < \frac{(2 - V_{FD})}{50\mu A} \quad (1)$$

where V_{FD} is the forward-voltage drop of DETL diode.

R_{DETL} larger than 20kΩ is not typically recommended for proper low-voltage detection on DETL pin.

R_{DETL} should be determined such that the DETL voltage is higher than -0.3V when the maximum voltage drop occurs across SR, such as:

$$R_{DETL} > \frac{I_{SR}^{max} R_{DS.ON} - V_{FD} - 0.3}{50\mu A} \quad (2)$$

where I_{SR}^{max} is the maximum current of SR and $R_{DS.ON}$ is the maximum on-resistance of the SR MOSFET at high temperature.

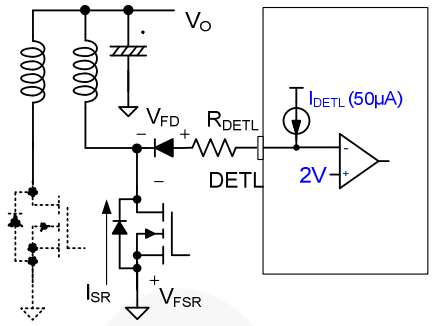

Figure 9. Application Circuit of DETL Pin

RP Pin Configuration

The dead time can be programmed using a resistor on the RP pin. The relationship between the dead time and SR conduction duration (t_{DETL}) for different resistor values on the RP pin are given in Figure 10 and Figure 11. Since the SR conduction time is shrunk by the protection function (gate-shrink function) when t_{DEAD} is smaller than 125ns, R_p should be properly selected such that the gate-shrink function does not operate at maximum switching frequency.

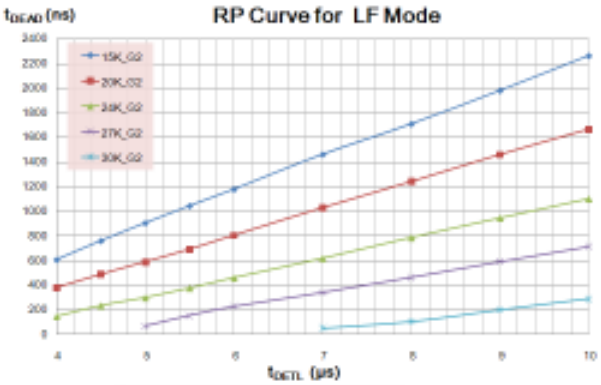

Figure 10. t_{DEAD} vs. t_{DETL} for Different R_P (Low Frequency)

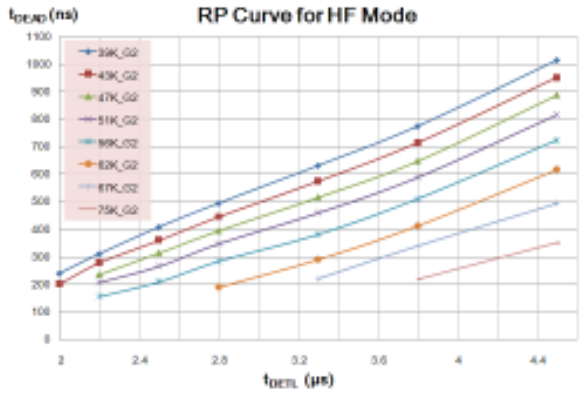

Figure 11. t_{DEAD} vs. t_{DETL} for Different R_P (High Frequency)

The RP pin has an internal constant current source (41.5μA) and the pin voltage is determined by the R_p resistor. Depending on the RP pin voltage, the Green Mode threshold of t_{DETL} is determined as shown in Figure 12. When R_{RP} is less than 36KΩ, FAN6208 operates in Low-Frequency Mode, where Green Mode is enabled when t_{DETL} is smaller than 3.75μs. When R_{RP} is larger than 36KΩ, High-Frequency Mode is selected and Green Mode is enabled for t_{DETL} smaller than 1.90μs.

The RP pin also has two internal thresholds for pin-open / short protection. Using RP pin short protection, remote on / off control can be implemented as shown in Figure 13.

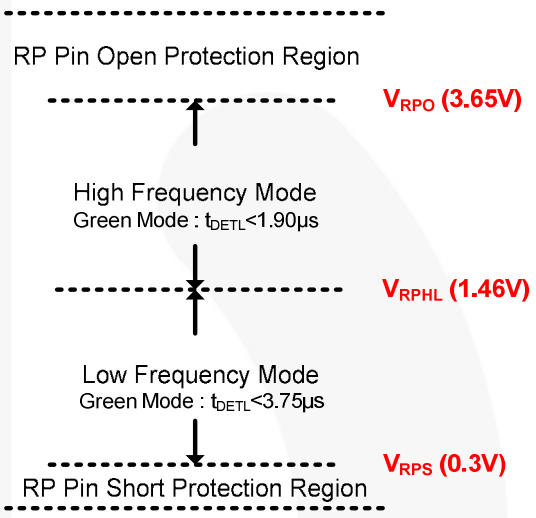

Figure 12. RP Pin Operation

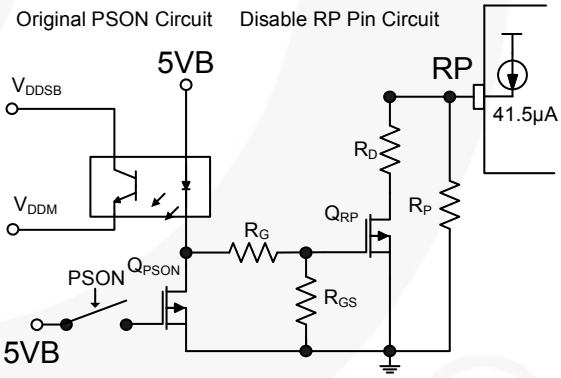

Figure 13. Application Circuit of RP Pin for Remote ON / OFF

Gate-Shrink Functions

In normal operation, the turn-off instant is determined by subtracting a dead time (t_{DEAD}) from the measured SR conduction duration of the previous switching cycle, as shown in Figure 7. This allows proper driving timing for the SR MOSFETS when the converter is in steady state and the switching frequency does not change much. However, this control method may cause shoot-through of SR MOSFETs when the switching frequency increases fast and switching

transition of the primary-side MOSFETs takes place before the turn-off command of the SR is given. To prevent the shoot-through problem, FAN6208 has gate-shrink functions. Gate shrink takes place in the following three conditions:

1. When an insufficient dead time is detected in the previous switching cycle. When the DETL becomes HIGH within 125ns of the detection window after SR gate is turned off, the SR gate drive signal in the next switching cycle is reduced by $t_{SHRINK-DT}$ (about 1.25µs) to increase the dead time as shown in Figure 14.

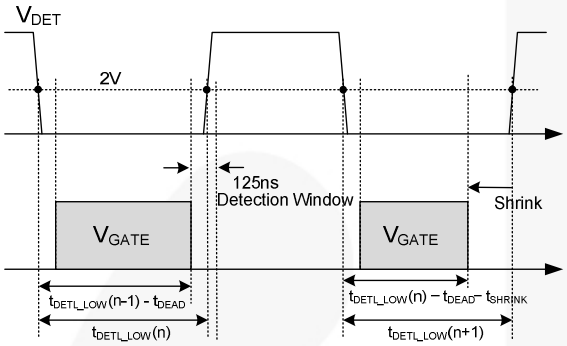

Figure 14. Gate Shrink by Insufficient Dead Time

2. When the feedback information changes fast. FAN6208 monitors the current through the opto-coupler diode by measuring the voltage across the resistor in series with opto-diode, as depicted in Figure 15. If the feedback current through the opto diode increases by more than 20% of the feedback current of the previous switching cycle, SR gate signal is shrunk by $t_{SHRINK-FD}$ (about 1.4µs) for $t_{D-SHRINK-FD}$ (about 90µs), shown in Figure 16.

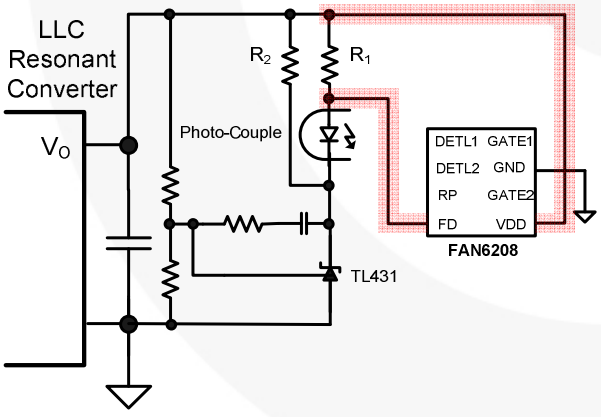

Figure 15. Application Circuit of FD Pin

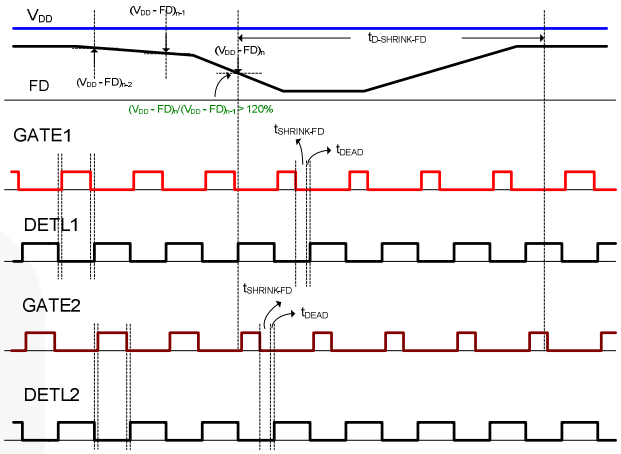

Figure 16. Gate Shrink by Feedback Detection

3. When the DETL voltage has ringing around zero. As depicted in Figure 17, the drain voltage of SR has ringing around zero at light-load condition after the switching transition of primary-side switches. When DETL voltage rises above 2V within 350ns after DETL voltage drops to zero and stays above 2V longer than 150ns, the gate is shrunk by 1.2µs ($t_{SHRINK-RNG}$), as shown in Figure 17.

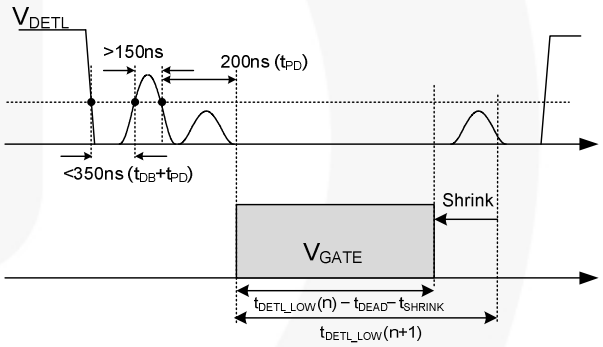

Figure 17. Gate Shrink by the DETL Voltage Ringing

Printed Circuit Board Layout

In Figure 18, the power traces are marked as bold lines. Good PCB layout improves power system efficiency and reliability and minimizes EMI.

Guidelines

- For feedback detection, the FD pin should be connected to the anode of the opto diode. Connecting the FD pin through a resistor can improve surge immunity of the system. Keep trace **1** away from any power trace with high pulsating current.
- The control ground (trace 2) and power ground (trace 7) should meet at a single point to minimize interference. The connecting trace should be as short as possible.
- As indicated by 4, the ground of the feedback loop should be connected to the negative terminal of output capacitor C_O.
- Trace 5 should be long and far from V_o terminal.
- Keep trace **6** as short as possible.
- As indicated by 7, the source terminals of Q_1 and Q_2 are connected to the negative terminal of C_o. Keep trace 10 short, direct, and wide.
- As indicated by 8, the negative terminal of C_o should be connected to the case directly.

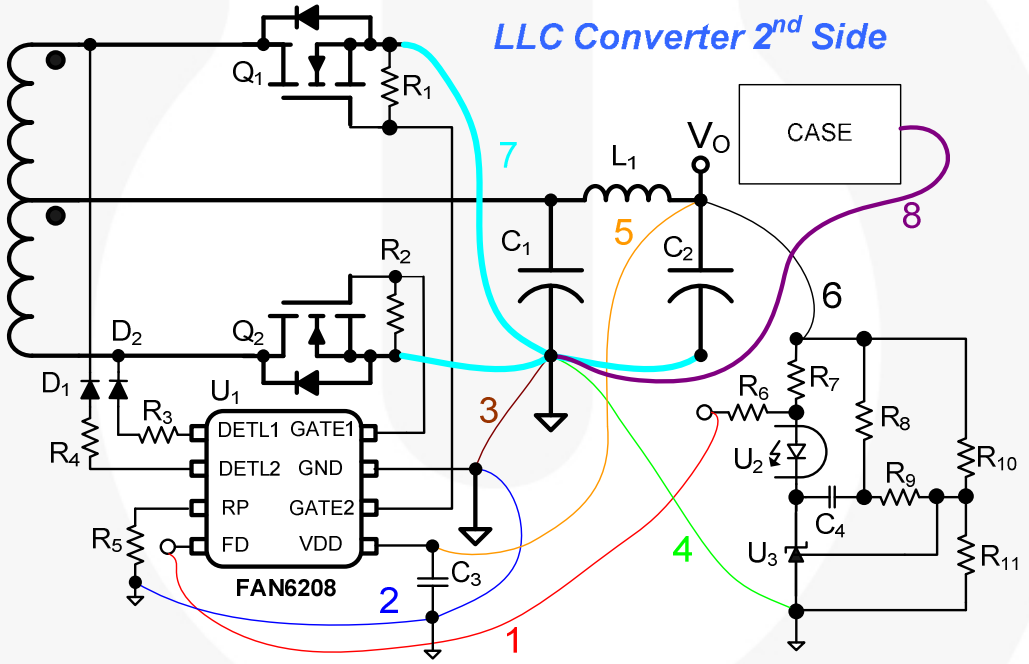

Figure 18. Layout Considerations

Design Example

The following example is a 12V/300W single output power supply with LLC resonant converter topology. As Figure 19 shows, the FAN7621 controller is used for the LLC resonant converter. The integrated CCM PFC controller FAN6982 is used for PFC stage.

The key system parameters are listed in Table 1 and the Bill of Materials (BOM) is summarized in Table 2.

The two-level PFC output voltage function of FAN6982 is used where the typical PFC output voltage is 390V. The PFC output voltage is reduced to 360V for low-line and light-load condition to improve efficiency of the PFC stage. The typical switching frequency (f_s) is 65kHz for PFC stage.

Table 1. System Specification

Input Voltage Range	90~264V_{AC}
PFC Output	360~390V_{DC}
PFC Controller	FAN6982
Main power Controller	FAN7621
Output Voltage (Vo)	12V
Output Power (Po)	300W
PFC Switching Frequency	65kHz
LLC resonant converter Switching Frequency	60~140kHz

The turn ratio n of TX_1 is 13.5, L_m is 1.2mH, L_r is 150μH, and C_r is 47nH. 1N4148 is used for D201 & D202 whose voltage rating is 100V. 27kΩ is used for R204 (R_{RP}) for the Low-Frequency Mode setting.

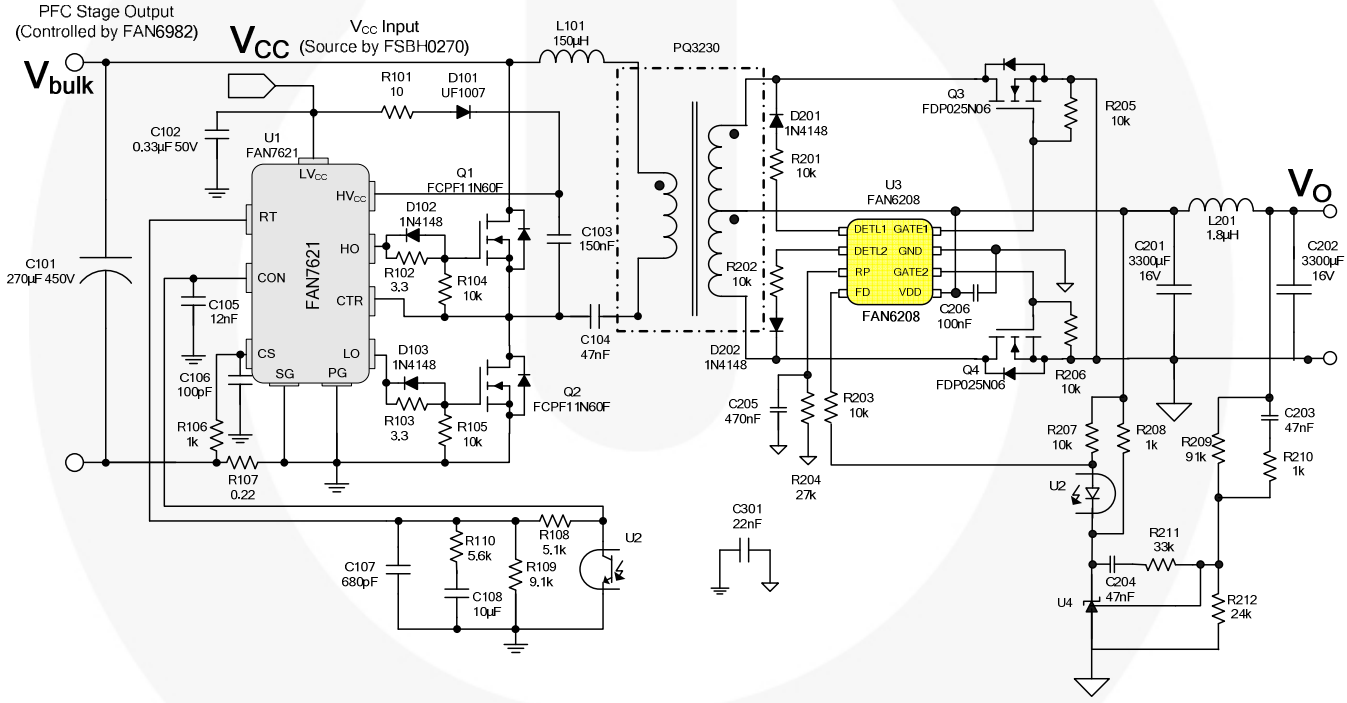

Figure 19. Complete Circuit Diagram

Table 2. Bill of Materials

Part	Value	Note	Part	Value	Note
Resistor			**Capacitor**		
R_{101}	10Ω	1/4W	C_{108}	10μF	25V
R_{102}	3.3Ω	1/4W	C_{201}	3300μF	16V
R_{103}	3.3Ω	1/8W	C_{202}	3300μF	16V
R_{104}	10kΩ	1/8W	C_{203}	47nF	50V
R_{105}	10kΩ	1/8W	C_{204}	47nF	50V
R_{106}	1kΩ	1/8W	C_{205}	470nF	25V
R_{107}	0.2Ω	2W	C_{206}	100nF	50V
R_{108}	5.1kΩ	1/8W	C_{301}	22nF/250V	Y-Capacitor
R_{109}	9.1kΩ	1/8W	**Transformer**		
R_{110}	5.6kΩ	1/8W	TX_1	L_r =10μH/ L_m =1200μH	PQ3230
R_{201}	10kΩ	1/8W	**Diode**		
R_{202}	10kΩ	1/8W	D_{101}	UF1007	1A/1000V
R_{203}	10kΩ	1/8W	D_{102}	1N4148	
R_{204}	27kΩ	1/8W	D_{103}	1N4148	
R_{205}	10kΩ	1/8W	D_{201}	1N4148	
R_{206}	10kΩ	1/8W	D_{202}	1N4148	
R_{207}	10kΩ	1/8W	**Inductor**		
R_{208}	1kΩ	1/8W	L101	L = 150μH	QP2914
R_{209}	91kΩ	1/8W	L201	L = 1.8μH	
R_{210}	1kΩ	1/8W	**MOSFET**		
R_{211}	33kΩ	1/8W	Q_1	FCPF11N60F	
R_{212}	24kΩ	1/8W	Q_2	FCPF11N60F	
Capacitor			Q_3	FDP025N06	
C_{101}	270μF	450V	Q_4	FDP025N06	
C_{102}	0.33μF	50V	**IC**		
C_{103}	150nF	1kV	U_1	FAN7621	LLC Controller
C_{104}	47nF	1kV	U_2	PC817	
C_{105}	12nF	50V	U_3	FAN6208	SR Controller
C_{106}	100pF	50V	U_4	TL431	
C_{107}	680pF	50V			

Figure 20 and Figure 21 show the SR gate drive waveforms for different R_P. As can be seen, the dead time of SR drive can be programmed.

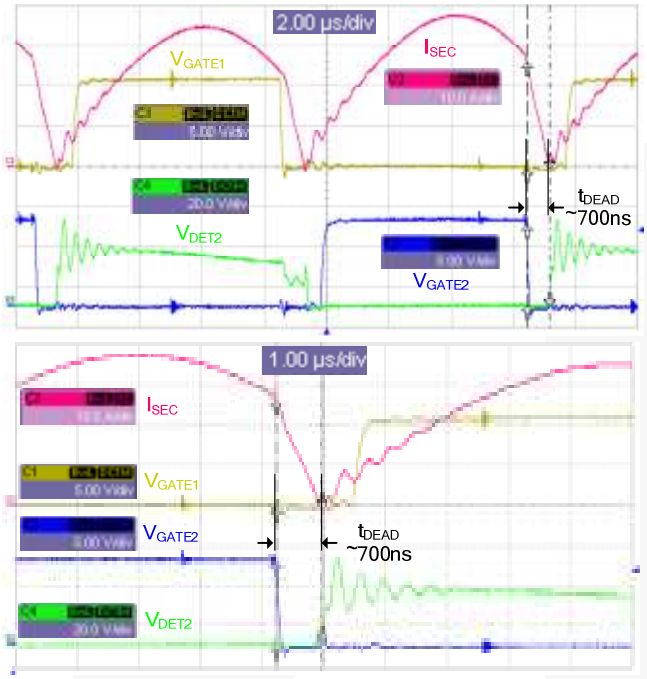

Figure 20. Secondary Side Current and SR Gate Signal by R_{RP}=24kΩ

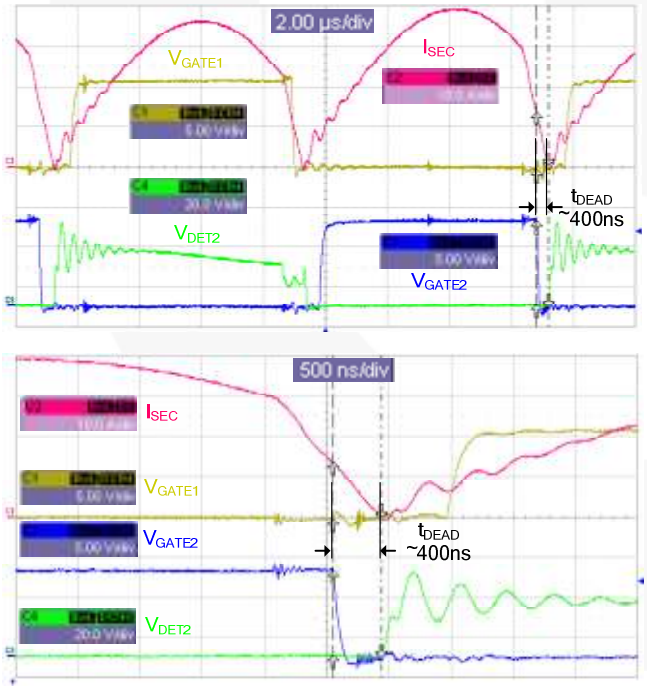

Figure 21. Secondary Side Current and SR Gate Signal by R_{RP}=27kΩ

The efficiency test results of the Schottky diode and synchronous rectification are shown in Table 3 and Table 4. Figure 22 compares the efficiencies of Schottky diode and synchronous rectification. As can be seen, 1~2% efficiency improvement can be obtained using synchronous rectification. Figure 22 also shows how the dead time of SR affects the efficiency. By fine-tuning the dead time, efficiency can be maximized.

Table 3. Efficiency Measurements at V_{AC}=115V on 300W PC Power with Schottky Diodes (MBRP3045)

Load	Input Watts(W)	Output Watts(W)	Efficiency
100%	358.070	307.658	85.920%
50%	176.38	154.91	87.82%
20%	73.30	62.19	84.80%

Table 4. Efficiency Measurements at V_{AC}=115V on 300W PC Power with SRs (FDP025N06 and R_{RP}=30kΩ)

Load	Input Watts (W)	Output Watts (W)	Efficiency	vs. Schottky Diode
100%	347.70	307.62	88.47%	+2.55%
50%	172.81	154.77	89.56%	+1.74%
20%	72.41	62.21	85.91%	+1.11%

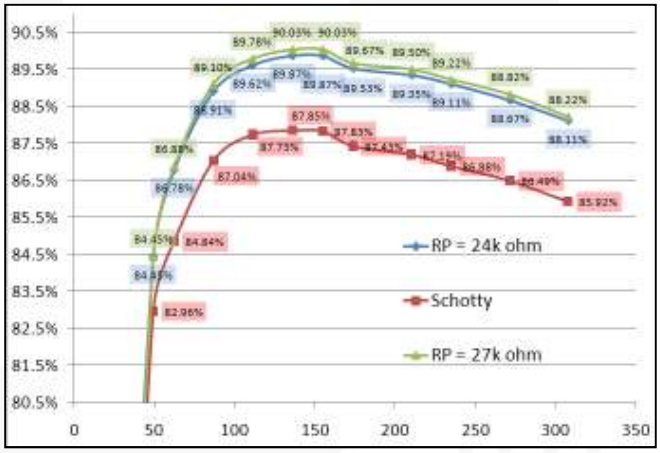

Figure 22. Efficiency Analysis

Related Resources

FAN6208 — Secondary Synchronous Rectifier Controller for LLC Topology
FAN7621 — PFM Controller for Half-Bridge Resonant Converters
FAN6982 — CCM Power Factor Correction Controller
FDP025N06 —FDP025N06 N-Channel PowerTrench® MOSFET 60V,265A, 2.5mΩ
1N/FDLL 914/A/B / 916/A/B / 4148 / 4448 — Small Signal Diode
FSFR2100 — Fairchild Power Switch for Half-Bridge Resonant Converters
AN4137 — Design Guidelines for Off-line Flyback Converters Using Fairchild Power Switch (FPS)
AN-4151 — Half-Bridge LLC Resonant Converter Design Using FSFR-Series Fairchild Power Switch (FPS)