STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCT NAME IC for DC－AC inverter control

TYPE **ＢＤ９２４１Ｆ**

FUNCTION
1. For 36 V high voltage process/ 1 ch Full Bridge control
2. Current, voltage feedback control
3. Built-in soft start circuit
4. Built-in timer-latch circuit
5. Built-in the malfunction preventing circuit (UVLO) when lower voltage
6. Shifting to current consumption save mode from STB terminal
7. External PWM,DC voltage control and current linear control

ABSOLUTE MAXIMUM RATINGS（Ｔａ＝２５℃）

Parameter	Symbol	Rating	Unit
Power Supply Voltage	VCC	36	V
Operating Temperature Range	Topr	-40～+85	℃
Storage Temperature Range	Tstg	-55～+150	℃
allowable loss	Pd	687*	mW
Junction Temperature	Tjmax	+150	℃

*Reduced by 5.5mW/℃ when Ta=25℃ or over (when 70.0mm×70.0mm×1.6mm board is mounting)

OPERATING Range

Parameter	Symbol	Range	Unit
Power Supply Voltage	VCC	9～30	V
Terminal Voltage (SRT,RT,VS,IS,COMP,DUTY)	-	-0.3～5.5	V
Drive output frequency	fOUT	30～90	kHz
BCT oscillation frequency	fBCT	0.10～0.50	kHz

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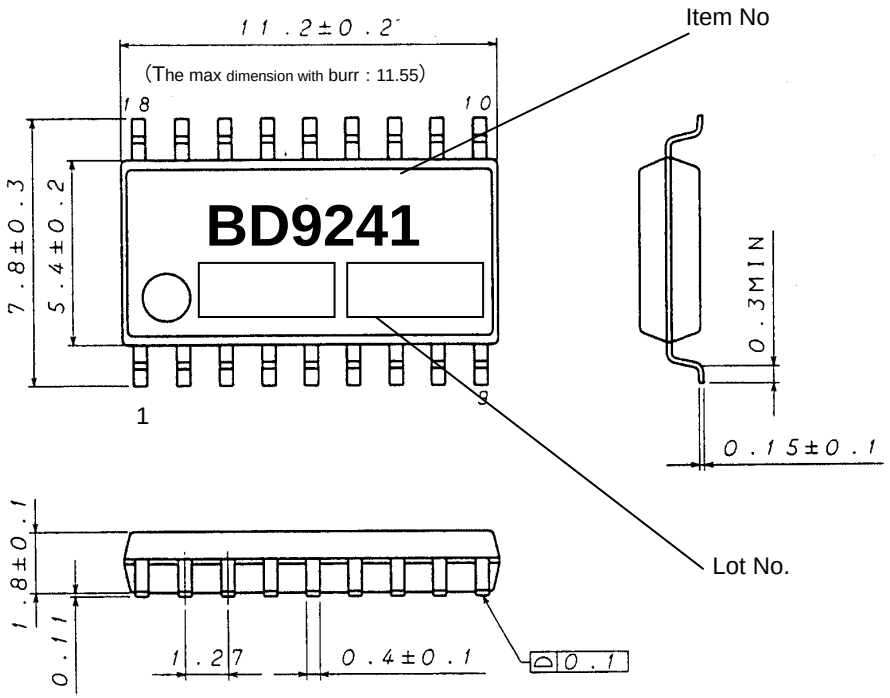
○ELECTRICAL CHARACTERISTICS（Ta=25℃，VCC=15V）

Parameter	Symbol	Rating			Unit	Condition
		MIN	Standard	MAX		
((devices whole))						
Circuit Current at operating	ICC1	—	2.3	5.0	mA	
Circuit Current when standby	ICC2	—	0	10	μA	
((Standby control, SEL control)						
Standby Terminal voltage H	VstH	2.0	—	VCC	V	System ON
Standby Terminal voltage L	VstL	-0.3	—	0.8	V	System OFF
SEL Terminal voltage H	VSELH	2.4	—	VCC	V	DUTY Terminal : 0.5V→2.0V Burst dimming : 100%→0%
SEL Terminal voltage L	VSELL	-0.3	—	0.8	V	DUTY Terminal : 0.5V→2.0V Burst dimming : 0%→100%
((Timer—Latch))						
Voltage setting time	VCP	1.9	2.0	2.1	V	
Current setting time	ICP	0.85	1.0	1.15	μA	
((OSC Block))						
Active edge setting current	Iact	1.25/RT	1.5/RT	1.75/RT	A	
MAX DUTY	MAXDUTY	44	46.4	49	%	RT=100kΩ
Soft start time	TSS	50	100	150	msec	
SRT Terminal ON Resistant	RSRT	—	100	200	Ω	
((UVLOBLOCK))						
Voltage starting operation	VuvloH	6	7	8	V	
Hysteresis width	ΔVuvloH	0.15	0.3	0.6	V	
((Feedback system))						
IS Threshold voltage	VIS	1.225	1.250	1.275	V	
VS Threshold voltage	VVS	1.210	1.250	1.290	V	
IS Source current1	IIS1	—	—	0.9	μA	DUTY=2.0V
IS Source current 2	IIS2	40	50	60	μA	DUTY=0V、IS=0.5V
VS Source current	IVS	—	—	1.0	μA	
ISCOMP Detecting voltage	VISC	0.45	0.50	0.55	V	
((Output block))						
P1，P2 Output voltage H	VOUTPH	VCC-0.3	VCC	—	V	
P1，P2 Output voltage L	VOUTPL	VCC-10.3	VCC-9.3	VCC-8.3	V	
N1，N2 Output voltage H	VOUTNH	8.3	9.3	10.3	V	
N1，N2 Output voltage L	VOUTNL	—	0	0.3	V	
P1，P2 Output sink resistance	RsinkP1,2	—	3	10	Ω	Isink=10mA
P1，P2 Output source resistance	R source P1,2	—	6	12	Ω	Isource=10mA
N1，N2 Output sink resistance	RsinkN1,2	—	4	10	Ω	Isink=10mA
N1，N2 Output source resistance	RsourceN1,2	—	6	12	Ω	Isource=10mA
Drive output frequency	FOUT	48.5	50	51.5	kHz	RT=100kΩ
((Burst mode setting block))						
Triangular wave upper voltage	VburH	1.9	2.0	2.1	V	
Triangular wave lower voltage	VburL	0.4	0.5	0.6	V	
Triangular wave frequency	FBOSC	337	350	363	Hz	BCT=4700pF
((COMP Block))						
Over-voltage detecting voltage	VCOMPH	1.9	2.00	2.1	V	
Hysteresis width	VCOMP	0.1	0.2	0.4	V	

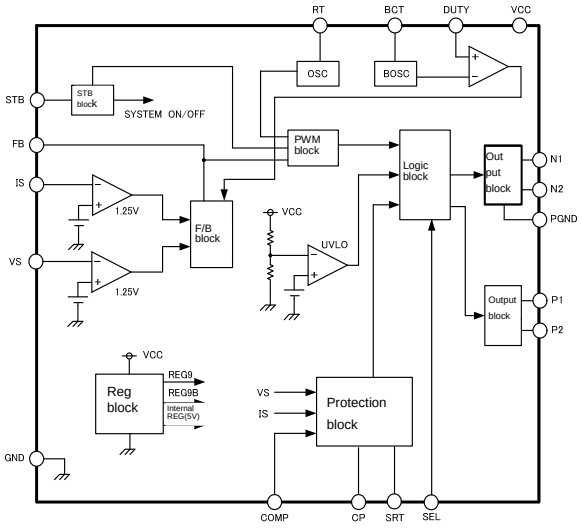
(It is not the radiation-proof design for this product.)

○Dimensional outline drawing



SOP18 (Unit:mm)

○ Block diagram



○Terminal description

Terminal No	Terminal name	Function
1	N2	External FET drive circuit output terminal
2	P2	External FET drive circuit output terminal
3	VCC	Power terminal
4	SEL	Dimming(POS,NEG)select terminal
5	CP	Timer ― latch setting capacity connection terminal
6	GND	GROUND
7	SRT	Connecting terminal for charging and discharging current setting resistance of OSC block
8	RT	Connecting terminal for charging and discharging current setting resistance of OSC block
9	VS	Error amplifier input terminal②
10	IS	Error amplifier input terminal①
11	FB	Error amplifier output terminal
12	COMP	Over-voltage detecting terminal
13	BCT	Connecting terminal for charging and discharging current setting capacity of BOSC block.
14	DUTY	Switching terminal of PWM mode and burst mode
15	STB	Standby switch terminal
16	PGND	External FET drive circuit GND terminal
17	P1	External FET drive circuit output terminal
18	N1	External FET drive circuit output terminal

○Usage notes

1. About the absolute maximum ratings
   The damage may occur If absolute maximum rating such as applied voltage and operating temperature range etc. is exceeded, moreover such destructive conditions as short mode or open mode etc. can not be assumed, so If a particular mode such as exceeding the absolute maximum rating is assumed, please consider taking physical safety measures such as fuse etc.
2. As long as being operation range, the operation of circuit function will be assured in the range of operating ambient temperature. About characteristic value, the specification value of electric characteristic can't be guaranteed, but the characteristic value doesn't change rapidly in these ranges.
3. When attaching to the printed substrate, pay special attention to the direction and proper placement of the IC. If the IC is attached incorrectly, it may be destroyed. Destruction can also occur when there is a short, which can be caused by foreign objects entering between outputs or an output and the power GND.
4. Please be careful that there is a possibility of malfunction which is happening when you use it in a strong electromagnetic field.
5. The potential of GND terminal and PGND terminal is used with not over ±0.3V please.
6. This IC has a built-in Temperature Protection Circuit (TSD circuit). The temperature protection circuit (TSD circuit) is only to cut off the IC from thermal runaway, and has not been designed to protect or compensate the IC. Therefore, the user should not plan to activate this circuit with continued operation in mind.
7. Although the quality of this product has been tightly controlled , the damage may occur If absolute maximum rating such as applied voltage and operating temperature range etc. is exceeded, moreover such destructive conditions as short mode or open mode etc. can not be assumed, so If a particular mode such as exceeding the absolute maximum rating is assumed, please consider taking a measures such as fuse etc.
8. Regarding the external FET, since gate voltage will be changed regarding parasitic capacity between drain gates while switching the drain voltage, please think over dispersion etc of our company's IC, please select FET with sufficient margin.
9. CP timer does not operate during the time of soft start.
10. To prevent the destruction from external static electricity, please give resistance to the pin which directly link with connector etc.
11. This IC is a monolithic IC, and between each element there is a P+ isolation and P substrate for element separation. There is a P-N junction and other parasitic elements formed between this P-layer and each element's N-layer, as shown in Fig. when the resistors and transistors are connected to the terminal ,
    - ○ When GND>(terminal A) at the resistance, or GND>(terminal B) at the transistor (NPN), the P-N junction operates as a parasitic diode.
    - ○ Also, when GND>(terminal B) at the transistor, a parasitic NPN transistor operates by the N-layer of other elements which close to the aforementioned parasitic diode.

    With the IC's configuration, the production of parasitic elements by the relationships of the electrical potentials is inevitable. The operation of the parasitic elements can also interfere with the circuit operation, leading to malfunction and even destruction. Therefore, uses which cause the parasitic elements to operate, such as applying voltage to the input terminal which is lower than the GND (P-substrate), should be avoided.

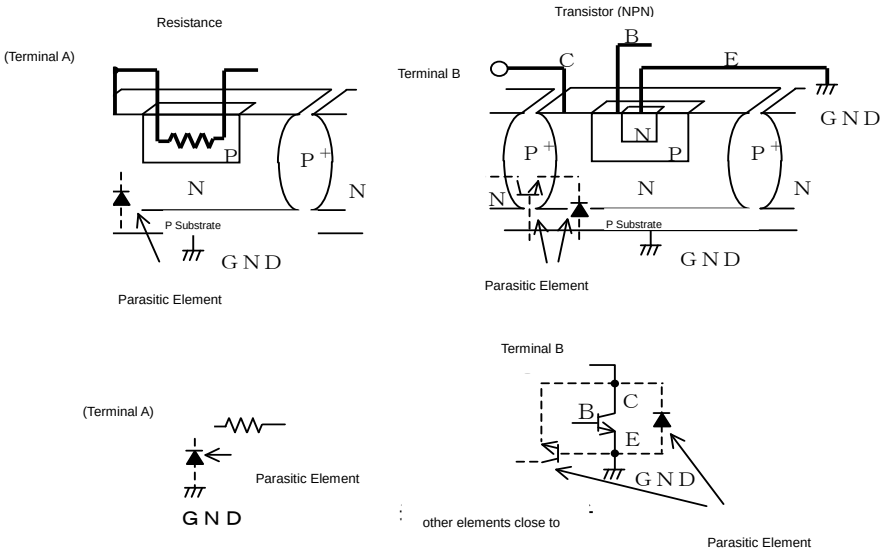


Fig.1 Simple Structure of Monolithic IC

Notes

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