



## UR6512

## LINEAR INTEGRATED CIRCUIT

### 2A DDR BUS TERMINATION REGULATOR

#### DESCRIPTION

The **UR6512** is a linear regulator providing up to 2A transient peak current and has sourcing and sinking capability for DDR SDRAM bus terminator applications while regulating an output voltage to within 20mV. It contains a high speed operational amplifier which provides fast load transient response and only requires 10uF of ceramic output capacitance.

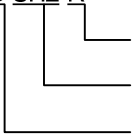
The **UR6512** output termination voltage tracks the reference voltage applied at  $V_{REF}$  pin. A resistor divider connected to  $V_{IN}$ , GND and  $V_{REF}$  pins is used to force the reference voltage to  $V_{REF}$  pin. Additional features include current limiting protection and thermal shutdown protection.

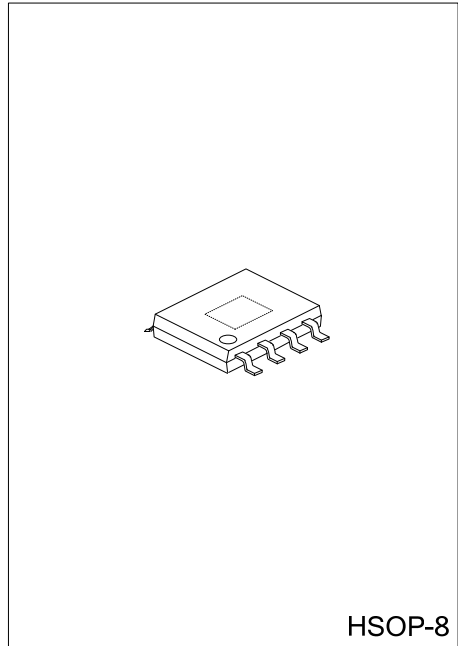
#### FEATURES

- \* DDR1/ DDR2 Termination Voltage Applications
- \* Low Output Voltage Offset within 20mV@±1.8A
- \* Source and Sink 2A Peak Current
- \* Adjustable Output Voltage by External Resistors
- \* Integrated Power MOS Devices
- \* Suspend to RAM(STR) Functionality
- \* Current Limiting Protection
- \* Thermal Shutdown Protection
- \* Cost-Effective and Easy to Use

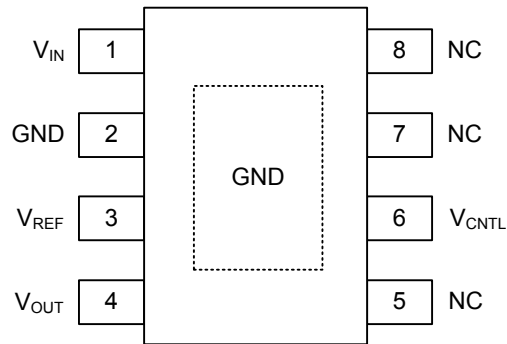
#### ORDERING INFORMATION

| Ordering Number | Package | Packing   |
|-----------------|---------|-----------|
| UR6512G-SH2-R   | HSOP-8  | Tape Reel |

|   |                  |                     |  |
|---|------------------|---------------------|--|
|  | UR6512G-SH2-R    |                     |  |
|   | (1) Packing Type | (1) R: Tape Reel    |  |
|   | (2) Package Type | (2) SH2: HSOP-8     |  |
|   | (3) Halogen Free | (3) G: Halogen Free |  |



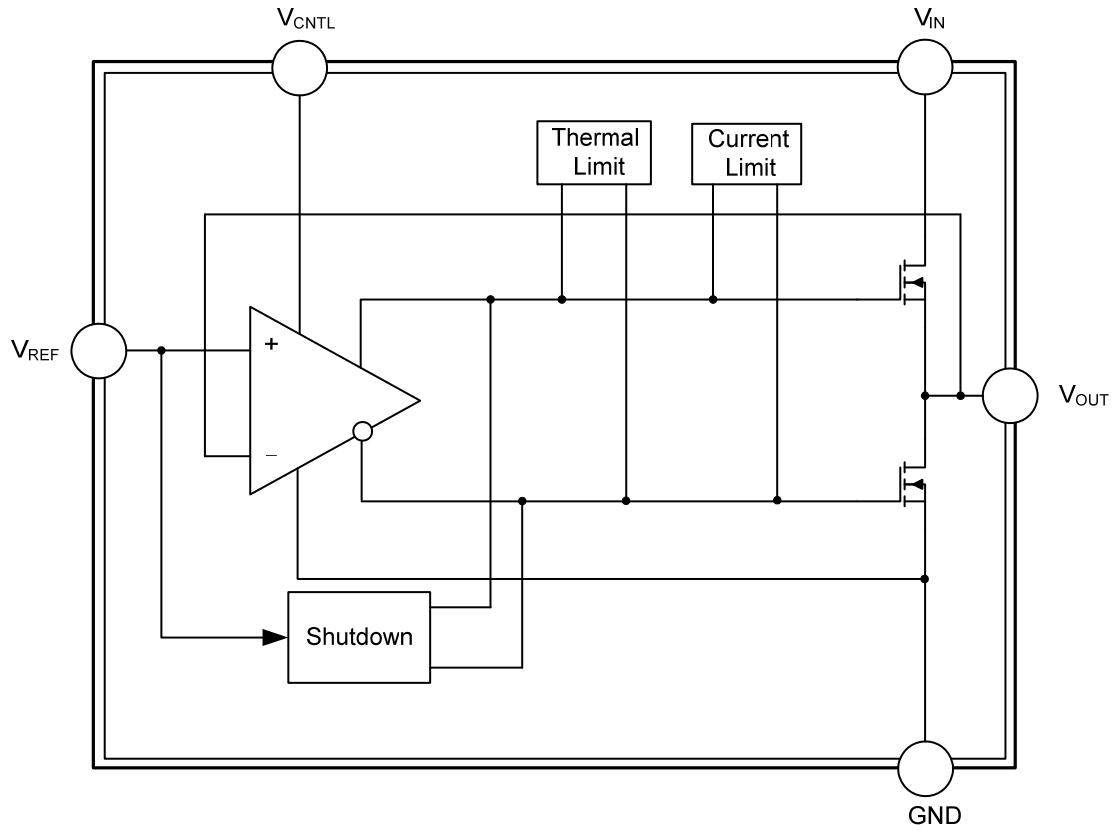
### ■ PIN CONFIGURATIONS



### ■ PIN DESCRIPTION

| PIN NO | PIN NAME          | PIN TYPE | PIN DESCRIPTION   |
|--------|-------------------|----------|---|
| 1      | V <sub>IN</sub>   | I        | Power supply pin for the V <sub>OUT</sub> output            |
| 2      | GND               | O        | Ground pin  |
| 3      | V <sub>REF</sub>  | I        | Reference voltage input and active-low shutdown control pin |
| 4      | V <sub>OUT</sub>  | O        | Output voltage pin  |
| 6      | V <sub>CNTL</sub> | I        | Power supply pin for the internal control circuits          |
| 5,7,8  | NC                | --       | No connect  |

## ■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

| PARAMETER                         | SYMBOL            | RATINGS    | UNIT |
|-----------------------------------|-------------------|------------|------|
| V <sub>CNTL</sub> Control Voltage | V <sub>CNTL</sub> | 6          | V    |
| V <sub>IN</sub> Supply Voltage    | V <sub>IN</sub>   | 6          | V    |
| Power Dissipation (Ta=25°C)       | P <sub>D</sub>    | 1.176      | W    |
| Junction Temperature              | T <sub>J</sub>    | 125        | °C   |
| Storage Temperature               | T <sub>STG</sub>  | -65 ~ +150 | °C   |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.  
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

| PARAMETER                  | SYMBOL        | RATINGS | UNIT |
|----------------------------|---------------|---------|------|
| Junction to Ambient (Note) | $\theta_{JA}$ | 86      | °C/W |
| Junction to Case           | $\theta_{JC}$ | 15      | °C/W |

■ RECOMMENDED OPERATING CONDITIONS (Note 1)

| PARAMETER                         | SYMBOL            | RATINGS          | UNIT |
|-----------------------------------|-------------------|------------------|------|
| V <sub>CNTL</sub> Control Voltage | V <sub>CNTL</sub> | (3.3 or 5) ±5%   | V    |
| V <sub>IN</sub> Supply Voltage    | V <sub>IN</sub>   | (1.8 ~ 2.5) ±3%  | V    |
| V <sub>REF</sub> Input Voltage    | V <sub>REF</sub>  | (0.9 ~ 1.25) ±3% | V    |
| Junction Temperature              | T <sub>J</sub>    | -40~+125         | °C   |

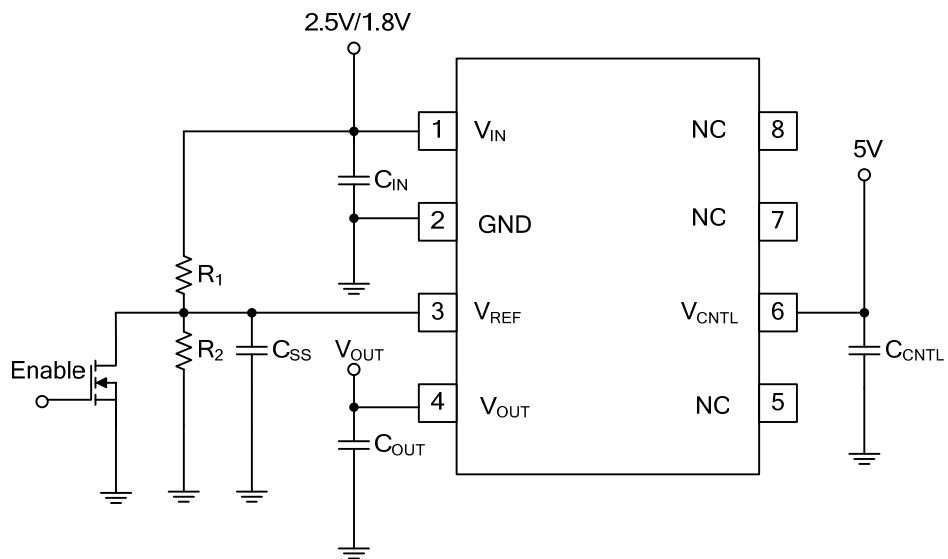
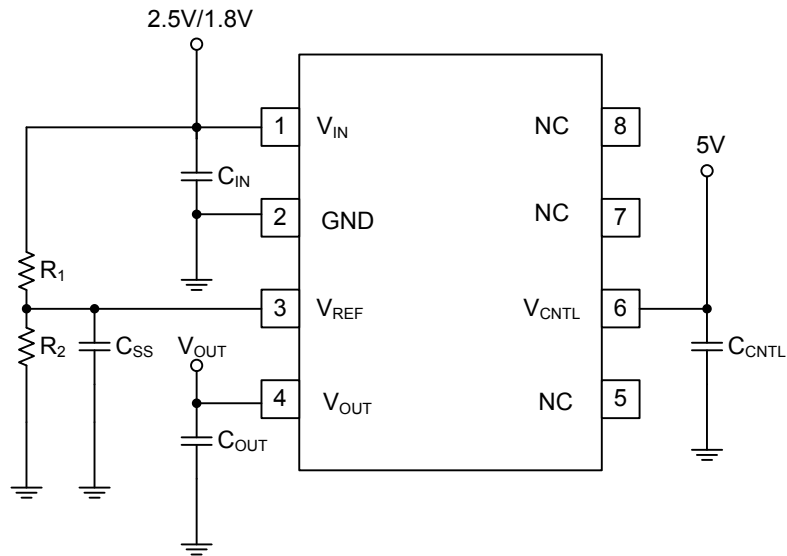
Notes: 1. All voltage values are with respect to the network ground terminal unless otherwise noted.  
2. The V<sub>OUT</sub> tracks the V<sub>REF</sub> with additional voltage offset and load regulation.

■ ELECTRICAL CHARACTERISTICS (Ta=25°C, unless otherwise specified)

(V<sub>IN</sub>=1.8V, V<sub>CNTL</sub>=5V, V<sub>REF</sub>=0.9V, C<sub>OUT</sub> = 10μF (Ceramic))

| PARAMETER   | SYMBOL             | TEST CONDITIONS                                 | MIN | TYP | MAX  | UNIT |
|---|--------------------|---|-----|-----|------|------|
| <b>INPUT CURRENT</b>  |                    |   |     |     |      |      |
| Operation Current of V <sub>CNTL</sub>                      | I <sub>CNTL</sub>  | I <sub>OUT</sub> =0A                            |     | 1   | 2.5  | mA   |
| Standby Current   | I <sub>STB</sub>   | V <sub>REF</sub> <0.2V, R <sub>LOAD</sub> =180Ω |     | 2   | 90   | μA   |
| <b>OUTPUT VOLTAGE (DDR/DDR II/DDR III)</b>                  |                    |   |     |     |      |      |
| Output Voltage Offset (V <sub>REF</sub> -V <sub>OUT</sub> ) | V <sub>OS</sub>    | I <sub>OUT</sub> =0A                            | -20 |     | 20   | mV   |
| Load Regulation   | ΔV <sub>LOAD</sub> | I <sub>OUT</sub> =±1.8A                         | -20 |     | 20   | mV   |
| <b>PROTECTION</b>   |                    |   |     |     |      |      |
| Current Limit   | I <sub>LIMIT</sub> | V <sub>IN</sub> =2.5V/1.8V                      | 2   |     |      | A    |
| Thermal Shutdown Temperature                                | T <sub>SD</sub>    | V <sub>CNTL</sub> =5V                           | 125 | 170 |      | °C   |
| Thermal Shutdown Hysteresis                                 | ΔT <sub>SD</sub>   | V <sub>CNTL</sub> =5V                           |     | 35  |      | °C   |
| <b>V<sub>REF</sub> Shutdown</b>                             |                    |   |     |     |      |      |
| Shutdown Threshold  | V <sub>IH</sub>    | Enable  | 0.6 |     |      | V    |
|   | V <sub>IL</sub>    | Shutdown  |     |     | 0.15 | V    |

## ■ TYPICAL APPLICATIONS CIRCUIT



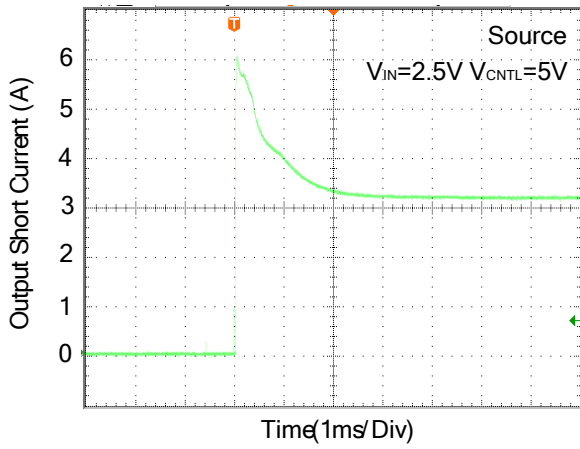
$R_1=R_2=100\text{K}\Omega$ ,  $C_{OUT}=10\mu\text{F}(\text{Ceramic})+1000\mu\text{F}$  under the worst case testing condition

$C_{SS}=1\mu\text{F}$ ,  $C_{IN}=470\mu\text{F}(\text{Low ESR})$ ,  $C_{CNTL}=47\mu\text{F}$

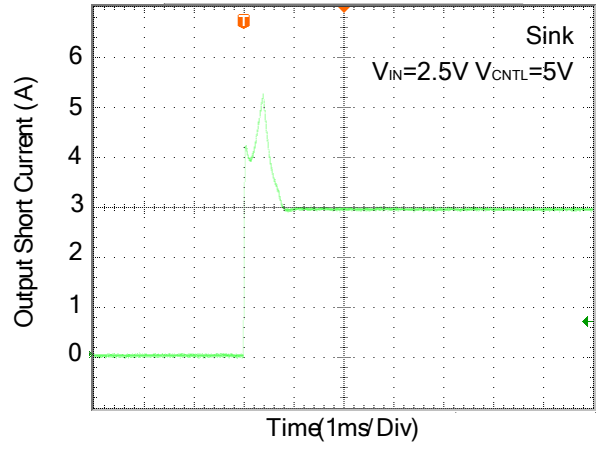
$$V_{REF} = \frac{R_2}{R_1 + R_2} V_{IN}(V), V_{OUT} \text{ track } V_{REF}$$

■ TYPICAL CHARACTERISTICS

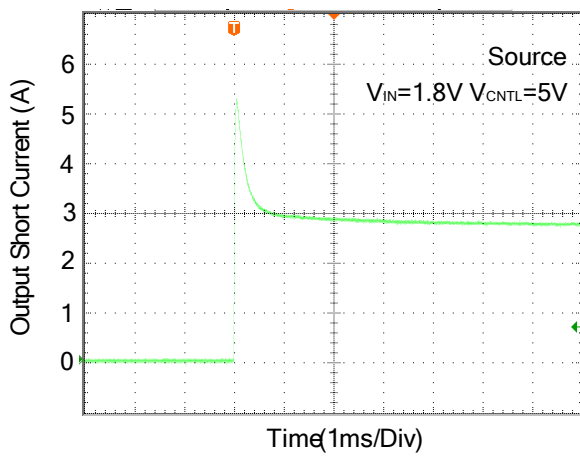
Output Short Circuit Protection



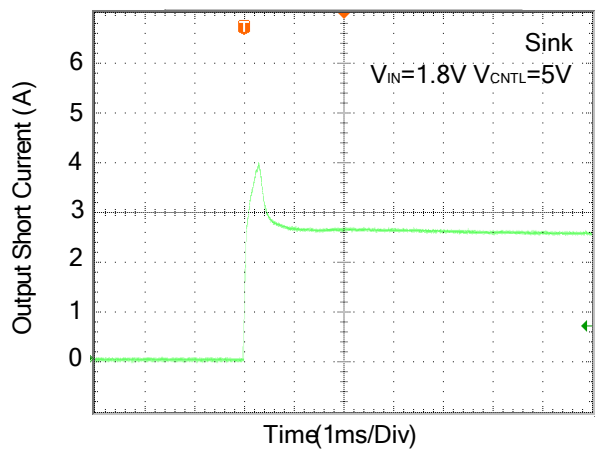
Output Short Circuit Protection



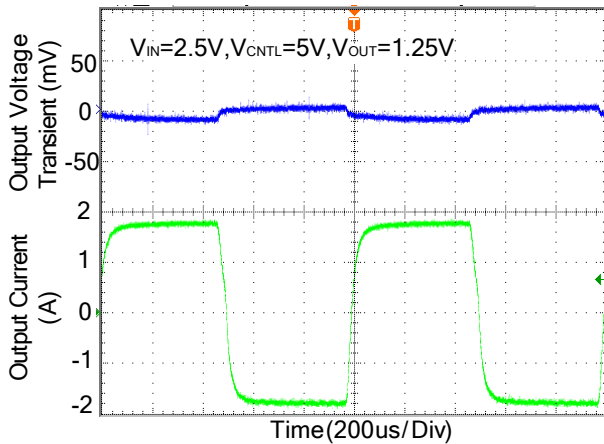
Output Short Circuit Protection



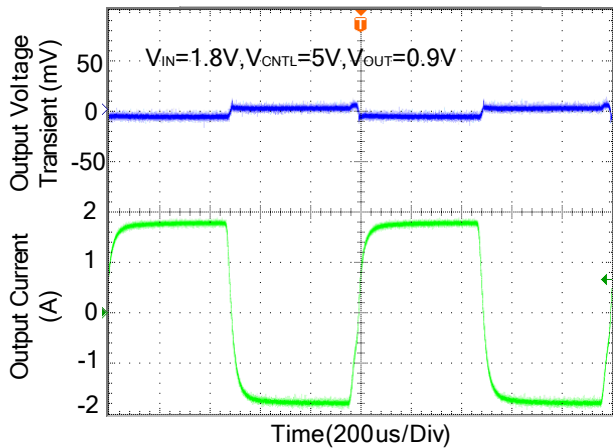
Output Short Circuit Protection



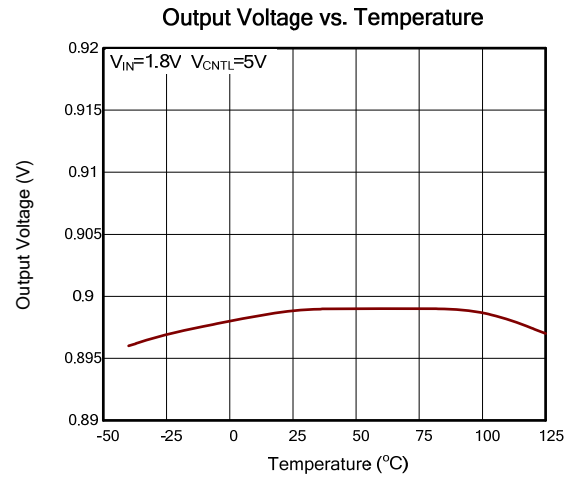
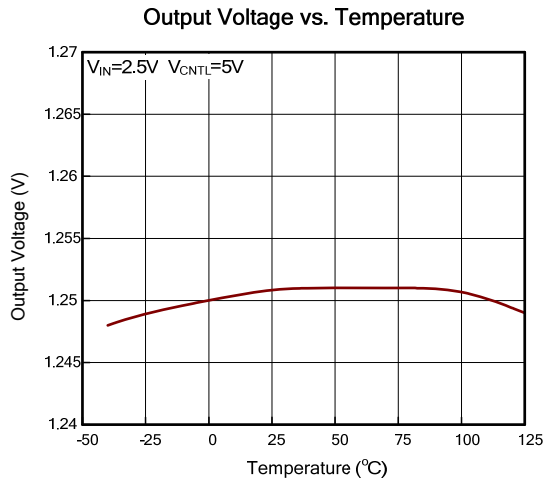
1.25V<sub>TT</sub>@1.8A Transient Response



0.9V<sub>TT</sub>@1.8A Transient Response



■ TYPICAL CHARACTERISTICS(Cont.)



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