

MMDJ3N03BJT

Plastic Power Transistors SO-8 for Surface Mount Applications

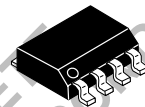
- Collector -Emitter Sustaining Voltage — $V_{CE(sus)}$
= 30 Vdc (Min) @ $I_C = 10$ mAdc
- High DC Current Gain —
 $h_{FE} = 85$ (Min) @ $I_C = 0.8$ Adc
= 60 (Min) @ $I_C = 3.0$ Adc
- Low Collector -Emitter Saturation Voltage —
 $V_{CE(sat)} = 0.18$ Vdc (Max) @ $I_C = 1.2$ Adc
= 0.45 Vdc (Max) @ $I_C = 3.0$ Adc
- Miniature SO-8 Surface Mount Package – Saves Board Space



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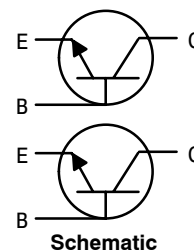
**DUAL BIPOLAR
POWER TRANSISTOR
NPN SILICON
30 VOLTS, 3 AMPERES**



(SO-8)
CASE 751-07
Style 16

Emitter-1	1	8	Collector-1
Base-1	2	7	Collector-1
Emitter-2	3	6	Collector-2
Base-2	4	5	Collector-2

Top View
Pinout



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MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Base Voltage	V _{CB}	45	Vdc
Collector–Emitter Voltage	V _{CEO}	30	Vdc
Emitter–Base Voltage	V _{EB}	±6.0	Vdc
Collector Current — Continuous — Peak	I _C	3.0 5.0	Adc
Base Current — Continuous	I _B	1.0	Adc
Operating and Storage Junction Temperature Range	T _J , T _{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance – Junction to Ambient on 1" sq. (645 sq. mm) Collector pad on FR-4 board material with one die operating.	R _{θJA}	100	°C/W
Thermal Resistance – Junction to Ambient on 0.012" sq. (7.6 sq. mm) Collector pad on FR-4 board material with one die operating.		185	
Total Power Dissipation @ T _A = 25°C mounted on 1" sq. (645 sq. mm) Collector pad on FR-4 board material with one die operating. Derate above 25°C	P _D	1.25 10	W mW/°C
Maximum Temperature for Soldering	T _L	260	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I _C = 10 mAdc, I _B = 0 Adc)	V _{CEO(sus)}	30	—	—	Vdc
Emitter–Base Voltage (I _E = 50 μAdc, I _C = 0 Adc)	V _{EBO}	6.0	—	—	Vdc
Collector Cutoff Current (V _{CE} = 25 Vdc, R _{BE} = 200 Ω) (V _{CE} = 25 Vdc, R _{BE} = 200 Ω, T _J = 125°C)	I _{CER}	— —	— —	20 200	μAdc
Emitter Cutoff Current (V _{BE} = 5.0 Vdc)	I _{EBO}	—	—	10	μAdc

ON CHARACTERISTICS⁽¹⁾

Collector–Emitter Saturation Voltage (I _C = 0.8 Adc, I _B = 20 mAdc) (I _C = 1.2 Adc, I _B = 20 mAdc) (I _C = 3.0 Adc, I _B = 0.3 Adc)	V _{CE(sat)}	— — —	0.105 — —	0.15 0.18 0.45	Vdc
Base–Emitter Saturation Voltage (I _C = 3.0 Adc, I _B = 0.3 Adc)	V _{BE(sat)}	—	—	1.25	Vdc
Base–Emitter On Voltage (I _C = 1.2 Adc, V _{CE} = 4.0 Vdc)	V _{BE(on)}	—	—	1.10	Vdc
DC Current Gain (I _C = 0.8 Adc, V _{CE} = 1.0 Vdc) (I _C = 1.2 Adc, V _{CE} = 1.0 Vdc) (I _C = 3.0 Adc, V _{CE} = 1.0 Vdc)	h _{FE}	85 80 60	195 — —	— — —	—

DYNAMIC CHARACTERISTICS

Output Capacitance (V _{CB} = 10 Vdc, I _E = 0 Adc, f = 1.0 MHz)	C _{ob}	—	85	135	pF
Input Capacitance (V _{EB} = 8.0 Vdc)	C _{ib}	—	200	—	pF
Current–Gain — Bandwidth Product ⁽²⁾ (I _C = 500 mAdc, V _{CE} = 10 Vdc, F _{test} = 1.0 MHz)	f _T	—	72	—	MHz

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) f_T = |h_{FE}| • f_{test}

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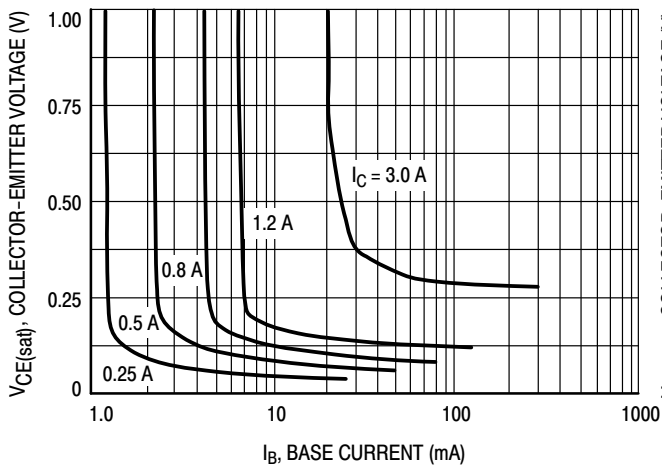


Figure 1. Collector Saturation Region

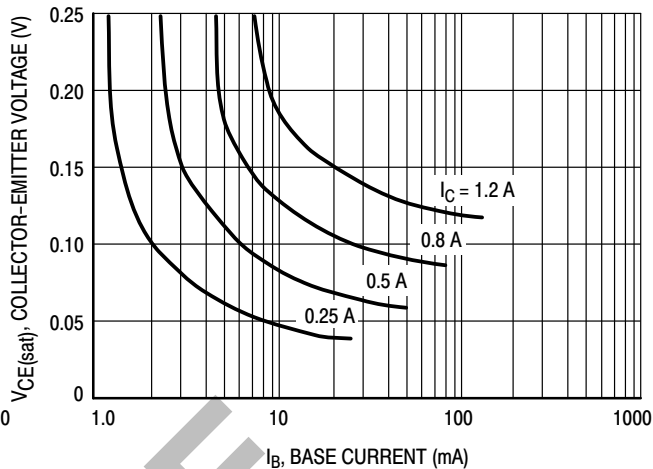


Figure 2. Collector Saturation Region

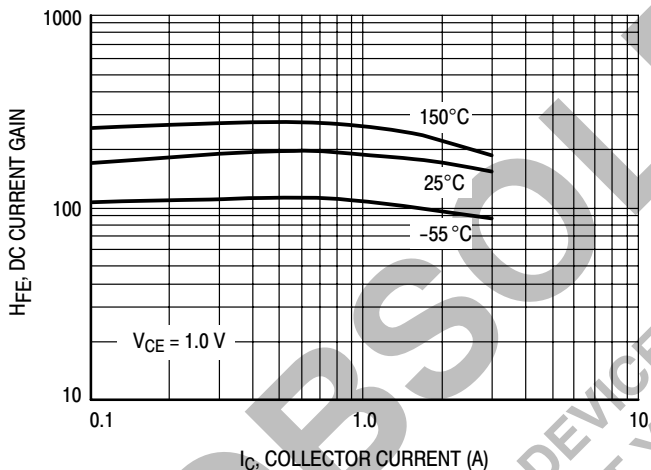


Figure 3. DC Current Gain

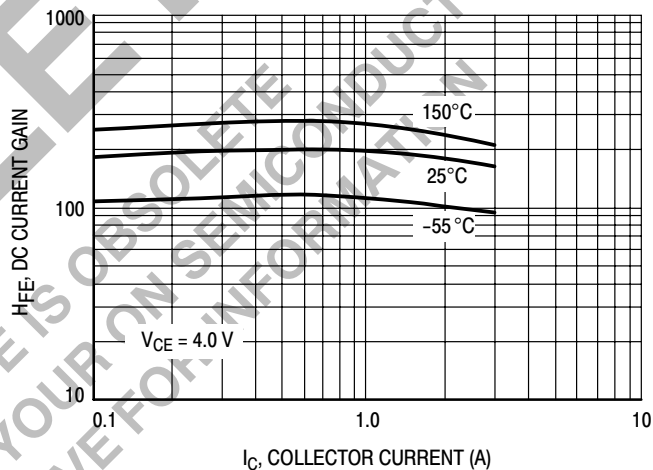


Figure 4. DC Current Gain

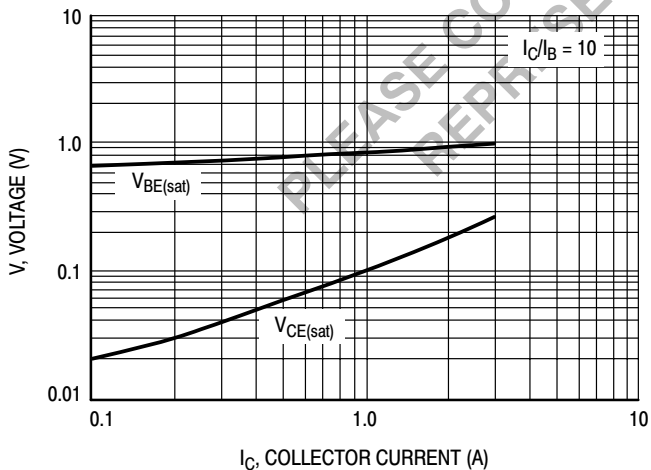


Figure 5. "On" Voltages

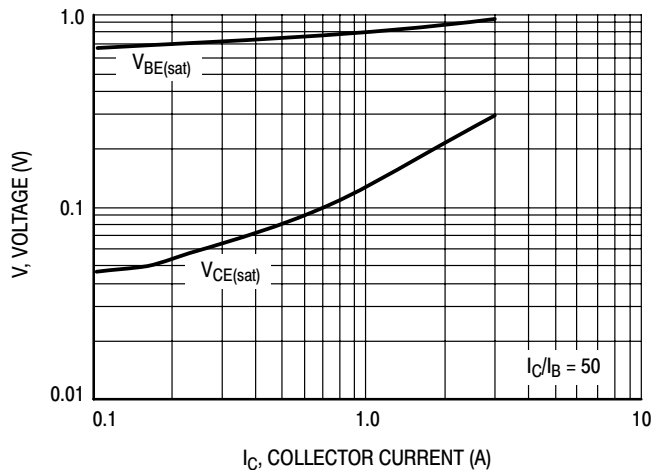


Figure 6. "On" Voltages

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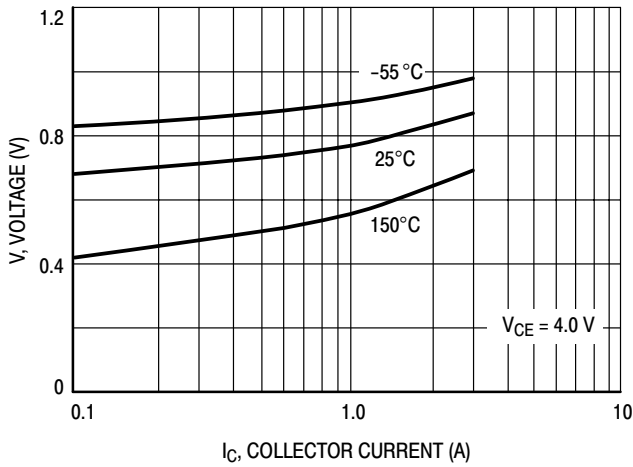


Figure 7. $V_{BE(on)}$ Voltage

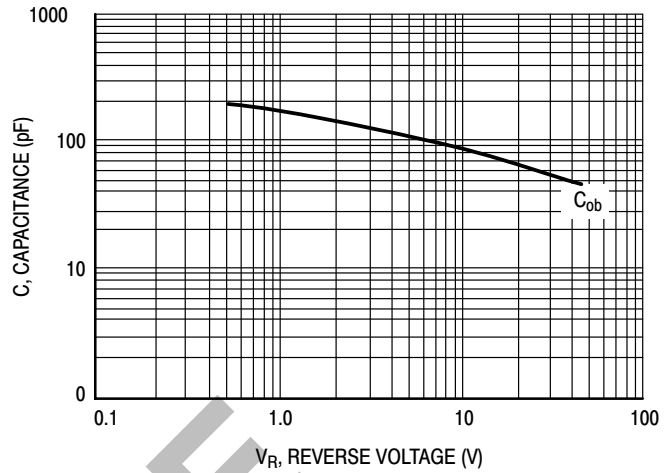


Figure 8. Capacitance

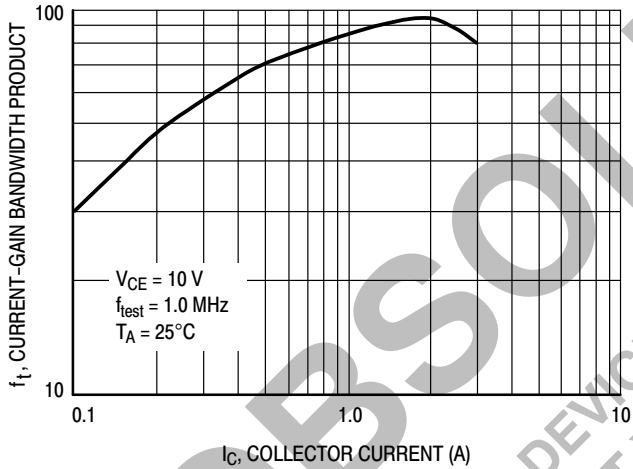


Figure 9. Current-Gain Bandwidth Product

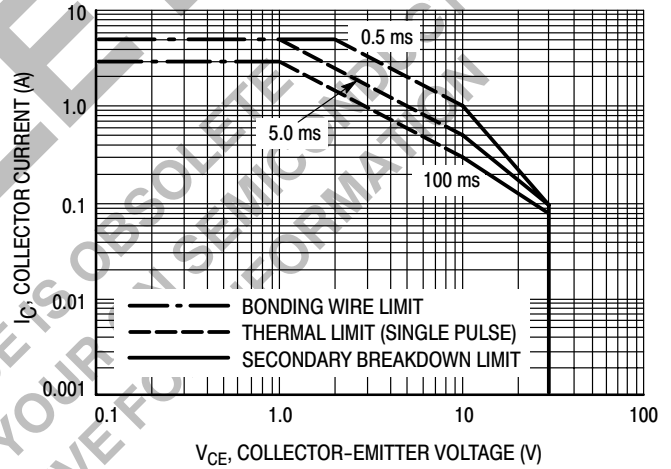


Figure 10. Active Region Safe Operating Area

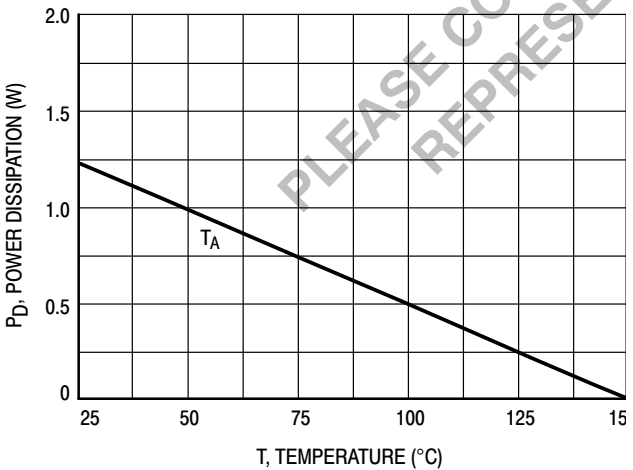


Figure 11. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Secondary breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

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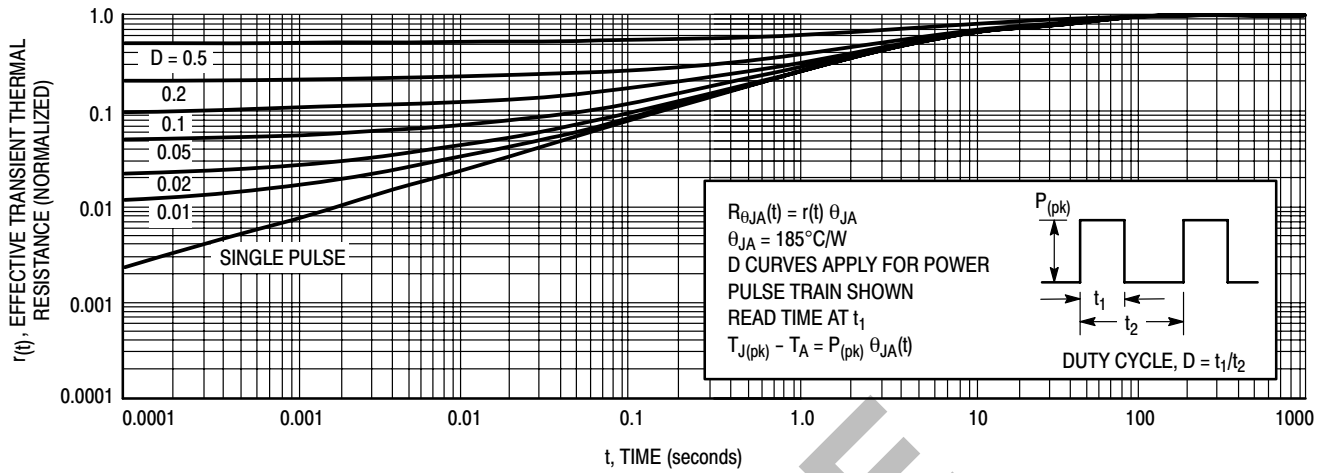


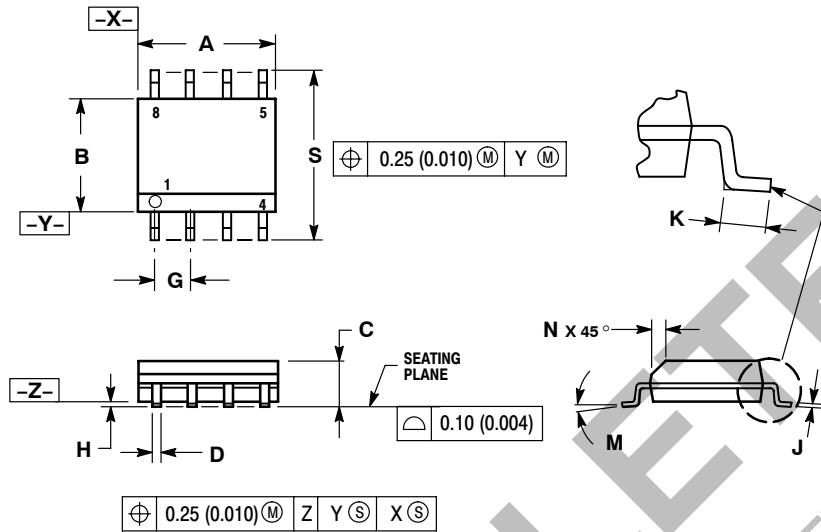
Figure 12. Thermal Response

OBSOLETE
 THIS DEVICE IS OBSOLETE
 PLEASE CONTACT YOUR ON SEMICONDUCTOR
 REPRESENTATIVE FOR INFORMATION

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PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE W



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

STYLE 16:

1. PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

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