

No.09029EAT09

Power Management Switch IC Series for PCs and Digital Consumer Product

Power Switch IC for ExpressCard[™]

BD4154FV

Description

BD4154FV is a power management switch IC for the next generation PC card (ExpressCard[™]) developed by the PCMCIA. It conforms to the PCMCIA ExpressCard[™] Standard, ExpressCard[™] Compliance Checklist, and ExpressCard[™] Implementation Guideline, and obtains the Compliance ID "EC100040" from PCMCIA. The power switch offers a number of functions - card detector, and system status detector - which are ideally suited for laptop and desktop computers.

Features

- 1) Incorporates three low on-resistance FETs for ExpressCard[™].
- 2) Incorporates an FET for output discharge.
- 3) Incorporates an enabler.
- 4) Incorporates under voltage lockout (UVLO) protection.
- 5) Employs an SSOP-B20 package.
- 6) Built-in thermal shutdown protector (TSD).
- 7) Built-in soft start function.
- 8) Incorporates an overcurrent protection (OCP).
- 9) Built-in enable signal for PLL
- 10) Built-in Pull up resistance for detecting ExpressCard[™]

- Conforms to the ExpressCardTM Standard.
 Conforms to the ExpressCardTM Compliance Checklist.
 Conforms to the ExpressCardTM Implementation Guideline.



Applications

Laptop and desktop computers, and other ExpressCard [™] equipped digital devices.

Product Lineup

Parameter	BD4154FV
Package	SSOP-B20

"ExpressCardTM" is a registered trademark registered of the PCMCIA (Personal Computer Memory Card International Association).

●Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
Input Voltage	V3AUX_IN, V3_IN, V15_IN	-0.3~5.0 ^{*1}	V
Logic Input Voltage 1	EN,CPPE#,CPUSB#,SYSR, PERST_IN#,RCLKEN	-0.3~V3AUX_IN+0.3 ^{*1}	V
Logic Output Voltage 1	RCLKEN	-0.3~V3AUX_IN+0.3 ^{*1}	V
Logic Output Voltage 2	PERST#	-0.3~V3AUX_IN+0.3	V
Output Voltage	V3AUX,V3, V15	-0.3~5.0 * ¹	V
Output Current 1	IOV3AUX	1.0	А
Output Current 2	IOV3	2.0	А
Output Current 3	IOV15	2.0	А
Power Dissipation 1	Pd1	500.0 ^{*2}	mW
Power Dissipation 2	Pd2	812.5 ^{*3}	mW
Operating Temperature Range	Topr	-40~+100	°C
Storage Temperature Range	Tstg	-55~+150	°C
Maximum Junction Temperature	Tjmax	+150	°C

*1 Not to exceed Pd.

*2 Reduced by 4.0mW for each increase in Ta of 1°C over 25°C *3 Reduced by 6.5mW for each increase in Ta of 1°C over 25°C(When mounted on a board 70mmx70mmx1.6mm Glass-epoxy PCB)

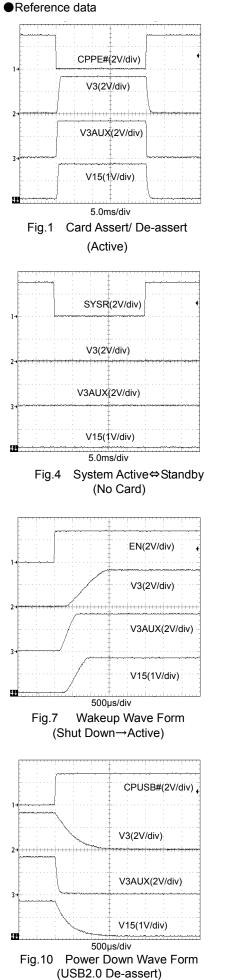
•Operating Conditions (Ta=25°C)

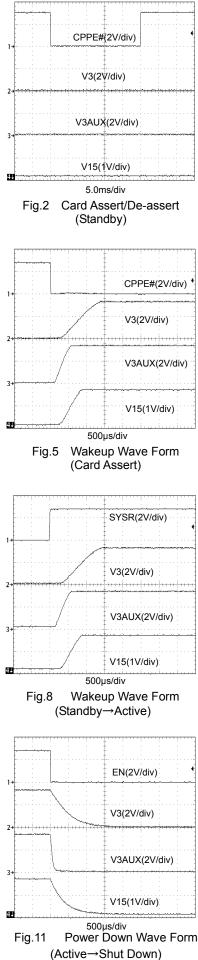
Parameter	Symbol	MIN	MAX	Unit
Input Voltage 1	V3AUX_IN	3.0	3.6	V
Input Voltage 2	V3_IN	3.0	3.6	V
Input Voltage 3	V15_IN	1.35	1.65	V
Logic Input Voltage 1	EN	-0.3	3.6	V
Logic Input Voltage 2	CPPE#,CPUSB#,SYSR, PERST_IN#,RCLKEN	0	V3AUX_IN	V
Logic Output Voltage 1	RCLKEN	0	V3AUX_IN	V
Logic Output Voltage 2	PERST#	0	V3AUX_IN	V
Output Current 1	IOV3AUX	0	275	mA
Output Current 2	IOV3	0	1.3	А
Output Current 3	IOV15	0	650	mA

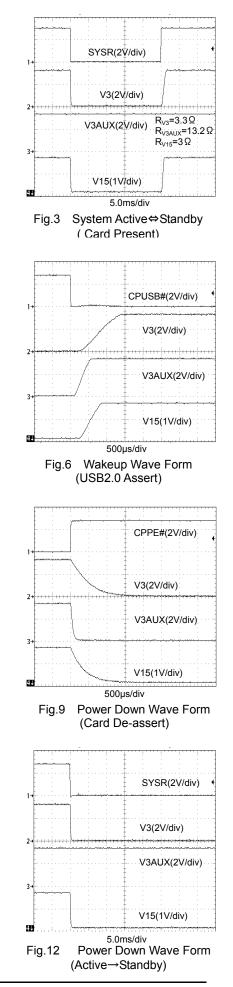
* This product is not designed to offer protection against radioactive rays.

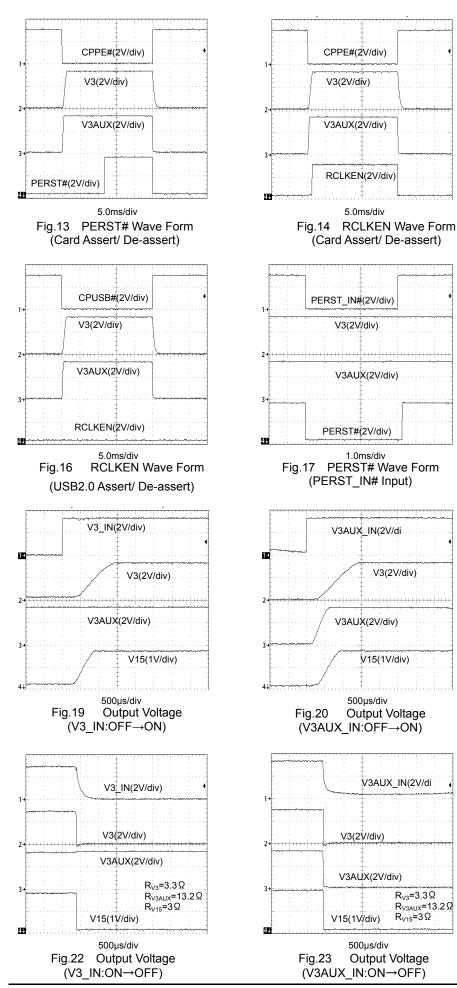
●Electrical Characteristics (unless otherwise noted, Ta=25°C VEN=3.3V V3AUX_IN =V3_IN=3.3V,V15_IN=1.5V)

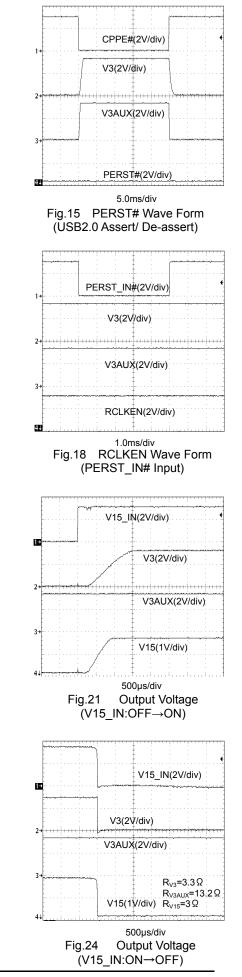
Parameter Symbol Symbol Standby Current Int TYP MAX Vertex Condition Standby Current 1 Ioc1 120 250 µA VENDU (Include IEN, IFCLKEN) Bias Current 2 Ioc2 - 250 µA VSYSRe0. [Enable] Iput Voltage VENH 2.0 - 5.5 V [Enable] Iput Voltage VENU -0.2 - 0.8 V [Logic] - - - 0.4 VENOV - - 0.8 V Low Level Logic Input Voltage VLH 2.0 - - V - 0.8 V Low Level Logic Input Voltage VLH 2.0 - - V - 0.8 V Logic Pin Input Current ISYSR - 0 1 µA CPUSB#-0V - Logic Pin Input Current ISYSR - 0 1 µA RCLKEN Low SVEN -	Liectrical Characteristics (unless	s other wise noted					<u>-vs_iii=5.5v,v15_iii=1.5v)</u>
Standby Qurrent IST - 40 Ø0 μA VEN=0V (Include IEN, IRCLKEN) Bias Current 1 Icc1 - 120 250 μA VSYSR=3.3V [Enable] High Level Enable Input Voltage VENH 2.0 - 0.8 V [Low Level Enable Input Voltage VENH 10 - 30 μA VEN=0V [Logic] High Level Logic Input Voltage VLH 2.0 - 0.8 V [Logic] High Level Logic Input Voltage VLH 2.0 - - V [Logic Pin Input Current ICPPE# - 0 1 μA CPPE#=36V [Logic Pin Input Current ISYSR - 0 1 μA SYSR=36V [Logic Pin Input Current ISYSR - 0 1 μA SYSR=36V [Logic Pin Input Current IRCLKEN - 0 1 μA SYSR=36V [Logic Pin Input Current IRCLKEN - 0 1	Parameter	Symbol				Unit	Condition
Biss Current 1 Icc1 - 120 250 μA SYSR=0V Biss Current 2 Icc2 - 250 500 μA VSYSR=03.V Biss Current 2 Icc2 - 250 500 μA VSYSR=03.V Use Vere Enable Input Voltage VENUV - 5.5 V V Enable Pin Input Current IEN 10 - 0.8 V VENUV Logic Input Voltage VLLIW - - V V V 0.8 V Logic Pin Input Current ISYSR - 0 1 μA SYSR=0V SYSR=0V IgPT_IN# - 0 1 μA SYSR=0V S	Standby Current	IST	-			μА	VEN=0V (Include IEN_IRCLKEN)
Bits Current 2 Icc2 - 250 500 μA VSYSR=3.3V [Enable] High Level Enable Input Voltage VENLOW -0.2 - 0.8 V [Low Level Enable Input Voltage VENLOW -0.2 - 0.8 V [Logic] T 10 - 30 μA VEN=0V [Logic] T - 0.8 V V VEN=0V [Logic] T - 0.8 V VEN=0V [Logic] T - 0.8 V VEN=0V [Logic Pin Input Current [CPUSB# - 0 1 μA CPUSB#-0V [IPRT_IN# - 0 1 μA SYSR=36V VENENT Logic Pin Input Current IRCLKEN - 0 1 μA SYSR=36V [IPRT_IN# - 0 1 μA SERS=0V VENENT SERS=0V [ISVER VISIS - 0 1 μA	-	_	_				
[Enable] VENHI 2.0 - 5.5 V High Level Enable Input Voltage VENLOW 0.2 .0.8 V V Enable Pin Input Current IEN 10 - 0.8 V V High Level Logic Input Voltage VLH 2.0 - - V Low Level Logic Input Voltage VLH 2.0 - - V Low Level Logic Input Voltage VLH 2.0 - 0 1 µA CPPE#3.6V Logic Pin Input Current ICPUSB# - 0 1 µA CPPE#3.6V Logic Pin Input Current ISYSR - 0 1 µA SYSR=0V IPRT_IN# - 0 1 µA SYSR=0V - CCKEN Low Voltage VRCLKEN - 0 1 µA PERST_IN#=3.6V Switch V32 - 60 150 Ω C 10 - 30 µA PERST_IN#=3.6V -							
High Level Enable Input Voltage VENLOW -0.2 - 5.5 V Low Level Enable Input Voltage VENLOW -0.2 - 0.8 V Logic Input Voltage VENLOW - 30 µA VEN=0V Logic Input Voltage VLLOW - - 0.8 V Low Level Logic Input Voltage VLLOW - - 0.8 V Logic Pin Input Current ICPPE# - 0 1 µA CPPE#=3.6V Legic Pin Input Current ISYSR - 0 1 µA CPUSB#=0V IPRT_IN# - 0 1 µA SYSR=3.6V CPUSB#=0V IPRT_IN# - 0 1 µA SYSR=3.6V CPUSB#=0V IPRT_IN# - 0 1 µA RCKEN=3.6V CPUSB#=0V IRCLKEN - 0 1 µA RCKEN=3.6V CPUSB#=0V RCLKEN Leak Current IRCLKEN - 10 -		1002	-	230	500	μΛ	V313IX-3.3V
Low Level Enable Input Voltage VENLOW -0.2 - 0.8 V Enable Pin Input Current IEN 10 - 30 µA VEN=0V Logic Logic Input Voltage VLHI 2.0 - - V High Level Logic Input Voltage VLHI 2.0 - 0 1 µA CPPE#-6V Low Level Logic Input Voltage VLHI - 0.1 µA CPPE#-6V Logic Pin Input Current ICPUSB# - 0 1 µA CPUSB#-36V IRCLKEN - 0 1 µA CPUSB#-36V - IRCLKEN - 0 1 µA CPUSB#-36V - RCLKEN Low Voltage VRCLKEN - 0 1 µA RCLKEN-36V RCLKEN Low Voltage VRCLKEN - 10 - 10 PA RCLKEN-36SV Switch V30 - 160 150 Q - 10 - 10 -	L 1		2.0		55	V	
Enable Pin Input Current IEN 10 - 30 μA VEN=0V [Logic] High Level Logic Input Voltage VLHI 2.0 - - V Low Level Logic Input Voltage VLUOW - - 0.8 V Low Level Logic Input Voltage VLUOW - - 0.8 V Logic Pin Input Current ICPPE# - 0 1 µA CPUSB#=3.6V Logic Pin Input Current ISYSR - 0 1 µA SYSR=3.6V IPRT_IN# - 0 1 µA SYSR=3.6V - IRCLKEN - 0 1 µA PERST_IN#=3.6V - IRCLKEN - 0 1 µA PERST_IN#=3.6V - RCLKEN Low Voltage VRCLKEN - 0 1 µA PERST_IN#=3.6V Switch V13 - - 1 µA PERST_IN#=3.6V - On Resistance Rvaux - <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>							
Logic VLH 2.0 - V High Level Logic Input Voltage VLH 2.0 - - V Low Level Logic Input Voltage VLLOW - 0 1 μA CPPE#-3.6V Low Level Logic Input Voltage VLLOW - 0 1 μA CPPE#-0V Logic Pin Input Current ICPUSB# 10 - 30 μA CPUSB#-3.6V IPRT_IN# 10 - 30 μA SYSR=5.0V - IPRT_IN# - 0 1 μA SYSR=5.0V - IPRT_IN# - 0 1 μA RCLKEN=3.6V - RCLKEN Low Voltage VRCLKEN - 1.1 μA RCKEN=3.6V Switch V3AUXJ - 120 220 mQ Tj=-10~100°C * Switch V3 - 60 150 Q - OR Resistance R _{V10} IS - 60 150 Q Or Resistance <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>							
High Level Logic Input Voltage VLHI 2.0 - - 0.8 V Low Level Logic Input Voltage VLLOW - - 0.8 V Low Level Logic Input Voltage VLLOW - - 0.8 V Logic Pin Input Current ICPPE# - 0 1 µA CPDE#=3.6V Logic Pin Input Current ISYSR - 0 1 µA SYSR=3.6V Logic Pin Input Current IPRT_IN# - 0 1 µA SYSR=3.6V IPRT_IN# - 0 1 µA SYSR=3.6V SYSR=3.6V RCLKEN Low Voltage VRCLKEN - 0 1 µA RCREN=3.6V RCLKEN Low Voltage VRCLKEN - 0.1 0.30 µA PERST_IN#=0V Robistance Ryaux - 120 220 mQ Tj=-10~100°C * Discharge On Resistance Rya - 42 90 mQ Tj=-10~100°C * Discha		IEN	10	-	30	μΑ	VEN=0V
Low Level Logic Input Voltage VLOW - - 0.8 V Low Level Logic Input Voltage VLOW - 0 1 µA CPPE#=3.6V Logic Pin Input Current ICPUSB# - 0 1 µA CPUSB#=3.6V Logic Pin Input Current ISYSR - 0 1 µA CPUSB#=3.6V IPRT_IN# - 0 1 µA SYSR=3.6V 0 IPRT_IN# - 0.1 0.3 Y I		<u> </u>	0.0	1		V	
Inclusion Image: head of the second se			2.0		-	-	
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	Low Level Logic Input Voltage	VLLOW	-				
ICPUSB# - 0 1 μA CPUSB#-36V Logic Pin Input Current ISYSR - 0 1 μA SYSR=3.6V ISYSR - 0 1 μA SYSR=3.6V IPRT_IN# 10 - 30 μA SYSR=3.6V IPRT_IN# 10 - 30 μA SYSR=3.6V IRCLKEN - 0 1 μA SYSR=3.6V IRCLKEN Low Voltage VRCLKEN - 0 1 μA RCLKEN=3.6V Switch V3AUT - 0.1 0.3 μA RCLKEN=3.6V IRCLKEN =3.6V OR Resistance Rv3AUX - 120 220 mQ Tj=-10~100°C * Discharge OR Resistance Rv3Dis - 60 150 Ω IS OR Resistance Rv3Dis - 60 150 Ω IS		ICPPE#	-	0	-		
ICPUSE# 10 - 30 μA CPUSE#=0V Logic Pin Input Current ISYSR - 0 1 μA SYSR=0V IPRT_IN# - 0 1 μA PERST_IN#=3.6V IPRT_IN# - 0 1 μA PERST_IN#=3.6V IRCLKEN - 0 1 μA PERST_IN#=0V RCLKEN Leak Current IRCLKEN - 0.1 0.3 μA RCLKEN=00V RCLKEN Leak Current IRCLKEN - 0.1 0.3 V IRCLKEN=0.56V Switch V3AUX - 120 220 mO Tj=-10~100°C * Discharge On Resistance Rv30. - 42 90 mO Tj=-10~100°C * Discharge On Resistance Rv15 - 45 90 mO Tj=-10~100°C * Orearcurrent OCPv3 1.3 - - A - V3 Over Current OCPv3 1.3 - - A			10	-			
Logic Pin Input Current IO - 30 μA CPUSB#UV Logic Pin Input Current ISYSR - 0 1 μA SYSR=3.6V IPRT_IN# - 0 1 μA SYSR=3.6V IRCLKEN - 0 1 μA SYSR=3.6V RCLKEN Low Voltage VRCLKEN - 0 1 μA PERST_IN#=0V RCLKEN Leak Current IRCLKEN - 0.1 0.3 VI RCLKEN=0V RCLKEN=0V Switch V3AUX - 120 220 mQ Tj=10~100°C * Discharge On Resistance Rv3aux - 120 220 mQ Tj=-10~100°C * On Resistance Rv3aux - 120 220 mQ Tj=-10~100°C * On Resistance Rv3aux - 142 90 mQ Tj=-10~100°C * On Resistance Rv15 - 455 90 mQ Tj=-10~100°C * On Resistance Rv15 - 45		ICPUSB#	-	0			
Logic Plin Input Current ISYSR 10 - 30 μA SYSR=0V IPRT_IN# - 0 1 μA PERST_IN#=36V IRCLKEN - 0 1 μA PERST_IN#=36V RCLKEN Low Voltage VRCLKEN - 0 1 μA RCLKEN=3.6V RCLKEN Leak Current IRCLKEN - 1 μA RCLKEN=0.5mA Switch V3AUX] - 120 220 mQ T[=-10~100°C * On Resistance R _{V3AUX} - 120 220 mQ T[=-10~100°C * Switch V3 On Resistance R _{V3} - 42 90 mQ T[=-10~100°C * On Resistance R _{V15} - 45 90 mQ T[=-10~100°C * Discharge On Resistance R _{V15} - 45 90 mQ T[=-10~100°C * On Resistance R _{V15} - 45 90 mQ T[=-10~100°C * User Current OCP _{V3}			10	-			
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Logic Pin Input Current	ISYSR	-	0			
$\begin{tabular}{ c $			10				
$ \begin{array}{ c c c c c c } \hline \hline \begin{tabular}{ c c c c c } \hline \hline \begin{tabular}{ c c c c c c c } \hline \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$		IPRT IN#	-	0			
IRCLKEN 10 - 30 μA RCLKEN=0V RCLKEN Leak Current IRCLKEN - 0.1 0.3 V IRCLKEN=0.5mA RCLKEN Leak Current IRCLKEN - 1 μA VRCLKEN=3.65V Switch V3AUX] - 120 220 mΩ Tj=-10~100°C * Discharge On Resistance R _{V3AUX} - 60 150 Ω Switch V3] - 60 150 Ω Tj=-10~100°C * Discharge On Resistance R _{V3} Dis - 60 150 Ω Switch V15] - 45 90 mΩ Tj=-10~100°C * On Resistance R _{V15} Dis - 60 150 Ω Icver Current Protection] - 45 90 mΩ Tj=-10~100°C * V3 Over Current Protection] OCPv3 1.3 - - A V15 Over Current Protection] OCPv3 1.3 - - A V16 Over Current OCPv3			10		30		—
ID - 30 PA PCLKEN RCLKEN Leak Current IRCLKEN - 0.1 0.3 V IRCLKEN-0.5mA RCLKEN Leak Current IRCLKEN - 1 μ A VRCLKEN-3.65V Switch V3AUX] - 120 220 mΩ Tj=-10~100°C * Discharge On Resistance R _{V3AUX} Dis - 60 150 Ω Switch V3] - 42 90 mΩ Tj=-10~100°C * Discharge On Resistance R _{V3} - 42 90 mΩ Tj=-10~100°C * Discharge On Resistance R _{V15} - 60 150 Ω - On Resistance R _{V15} Dis - 60 150 Ω - IOver Current Protection - A - A - - V3 Over Current OCPv3 1.3 - - A - V15 Over Current OCPv34UX 0.275 - - A -			-	0			
RCLKEN Leak Current IRCLKEN - - 1 μA VRCLKEN=3.65V [Switch V3AUX] - 120 220 mΩ Tj=-10~100°C * Discharge On Resistance Rv3AuX - 60 150 Ω [Switch V3] - 60 150 Ω - On Resistance Rv3 - 42 90 mΩ Tj=-10~100°C * [Switch V15] - 60 150 Ω - - On Resistance Rv15 - 45 90 mΩ Tj=-10~100°C * [Switch V15] - 60 150 Ω - - A [Over Current Protection] - - A - - - V3 Over Current OCPv3 1.3 - - A - V3AUX Over Current OCPv3 0.65 - A - - V3 IN Hysteresis Voltage VUVLOv3.IN 2.70 2.80 2.90 </td <td></td> <td>INCEREN</td> <td>10</td> <td>-</td> <td>30</td> <td>μA</td> <td>RCLKEN=0V</td>		INCEREN	10	-	30	μA	RCLKEN=0V
[Switch V3AUX] RV3AUX - 120 220 mΩ Tj=-10~100°C * Discharge On Resistance R _{V3AUX} Dis - 60 150 Ω On Resistance R _{V3} - 42 90 mΩ Tj=-10~100°C * Discharge On Resistance R _{V3} - 42 90 mΩ Tj=-10~100°C * Discharge On Resistance R _{V15} - 60 150 Ω On Resistance R _{V15} - 45 90 mΩ Tj=-10~100°C * Discharge On Resistance R _{V15} Dis - 60 150 Ω (Over Current Protection] V V V N Q 0.275 - A V15 Over Current OCP _{V34UX} 0.275 - A V10 VOL Orf Voltage VUVLO _{V3,IN} 2.70 2.80 2.90 V sweep up V3_IN UVLO OFF Voltage VUVLO _{V3,IN} 2.70 2.80 2.90 V sweep down	RCLKEN Low Voltage	VRCLKEN	-	0.1	0.3	V	IRCLKEN=0.5mA
On Resistance R _{V3AUX} - 120 220 mΩ Tj=-10~100°C * Discharge On Resistance R _{V3AUX} Dis - 60 150 Ω [Switch V3] 0 Resistance R _{V3} - 42 90 mΩ Tj=-10~100°C * Discharge On Resistance R _{V3} - 42 90 mΩ Tj=-10~100°C * Discharge On Resistance R _{V15} - 45 90 mΩ Tj=-10~100°C * Discharge On Resistance R _{V15} - 45 90 mΩ Tj=-10~100°C * Discharge On Resistance R _{V15} - 45 90 mΩ Tj=-10~100°C * Discharge On Resistance R _{V15} - 45 90 mΩ Tj=-10~100°C * Visich V15] On Resistance R _{V15} - 45 90 mΩ Tj=-10~100°C * Visich V15 OCP _{V34} 1.3 - - A V15 Over Current OCP _{V34}	RCLKEN Leak Current	IRCLKEN	-	-	1	μA	VRCLKEN=3.65V
Discharge On Resistance R_{VAUX} Dis - 60 150 Ω [Switch V3] - 42 90 mΩ Tj=-10~100°C * Discharge On Resistance R_{V3} Dis - 42 90 mΩ Tj=-10~100°C * Discharge On Resistance R_{V15} - 45 90 mΩ Tj=-10~100°C * Discharge On Resistance R_{V15} - 45 90 mΩ Tj=-10~100°C * Discharge On Resistance R_{V15} - 45 90 mΩ Tj=-10~100°C * Discharge On Resistance R_{V15} - 45 90 mΩ Tj=-10~100°C * Discharge On Resistance R_{V15} - 60 150 Ω D Discharge On Resistance R_{V15} - 60 150 Ω D	[Switch V3AUX]						·
[Switch V3] Num A 42 90 mΩ Tj=-10~100°C * Discharge On Resistance R _{V3} - 42 90 mΩ Tj=-10~100°C * [Switch V15] On Resistance R _{V15} - 45 90 mΩ Tj=-10~100°C * [On Resistance R _{V15} - 45 90 mΩ Tj=-10~100°C * Discharge On Resistance R _{V15} Dis - 60 150 Ω Tj=-10~100°C * Ore Current Protection] V3Over Current OCPv3 1.3 - - A V3AUX Over Current OCPv3 1.3 - - A V3AUX Over Current OCPv3 1.3 - - A V3AUX Over Current OCPv3 0.275 - - A V3AUX Over Current OCPv16 0.65 - - A V3AUX UVLO OFF Voltage VUVLO _{V3.IN} 2.70 2.80 2.90 V sweep up V3AUX_IN Hysteresis Voltage </td <td>On Resistance</td> <td>R_{V3AUX}</td> <td>-</td> <td>120</td> <td>220</td> <td>mΩ</td> <td>Tj=-10~100°C *</td>	On Resistance	R _{V3AUX}	-	120	220	mΩ	Tj=-10~100°C *
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	Discharge On Resistance	R _{V3AUX} Dis	-	60	150	Ω	
Discharge On Resistance R _{v3} Dis - 60 150 Ω [Switch V15] - 45 90 mΩ Tj=-10~10°C * Discharge On Resistance R _{V15} Dis - 60 150 Ω [Over Current Protection] - 60 150 Ω - V3 Over Current OCP _{V3AUX} 0.275 - - A V15 Over Current OCP _{V3AUX} 0.275 - - A V15 Over Current OCP _{V3BUX} 0.275 - - A V15 Over Current OCP _{V3BUX} 0.275 - - A V15 Over Current OCP _{V3BUX} 0.270 2.80 V sweep up V3_IN Hysteresis Voltage /UVULO _{V3LN} 50 100 150 mV sweep down V15_IN UVLO OFF Voltage /UVUC _{V3LN} 50 100 150 mV sweep down V15_IN Hysteresis Voltage /UVULO _{V3LN} 50 100 150 mV sw	[Switch V3]						
[Switch V15] Product Product Product Tj=-10~100°C * Discharge On Resistance R _{V15} Dis - 45 90 mΩ Tj=-10~100°C * [Over Current Protection] V3 Over Current OCP _{V3} 1.3 - - A V3 Over Current OCP _{V3} 1.3 - - A V3AUX Over Current OCP _{V3} 0.275 - - A V15 Over Current OCP _{V15} 0.65 - - A V19 Over Current OCP _{V15} 0.65 - - A V104er Voltage Lockout] VUVLO _{V3,IN} 2.70 2.80 2.90 V sweep up V3AUX_IN UVLO OFF Voltage VUVLO _{V3,IN} 2.70 2.80 2.90 V sweep down V3AUX_IN UVLO OFF Voltage VUVLO _{V3,IN} 50 100 150 mV sweep down V3AUX_IN UVLO OFF Voltage VUVLO _{V3,IN} 50 100 150 mV sweep down V15_IN Hysteresis Voltage /UVULO _{V15_IN} 1.15 1.20 1.25 V sweep down <td>On Resistance</td> <td>R_{V3}</td> <td>-</td> <td>42</td> <td>90</td> <td>mΩ</td> <td>Tj=-10~100°C *</td>	On Resistance	R _{V3}	-	42	90	mΩ	Tj=-10~100°C *
[Switch V15] R _{V15} - 45 90 mΩ Tj=-10~100°C * Discharge On Resistance R _{V15} - 60 150 Ω [Over Current Protection] V3 Over Current OCP _{V3} 1.3 - - A V3 Over Current OCP _{V3} 0.275 - - A V15 Over Current OCP _{V15} 0.65 - - A V3_IN UVLO OFF Voltage VUVLO _{V3 IN} 2.70 2.80 2.90 V sweep up V3_IN UVLO OFF Voltage VUVLO _{V3 IN} 50 100 150 mV sweep up V3AUX_IN UVLO OFF Voltage VUVLO _{V3 IN} 50 100 150 mV sweep down V3AUX_IN UVLO OFF Voltage VUVLO _{V3 IN} 50 100 150 mV sweep down V3AUX_IN UVLO OFF Voltage VUVLO _{V3 IN} 50 100 150 mV sweep down V15_IN UVLO OFF Voltage VUVLO _{V15 IN} 50 100 150 mV swee	Discharge On Resistance		-	60	150	Ω	
Discharge On Resistance R _{V15} Dis - 60 150 Ω [Over Current Protection] V3 Over Current OCPV ₃ 1.3 - - A V3 Over Current OCPV _{3AUX} 0.275 - - A V15 Over Current OCPV ₁₅ 0.65 - - A [Under Voltage Lockout] VUVLO OSF Voltage VUVLOV _{3.IN} 2.70 2.80 2.90 V sweep up V3_IN Hysteresis Voltage ∠VUVLO _{V3.IN} 50 100 150 mV sweep down V3AUX_IN UVLO OFF Voltage VUVLO _{V3.IN} 2.70 2.80 2.90 V sweep down V3AUX_IN UVLO OFF Voltage VUVLO _{V3.IN} 50 100 150 mV sweep down V15_IN Hysteresis Voltage ∠VUVLO _{V15.IN} 1.15 1.20 1.25 V sweep down V15_IN Hysteresis Voltage ∠VUVLO _{V15.IN} 50 100 150 mV sweep down V15_IN UVLO OFF Voltage PG _{V3} 2.700				1	1		
Discharge On Resistance R _{V15} Dis - 60 150 Ω [Over Current Protection] V3 Over Current OCPV ₃ 1.3 - - A V3 Over Current OCPV _{3AUX} 0.275 - - A V15 Over Current OCPV ₁₅ 0.65 - - A [Under Voltage Lockout] VUVLO OSF Voltage VUVLOV _{3.IN} 2.70 2.80 2.90 V sweep up V3_IN Hysteresis Voltage ∠VUVLO _{V3.IN} 50 100 150 mV sweep down V3AUX_IN UVLO OFF Voltage VUVLO _{V3.IN} 2.70 2.80 2.90 V sweep down V3AUX_IN UVLO OFF Voltage VUVLO _{V3.IN} 50 100 150 mV sweep down V15_IN Hysteresis Voltage ∠VUVLO _{V15.IN} 1.15 1.20 1.25 V sweep down V15_IN Hysteresis Voltage ∠VUVLO _{V15.IN} 50 100 150 mV sweep down V15_IN UVLO OFF Voltage PG _{V3} 2.700		R _{V15}	-	45	90	mΩ	Tj=-10∼100°C *
$ \begin{matrix} [Over Current Protection] \\ \hline V3 Over Current OCP_{V3} 1.3 A \\ \hline V3AUX Over Current OCP_{V15} 0.65 A \\ \hline V15 Over Current OCP_{V15} 0.65 A \\ \hline V3_{1N} UVLO OFF Voltage VUVLO_{V3_{1N}} 2.70 2.80 2.90 V sweep up \\ \hline V3_{1N} Hysteresis Voltage VUVLO_{V3_{1N}} 2.70 2.80 2.90 V sweep up \\ \hline V3AUX_{1N} UVLO OFF Voltage VUVLO_{V3AUX_{1N}} 2.70 2.80 2.90 V sweep up \\ \hline V3AUX_{1N} Hysteresis Voltage VUVLO_{V3AUX_{1N}} 50 100 150 mV sweep down \\ \hline V15_{1N} UVLO OFF Voltage VUVLO_{V3AUX_{1N}} 50 100 150 mV sweep down \\ \hline V15_{1N} UVLO OFF Voltage VUVLO_{V15_{1N}} 1.15 1.20 1.25 V sweep up \\ \hline V15_{1N} Hysteresis Voltage VUVLO_{V15_{1N}} 50 100 150 mV sweep down \\ \hline V15_{1N} Hysteresis Voltage VUVLO_{V15_{1N}} 50 100 150 mV sweep down \\ \hline V15_{1N} Hysteresis Voltage VUVLO_{V15_{1N}} 50 100 150 mV sweep down \\ \hline V15_{1N} Hysteresis Voltage PG_{V3} 2.700 2.850 3.000 V \\ \hline V3AUX POWER GOOD \\ \hline V0tage PG_{V3AUX} 2.700 2.850 3.000 V \\ \hline V15 POWER GOOD Voltage PG_{V15} 1.200 1.275 1.350 V \\ PERST# LOW Voltage VPERST#LOW - 0.1 0.3 V \\ PERST# LOW Voltage VPERST#HIGH 3.0 V \\ PERST# HIGH Voltage VPERST#HIGH 3.0 V \\ PERST# HIGH Voltage VPERST#HIGH 3.0 V \\ PERST# Belay Time T_{PERST#} 4 - 20 ms \\ PERST# Belay Time T_{PERST#} 4 - 20 ms \\ PERST# Belay Time T_{Y3} 0.1 - 3 ms \\ [OUTPUT RISE TIME] \\ \hline V3_{1N} to V3 X T_{V3} 0.1 - 3 ms \\ \hline V3AUX_{1N} to V3AUX T_{V3AUX} 0.1 - 3 ms \\ \hline V15_{1N} to V15 V15 T_{V15} 0.1 - 3 ms \\ \hline V15_{1N} to V15 V15 \\ \hline T_{V15} 0.1 - 3 ms \\ \hline V15_{1N} to V15 \\ \hline V15_{1N} to $			-	60		Ω	
V3 Over Current OCP _{V3} 1.3 - - A V3AUX Over Current OCP _{V3AUX} 0.275 - A V15 Over Current OCP _{V15} 0.65 - - A V15 Over Current OCP _{V15} 0.65 - - A V15 Over Current OCP _{V31N} 2.70 2.80 2.90 V sweep up V3_IN UVLO OFF Voltage VUVLO _{V31N} 50 100 150 mV sweep down V3AUX_IN UVLO OFF Voltage VUVLO _{V31N} 2.70 2.80 2.90 V sweep down V3AUX_IN UVLO OFF Voltage VUVLO _{V31N} 2.70 2.80 2.90 V sweep down V3AUX_IN UVLO OFF Voltage VUVLO _{V31N} 2.70 2.80 2.90 V sweep down V15_IN UVLO OFF Voltage VUVLO _{V31N} 1.15 1.20 1.25 V sweep down IPOWER GOOD PG _{V3} 2.700 2.850 3.000 V V3AUX POWER GOOD PG _{V34UX} 2.							
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		OCP _{V3}	1.3	-	-	Α	
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $				-	-		
[Under Voltage Lockout] VUVLO _{V3_IN} 2.70 2.80 2.90 V sweep up V3_IN Hysteresis Voltage ∠/VUVLO _{V3_IN} 50 100 150 mV sweep down V3AUX_IN UVLO OFF Voltage VUVLO _{V3AUX_IN} 50 100 150 mV sweep down V3AUX_IN UVLO OFF Voltage VUVLO _{V3AUX_IN} 50 100 150 mV sweep up V3AUX_IN UVLO OFF Voltage ∠/VUVLO _{V3AUX_IN} 50 100 150 mV sweep up V15_IN UVLO OFF Voltage ∠/VUVLO _{V15_IN} 50 100 150 mV sweep down V15_IN Hysteresis Voltage ∠/VUVLO _{V15_IN} 50 100 150 mV sweep down IPOWER GOOD ∠/VUVLO _{V15_IN} 50 100 150 mV sweep down V3AUX POWER GOOD PG _{V3} 2.700 2.850 3.000 V V V15 POWER GOOD Voltage PG _{V15} 1.200 1.275 1.350 V P PERST# LOW Voltage				_	_		
V3_IN_UVLO_OFF_Voltage VUVLO _{V3_IN} 2.70 2.80 2.90 V sweep up V3_IN_Hysteresis Voltage ∠/VUVLO _{V3_IN} 50 100 150 mV sweep down V3AUX_IN_UVLO_OFF_Voltage VUVLO _{V3AUX_IN} 2.70 2.80 2.90 V sweep up V3AUX_IN_Hysteresis Voltage ∠/VUVLO _{V3AUX_IN} 2.70 2.80 2.90 V sweep up V3AUX_IN_Hysteresis Voltage ∠/VUVLO _{V15_IN} 50 100 150 mV sweep down V15_IN_Hysteresis Voltage ∠/UVLO _{V15_IN} 1.15 1.20 1.25 V sweep down V15_IN_Hysteresis Voltage ∠/UVLO _{V15_IN} 50 100 150 mV sweep down IPOWER GOOD ∠/VUVLO _{V15_IN} 50 100 150 mV sweep down V3AUX_POWER GOOD PG _{V3} 2.700 2.850 3.000 V V V15 POWER GOOD Voltage PG _{V15} 1.200 1.275 1.350 V IPERST#LOW Voltage VPERST#LOW		001 113	0.00			~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $			2 70	2.80	2 90	V	sween un
$\begin{array}{c c c c c c c c c c c c c c c c c c c $	¥						
$\begin{array}{c c c c c c c c c c c c c c c c c c c $							
V15_IN_UVLO_OFF_Voltage VUVLO _{V15_IN} 1.15 1.20 1.25 V sweep up V15_IN_Hysteresis Voltage ∠/VUVLO _{V15_IN} 50 100 150 mV sweep up V15_IN_Hysteresis Voltage ∠/VUVLO _{V15_IN} 50 100 150 mV sweep down IPOWER GOOD V 2.700 2.850 3.000 V V V3AUX POWER GOOD PG _{V3AUX} 2.700 2.850 3.000 V V V15 POWER GOOD Voltage PG _{V15} 1.200 1.275 1.350 V V V15 POWER GOOD Voltage VERST#Low - 0.1 0.3 V IPERST=0.5mA PERST# LOW Voltage VPERST#LigH 3.0 - - V IPERST=0.5mA PERST# Delay Time T _{PERST#} 4 - 20 ms IPERST# assertion time Tast - - 500 ns [OUTPUT RISE TIME] V3_IN to V3 T _{V3} 0.1 - 3 ms <tr< td=""><td></td><td>_</td><td></td><td></td><td></td><td></td><td></td></tr<>		_					
$ \begin{array}{ c c c c c c } V15_IN \ Ivsteresis \ Voltage \ $$ /VUVLO_{V15_IN} \ 50 \ 100 \ 150 \ mV \ sweep \ down \ [POWER \ GOOD] \ \\ \hline V3 \ POWER \ GOOD \ Voltage \ PG_{V3} \ 2.700 \ 2.850 \ 3.000 \ V \ \\ V3 \ AUX \ POWER \ GOOD \ Voltage \ PG_{V3AUX} \ 2.700 \ 2.850 \ 3.000 \ V \ \\ \hline V15 \ POWER \ GOOD \ Voltage \ PG_{V15} \ 1.200 \ 1.275 \ 1.350 \ V \ \\ \hline V15 \ POWER \ GOOD \ Voltage \ VPERST \ I_{Low} \ - \ 0.1 \ 0.3 \ V \ \\ PERST \ HIGH \ Voltage \ VPERST \ I_{HIGH} \ 3.0 \ - \ 0.1 \ 0.3 \ V \ \\ PERST \ HIGH \ Voltage \ VPERST \ HIGH \ 3.0 \ - \ - \ V \ \\ \hline PERST \ PERST \ HIGH \ Voltage \ VPERST \ HIGH \ 3.0 \ - \ - \ V \ \\ \hline PERST \ Belay \ Time \ T_{PERST \ HIGH} \ 4 \ - \ 20 \ ms \ \\ \hline PERST \ Belay \ Time \ T_{PERST \ HIGH} \ 4 \ - \ 500 \ ns \ \\ \hline PERST \ Belay \ Time \ T_{PERST \ HIGH} \ 5 \ VPERST \ - \ 5 \ S \ S \ S \ S \ S \ S \ S \ S \ S$							•
[POWER GOOD] V3 POWER GOOD Voltage PG _{V3} 2.700 2.850 3.000 V V3AUX POWER GOOD Voltage PG _{V3AUX} 2.700 2.850 3.000 V V15 POWER GOOD Voltage PG _{V15} 1.200 1.275 1.350 V PERST# LOW Voltage VPERST#Low - 0.1 0.3 V IPERST=0.5mA PERST# HIGH Voltage VPERST# _{HIGH} 3.0 - - V PERST# Delay Time TPERST# 4 - 20 ms PERST# assertion time Tast - - 500 ns [OUTPUT RISE TIME] V3_IN to V3 T _{V3} 0.1 - 3 ms V3AUX_IN to V3AUX T _{V3AUX} 0.1 - 3 ms	, , , ,						
V3 POWER GOOD Voltage PG _{V3} 2.700 2.850 3.000 V V3AUX POWER GOOD Voltage PG _{V3AUX} 2.700 2.850 3.000 V V15 POWER GOOD Voltage PG _{V15} 1.200 1.275 1.350 V PERST# LOW Voltage VPERST#Low - 0.1 0.3 V IPERST=0.5mA PERST# HIGH Voltage VPERST#HIGH 3.0 - - V PERST# Delay Time TPERST# 4 - 20 ms PERST# assertion time Tast - - 500 ns [OUTPUT RISE TIME] V3.IN to V3 T _{V3} 0.1 - 3 ms V3AUX_IN to V3AUX T _{V3AUX} 0.1 - 3 ms	**************************************		50	100	150	mv	sweep down
V3AUX POWER GOOD PGv3AUX 2.700 2.850 3.000 V Voltage PGv15 1.200 1.275 1.350 V V15 POWER GOOD Voltage PGv15 1.200 1.275 1.350 V PERST# LOW Voltage VPERST#Low - 0.1 0.3 V IPERST=0.5mA PERST# HIGH Voltage VPERST#HIGH 3.0 - - V PERST# Delay Time TPERST# 4 - 20 ms PERST# assertion time Tast - - 500 ns [OUTPUT RISE TIME] V3_IN to V3 Tv3 0.1 - 3 ms V3AUX_IN to V3AUX Tv3AUX 0.1 - 3 ms		50	0 700	0.050	0.000		
Voltage PG _{V3AUX} 2.700 2.850 3.000 V V15 POWER GOOD Voltage PG _{V15} 1.200 1.275 1.350 V PERST# LOW Voltage VPERST#Low - 0.1 0.3 V IPERST=0.5mA PERST# HIGH Voltage VPERST#HIGH 3.0 - - V PERST# Delay Time TPERST# 4 - 20 ms PERST# assertion time Tast - - 500 ns [OUTPUT RISE TIME] V3_IN to V3 T _{V3} 0.1 - 3 ms V3AUX_IN to V3AUX T _{V3AUX} 0.1 - 3 ms V15_IN to V15 T _{V15} 0.1 - 3 ms	5	PG _{V3}	2.700	2.850	3.000	V	
Voltage PG _{V15} 1.200 1.275 1.350 V PERST# LOW Voltage VPERST#Low - 0.1 0.3 V IPERST=0.5mA PERST# HIGH Voltage VPERST#LOH 3.0 - - V PERST# Delay Time TPERST# 4 - 20 ms PERST# assertion time Tast - - 500 ns [OUTPUT RISE TIME] V3_IN to V3 Tv3 0.1 - 3 ms V3AUX_IN to V3AUX Tv3AUX 0.1 - 3 ms V15_IN to V15 Tv15 0.1 - 3 ms		PG _{V3AUX}	2.700	2.850	3.000	V	
PERST# LOW Voltage VPERST#Low - 0.1 0.3 V I _{PERST} =0.5mA PERST# HIGH Voltage VPERST# _{HIGH} 3.0 - - V PERST# Delay Time T _{PERST#} 4 - 20 ms PERST# assertion time Tast - - 500 ns [OUTPUT RISE TIME] V3_IN to V3 T _{V3} 0.1 - 3 ms V3AUX_IN to V3AUX T _{V3AUX} 0.1 - 3 ms V15_IN to V15 T _{V15} 0.1 - 3 ms						17	
PERST# HIGH Voltage VPERST# _{HIGH} 3.0 - - V PERST# Delay Time T _{PERST#} 4 - 20 ms PERST# assertion time Tast - - 500 ns [OUTPUT RISE TIME] - - 500 ns V3_IN to V3 T _{V3} 0.1 - 3 ms V3AUX_IN to V3AUX T _{V3AUX} 0.1 - 3 ms V15_IN to V15 T _{V15} 0.1 - 3 ms			1.200				-0.5mA
PERST# Delay Time T _{PERST#} 4 - 20 ms PERST# assertion time Tast - - 500 ns [OUTPUT RISE TIME] - - - 500 ns V3_IN to V3 T _{V3} 0.1 - 3 ms V3AUX_IN to V3AUX T _{V3AUX} 0.1 - 3 ms V15_IN to V15 T _{V15} 0.1 - 3 ms			-	0.1	0.3		IPERST=U.DITIA
PERST# assertion time Tast - - 500 ns [OUTPUT RISE TIME] - - 500 ns V3_IN to V3 T _{V3} 0.1 - 3 ms V3AUX_IN to V3AUX T _{V3AUX} 0.1 - 3 ms V15_IN to V15 T _{V15} 0.1 - 3 ms				-	-		
[OUTPUT RISE TIME] V3_IN to V3 T _{V3} 0.1 - 3 ms V3AUX_IN to V3AUX T _{V3AUX} 0.1 - 3 ms V15_IN to V15 T _{V15} 0.1 - 3 ms							
V3_IN to V3 T _{V3} 0.1 - 3 ms V3AUX_IN to V3AUX T _{V3AUX} 0.1 - 3 ms V15_IN to V15 T _{V15} 0.1 - 3 ms		Tast	-	-	500	ns	
V3AUX_IN to V3AUX T _{V3AUX} 0.1 - 3 ms V15_IN to V15 T _{V15} 0.1 - 3 ms				1			
V15_IN to V15 T _{V15} 0.1 - 3 ms				-		ms	
				-		ms	
* Design target		T _{V15}	0.1	-	3	ms	



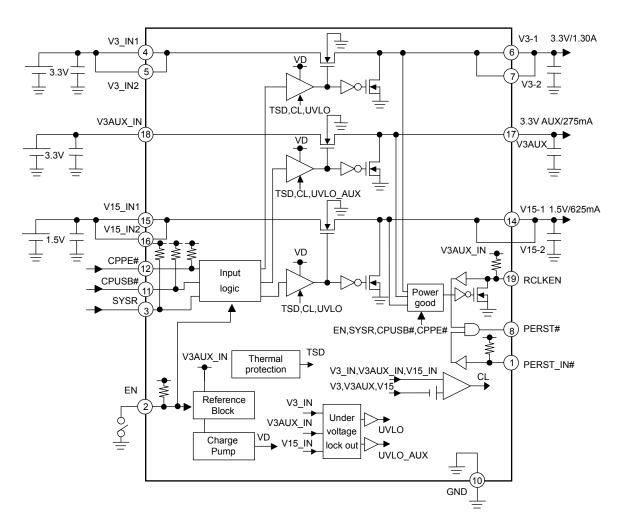




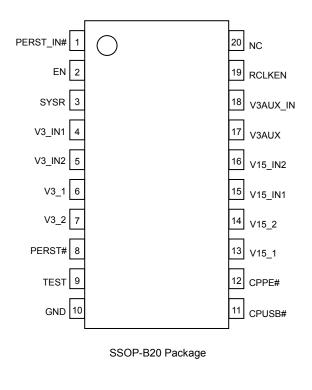




Block Diagram



●PIN CONFIGRATION



●PIN FUNCTION

PIN No	PIN NAME	PIN FUNCTION	
1	PERST_IN#	PERST# control input pin (SysReset#)	
2	EN	Enable input pin	
3	SYSR	Logic input pin	
4	V3_IN1	V3 input pin 1	
5	V3_IN2	V3 input pin 2	
6	V3_1	V3 output pin 1	
7	V3_2	V3 output pin 2	
8	PERST#	Logic output pin	
9	TEST	Test pin	
10	GND	GND pin	
11	CPUSB#	Logic input pin	
12	CPPE#	Logic input pin	
13	V15_1	V15 output pin 1	
14	V15_2	V15 output pin 2	
15	V15_IN1	V15 input pin 1	
16	V15_IN2	V15 input pin 2	
17	V3AUX	V3AUX output pin	
18	V3AUX_IN	V3AUX input pin 1	
19	RCLKEN	Reference clock enable signal/ Power good signal (No delay)	
20	NC	Non connection	

Description of block operation

ΕN

With an input of 2.0 volts or higher, this terminal goes HIGH to activate the circuit, and goes LOW to deactivate the circuit (with the standby circuit current of 40 μ A), It discharges each output and lowers output voltage when the input falls to 0.8 volts or less.

V3_IN, V15_IN, and V3AUX_IN

These are the input terminals for each channel of a 3ch switch. V3_IN and V15_IN terminals have two pins each, which should be short-circuited on the pc board with a thick conductor. A large current runs through these three terminals : (V3_IN: 1.35A; V3AUX_IN: 0.275 A; and V15_IN: 0.625 A). In order to lower the output impedance of the connected power supply, it is recommended that ceramic capacitors (with B-type characteristics or better) be provided between these terminals and the ground. Specifically, the capacitors should be on the order of 1 μ F between V3_IN and GND, and between V15_IN and GND; and on the order of 0.1 μ F between V3AUX_IN and GND.

V3, V15, and V3AUX

These are the output terminals for each switch. The V3 and V15 terminals have two pins each, which should be short-circuited on the PC board and connected to an ExpressCard connector with a thick conductor, as short as possible. In order to stabilize the output, it is recommended that ceramic capacitors (with B-type characteristics or better) be provided between these terminals and the ground. Specifically, the capacitors should be on the order of 10 μ F between V3 and GND, and between V15 and GND; and on the order of 1 μ F between V3AUX and GND.

CPPE#

This pin is used to find whether or not a PCI-Express signal compatible card is present. Turns to "High" level with an input of 2.0 volts or higher, which means that no card is provided, while it turns to "Low" level when the input is lowered to 0.8 volts or less, which means that a card is provided. Controls the ON/OFF, switch selecting the proper mode based on the status of the system.

Pull up resistance $(100k_{\Omega} \sim 200k_{\Omega})$ is built into, so the number of components is reduced.

CPUSB#

This pin is used to find whether or not a USB2.0 signal compatible card is present. Turns to "High" level with an input of 2.0 volts or higher, which means that no card is provided, while it turns to "Low" level when the input is lowered to 0.8 volts or less, which means that a card is provided. Controls the ON/OFF switch, selecting the proper mode based on the system status.

Pull up resistance $(100 \text{ k} \Omega \sim 200 \text{ k} \Omega)$ is built into, so the number of components is reduced.

SYSR

This pin is used to detect the system status. Turns to "High" level with an input of 2.0 volts or higher, which means that the system is activated, while it turns to "Low" level when the input is lowered to 0.8 volts or less, which means that the system is on standby.

PERST_IN#

This pin is used to control the reset signal (PERST#) to a card from the system side. (Also referred to as "SysReset#" by PCMCIA.) Turns to "High" level with an input of 2.0 volts or higher, and sets PERST# to "High" AND with a "Power Good" output. Turns to "Low" level and sets PERST# to "Low" when the input falls to 0.8 volts or less.

PERST#

This pin is used to send a reset signal to a PCI-Express compatible card. Reset status is determined by the outputs, PERST_IN#, CPPE# system status, and EN on/off status. Turns to "High" level and activates the PCI-Express compatible card only if each output is within the "Power Good" threshold, with the card inserted and PERST_IN# turned to "High" level.

RCLKEN

This pin is used to send an enable signal to the reference clock. Activation status is determined by the outputs, CPPE# system status, and EN on/off status. Turns to "High" level and activates the reference clock PLL only if each output is within the "Power Good" threshold, with the card kept inserted.

TEST

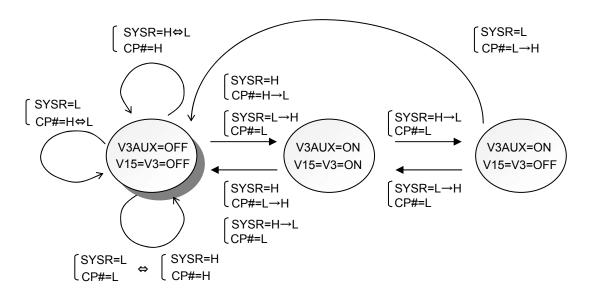
This pin is used to test, which should be short-circuited to the GND. When it is short-circuited to V3AUX_IN, UVLO (V3_IN, V15_IN) turns OFF.

Timing Chart

System Status		ExpressCard [™] Module Status	Power Switch Status		
Primary	Auxiliary	Expresseard Module Status	Primary(+3.3V and +1.5V)	Auxiliary(3.3V Aux)	
OFF	OFF	Don't care	OFF	OFF	
	ON ON		De-asserted	OFF	OFF
ON		Asserted	ON	ON	
		De-asserted	OFF	OFF	
ON ON	ON	Asserted Before This	OFF	ON	
		Asserted After This	OFF	OFF	

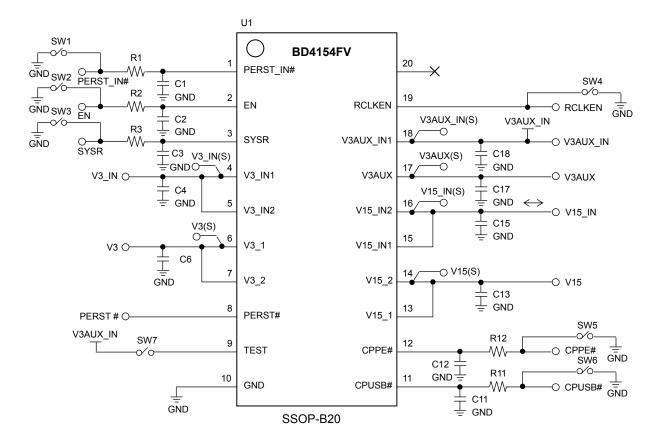
Power ON/OFF Status of ExpressCard[™]

ExpressCard[™] States Transition Diagram



System Status		Card Status	
Stand-by Status	:SYSR=L	Card Asserted Status	:CP#=L
ON Status	:SYSR=H	Card De-asserted Status	:CP#=H
From ON to Stand-by Status	:SYSR=H→L	From De-asserted to Asserted Status	:CP#=H→L
From Stand-by to ON Status	:SYSR=L→H	From Asserted to De-asserted Status	:CP #= L→H

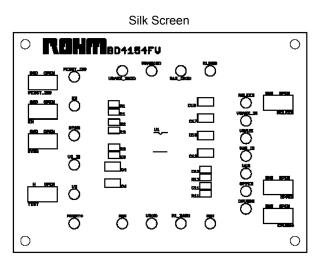
BD4154FV Evaluation Board

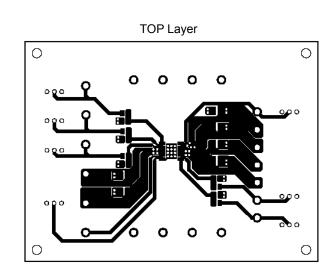


BD4154FV Evaluation Board Application Components

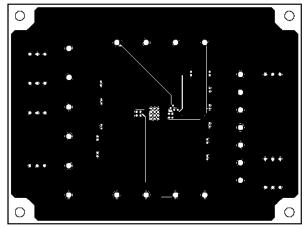
Part No	Value	Company	Part Name
R1	0Ω	ROHM	MCR03series
R2	0Ω	ROHM	MCR03series
R3	ΟΩ	ROHM	MCR03series
R11	ΟΩ	ROHM	MCR03series
R12	ΟΩ	ROHM	MCR03series
C1	-	-	-
C2	-	-	-
C3	-	-	-
C4	1µF	ROHM	MCH213CN 105K
C6	10µF	ROHM	MCH218CN 106K
C11	-	-	-
C12	-	-	-
C13	10µF	ROHM	MCH218CN 106K
C15	1µF	ROHM	MCH213CN 105K
C17	1µF	ROHM	MCH213CN 105K
C18	0.1µF	ROHM	MCH182CN 104K

BD4154FV Evaluation Board Layout

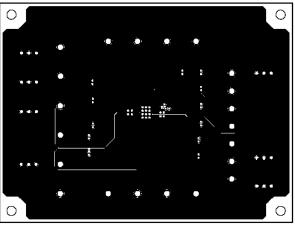




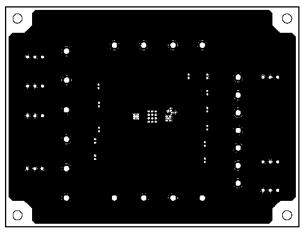
Mid Layer 2



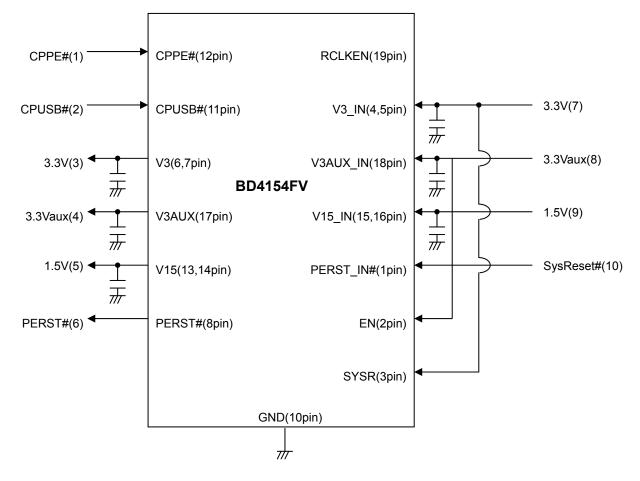
Mid Layer 1



Bottom Layer



●Application Circuit (Circuit for ExpressCard[™] Compliance Checklist)



Heat loss

Thermal design should allow the device to operate within the following conditions. Note that the temperatures listed are the allowed temperature limits. Thermal design should allow sufficient margin from these limits.

- 1. Ambient temperature Ta can be no higher than 100°C.
- 2. Chip junction temperature Tj can be no higher more than 150°C.

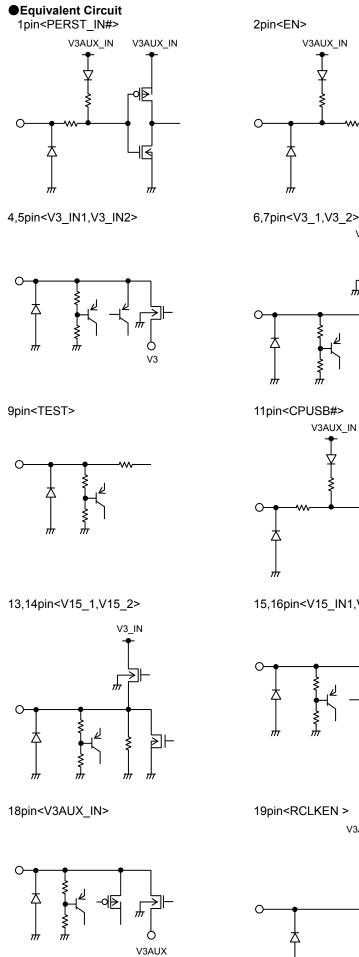
Chip junction temperature Tj can be determined as follows:

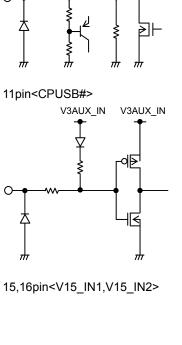
(1) Chip junction temperature Tj is calculated from IC surface temperature TC under actual application conditions: Tj=TC+ θ j-cxW

<Reference value>
 θj -c:SSOP-B2035 /W(2)Chip junction temperature Tj is calculated from ambient temperature Ta:
Tj=TC+ θj -axW
<Reference value>
 θj -a:SSOP-B20250°C/W (IC only)
153.8°C/W Single-layer substrate
(substrate surface copper foil area: less than 3%)

Most of heat loss in the BD4154FV occurs at the output switch. The power lost is determined by multiplying the on-resistance by the square of output current of each switch.

V3AUX_IN





Q

V15

V3AUX_IN

₽ŀ

 π

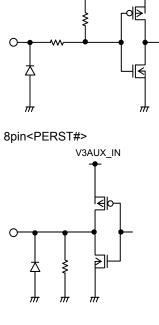
V3AUX_IN

łs

 π

V3_IN

Ŧ

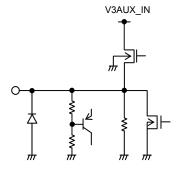


V3AUX_IN

3pin<SYSR>

12pin<CPPE#> V3AUX_IN V3AUX_IN dÞ 0 ि π

17pin<V3AUX>





 $\frac{1}{2}$

Notes for Use

1.Absolute maximum ratings

Although quality is rigorously controlled, the device may be destroyed when applied voltage, operating temperature, etc. exceeds its absolute maximum rating. Because the source (short mode or open mode) cannot be identified once the IC is destroyed, it is important to take physical safety measures such as fusing when implementing any special mode that operates in excess of absolute rating limits.

- 2. Thermal design
- Consider allowable loss (Pd) under actual operating conditions and provide sufficient margin in the thermal design. 3. Terminal-to-terminal short-circuit and mis-mounting

When the mounting the IC to a printed circuit board, take utmost care to assure the position and orientation of the IC are correct. In the event that the IC is mounted erroneously, it may be destroyed. The IC may also be destroyed when a short-circuit is caused by foreign matter introduced into the clearance between outputs, or between an output and power-GND. 4.Operation in strong electromagnetic fields

Using the IC in strong electromagnetic fields may cause malfunctions. Exercise caution in respect to electromagnetic fields. 5.Built-in thermal shutdown protection circuit

This IC incorporates a thermal shutdown protection circuit (TSD circuit). The working temperature is 175°C (standard value) with a -15°C (standard value) hysteresis width. When the IC chip temperature rises the TSD circuit is activated, while the output terminal is brought to the OFF state. The built-in TSD circuit is intended exclusively to shut down the IC in a thermal runaway event, and is not intended to protect the IC or guarantee performance in these conditions. Therefore, do not operate the IC after with the expectation of continued use or subsequent operation once this circuit is activated.

6.Capacitor across output and GND

When a large capacitor is connected across the output and GND, and the V3AUX_IN is short-circuited with 0V or GND for any reason, current charged in the capacitor flows into the output and may destroy the IC. Therefore, use a capacitor smaller than 1000 μ F between the output and GND.

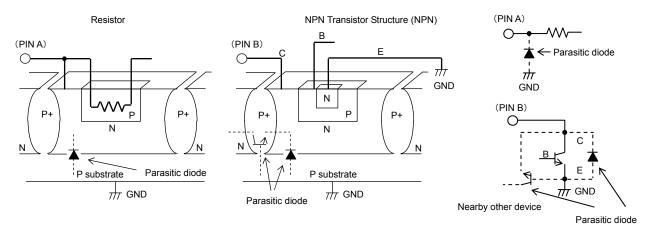
7.Set substrate inspection

Connecting a low-impedance capacitor to a pin when running an inspection with a set substrate may produce stress on the IC. Therefore, be certain to discharge electricity at each process of the operation. To prevent electrostatic accumulation and discharge in the assembly process, thoroughly ground yourself and any equipment that could sustain ESD damage, and continue observing ESD-prevention procedures in all handling, transfer and storage operations. Before attempting to connect the set substrate to the test setup, make certain that the power supply is OFF. Likewise, be sure the power supply is OFF before removing the substrate from the test setup.

8.IC terminal input

This integrated circuit is a monolithic IC, with P substrate and P^+ isolation between elements.

The P layer and N layer of each element form a, PN junction. When the potential relation is GND>terminal A>terminal B, the PN junction works as a diode, and when terminal B>GND terminal A, the PN junction operates as a parasitic transistor. Parasitic elements inevitably form, due to the nature of the IC construction. The operation of the parasitic element gives rise to mutual interference between circuits and results in malfunction, and eventually, breakdown. Consequently, take utmost care not to use the IC in a way that would cause the parasitic element to actively operate, such as applying voltage lower than GND (P substrate) to the input terminal.



9. GND wiring pattern

If both a small signal GND and a high current GND are present, it is recommended that the patterns for the high current GND and the small signal GND be separated. Proper grounding to the reference point of the set should also be provided. In this way, the small signal GND voltage will by unaffected by the change in voltage stemming from the pattern wiring resistance and the high current. Also, pay special attention to avoid undesirable wiring pattern fluctuations in any externally connected GND component.

10. Electrical characteristics

The electrical characteristics in the Specifications may vary, depending on ambient temperature, power supply voltage, circuit(s) externally applied, and/or other conditions. Therefore, please check all such factors, including transient characteristics, that could affect the electrical characteristics.

11. Capacitors applied to input terminals

The capacitors applied to the input terminals (V3_IN, V3AUX_IN and V15_IN) are used to lower the output impedance of the connected power supply. An increase in the output impedance of the power supply may result in destabilization of input voltages (V3_IN, V3AUX_IN and V15_IN). It is recommended that a low-ESR capacitor be used, with a lower temperature coefficient (change in capacitance vs. change in temperature), Recommended capacitors are on the order of 0.1 μ F for V3AUX_IN, and 1 μ F for V3_IN and V15_IN. However, they must be thoroughly checked at the temperature and with the load range expected in actual use, because capacitor selection depends to a significant degree on the characteristics of the input power supply to be used and the conductor pattern of the PC board.

12. Capacitors applied to output terminals

Capacitors for the output terminals (V3, V3_AUX, and V15), should be connected between each of the output terminals and GND. A low-ESR, low temperature coefficient output capacitor is recommended-on the order of 1 μ F for V3 and V15 terminals, and 1 μ F less for V3_AUX. However, they must be thoroughly checked at the temperature and with the load range expected in actual use, because capacitor selection depends to a significant degree on the temperature and the load conditions.

- 13. Not of a radiation-resistant design.
- 14. Allowable loss (Pd)

With respect to the allowable loss, please refer to the thermal derating characteristics shown in the Exhibit, which serves as a rule of thumb. When the system design causes the IC to operate in excess of the allowable loss, chip temperature will rise, reducing the current capacity and decreasing other basic IC functionality. Therefore, design should always enable IC operation within the allowable loss only.

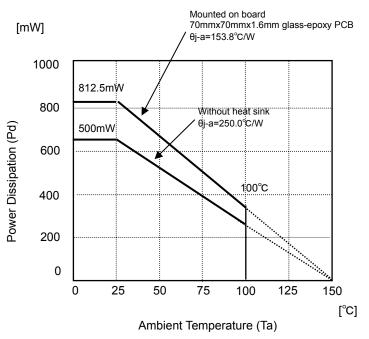
15. Operating range

Basic circuit functions and operations are warranted within the specified operating range the working ambient temperature range. Although reference values for electrical characteristics are not warranted, no rapid or extraordinary changes in these characteristics are expected, provided operation is within the normal operating and temperature range.

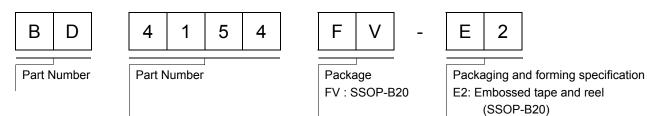
- 16. The applied circuit example diagrams presented here are recommended configurations. However, actual design depends on IC characteristics, which should be confirmed before operation. Also, note that modifying external circuits may impact static, noise and other IC characteristics, including transient characteristics. Be sure to allow sufficient margin in the design to accommodate these factors.
- 17. Wiring to the input terminals (V3 IN, V3AUX IN, and V15 IN) and output terminals (V3, V3AUX and V15) of the built-in FET should be carried out with special care. Using unnecessarily long and/or thin conductors may decrease output voltage and degrade other characteristics.
- 18. Heatsink

The heatsink is connected to the SUB, which should be short-circuited to the GND. Proper heatsink soldering to the PC board should enable lower thermal resistance.

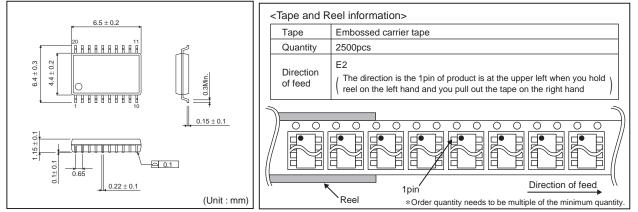
Power Dissipation



Ordering part number



SSOP-B20



	Notes
	g or reproduction of this document, in part or in whole, is permitted without the ROHM Co.,Ltd.
The conter	nt specified herein is subject to change for improvement without notice.
Products'	nt specified herein is for the purpose of introducing ROHM's products (hereinafte '). If you wish to use any such Product, please be sure to refer to the specifications be obtained from ROHM upon request.
illustrate th	of application circuits, circuit constants and any other information contained herein ne standard usage and operations of the Products. The peripheral conditions mus nto account when designing circuits for mass production.
However,	was taken in ensuring the accuracy of the information specified in this document should you incur any damage arising from any inaccuracy or misprint of sucl n, ROHM shall bear no responsibility for such damage.
examples implicitly, a other parti	cal information specified herein is intended only to show the typical functions of and of application circuits for the Products. ROHM does not grant you, explicitly o any license to use or exercise intellectual property or other rights held by ROHM and es. ROHM shall bear no responsibility whatsoever for any dispute arising from the h technical information.
equipment	cts specified in this document are intended to be used with general-use electronic or devices (such as audio visual equipment, office-automation equipment, commu evices, electronic appliances and amusement devices).
The Produ	cts specified in this document are not designed to be radiation tolerant.
	HM always makes efforts to enhance the quality and reliability of its Products, a ay fail or malfunction for a variety of reasons.
against the failure of a shall bear	sure to implement in your equipment using the Products safety measures to guard e possibility of physical injury, fire or any other damage caused in the event of the ny Product, such as derating, redundancy, fire control and fail-safe designs. ROHM no responsibility whatsoever for your use of any Product outside of the prescribed ot in accordance with the instruction manual.
system wh may result instrument fuel-contro any of the	icts are not designed or manufactured to be used with any equipment, device o nich requires an extremely high level of reliability the failure or malfunction of which in a direct threat to human life or create a risk of human injury (such as a medica t, transportation equipment, aerospace machinery, nuclear-reactor controller oller or other safety device). ROHM shall bear no responsibility in any way for use o Products for the above special purposes. If a Product is intended to be used for any ial purpose, please contact a ROHM sales representative before purchasing.
be control	nd to export or ship overseas any Product or technology specified herein that may led under the Foreign Exchange and the Foreign Trade Law, you will be required to sense or permit under the Law.



Thank you for your accessing to ROHM product informations. More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/