



Active-Clamped, Spread-Spectrum, Current-Mode PWM Controllers

General Description

The MAX5974_ provide control for wide-input-voltage, active-clamped, current-mode PWM, forward converters in Power-over-Ethernet (PoE) powered device (PD) applications. The MAX5974A/MAX5974C are well-suited for universal or telecom input range, while the MAX5974B/MAX5974D also accommodate low input voltage down to 10.5V.

The devices include several features to enhance supply efficiency. The AUX driver recycles magnetizing current instead of wasting it in a dissipative clamp circuit. Programmable dead time between the AUX and main driver allows for zero-voltage switching (ZVS). Under light-load conditions, the devices reduce the switching frequency (frequency foldback) to reduce switching losses.

The MAX5974A/MAX5974B feature unique circuitry to achieve output regulation without using an optocoupler, while the MAX5974C/MAX5974D utilize the traditional optocoupler feedback method. An internal error amplifier with a 1% reference is very useful in nonisolated design, eliminating the need for an external shunt regulator.

The devices feature a unique feed-forward maximum duty-cycle clamp that makes the maximum clamp voltage during transient conditions independent of the line voltage, allowing the use of a power MOSFET with lower breakdown voltage. The programmable frequency dithering feature provides low-EMI, spread-spectrum operation.

The MAX5974_ are available in 16-pin TQFN-EP packages and are rated for operation over the -40°C to +85°C temperature range.

Features

- ◆ Peak Current-Mode Control, Active-Clamped Forward PWM Controller
- ◆ Regulation Without Optocoupler (MAX5974A/MAX5974B)
- ◆ Internal 1% Error Amplifier
- ◆ 100kHz to 600kHz Programmable $\pm 8\%$ Switching Frequency, Synchronization Up to 1.2MHz
- ◆ Programmable Frequency Dithering for Low-EMI, Spread-Spectrum Operation
- ◆ Programmable Dead Time, PWM Soft-Start, Current Slope Compensation
- ◆ Programmable Feed-Forward Maximum Duty-Cycle Clamp, 80% Maximum Limit
- ◆ Frequency Foldback for High-Efficiency Light-Load Operation
- ◆ Internal Bootstrap UVLO with Large Hysteresis
- ◆ 100 μ A (typ) Startup Supply Current
- ◆ Fast Cycle-by-Cycle Peak Current-Limit, 35ns Typical Propagation Delay
- ◆ 115ns Current-Sense Internal Leading-Edge Blanking
- ◆ Output Short-Circuit Protection with Hiccup Mode
- ◆ Reverse Current Limit to Prevent Transformer Saturation Due to Reverse Current
- ◆ 3mm x 3mm, Lead-Free, 16-Pin TQFN-EP

Applications

PoE IEEE® 802.3af/at Powered Devices
 High-Power PD (Beyond the 802.3af/at Standard)
 Active-Clamped Forward DC-DC Converters
 IP Phones
 Wireless Access Nodes
 Security Cameras

Ordering Information

PART	TOP MARK	PIN-PACKAGE	UVLO THRESHOLD (V)	FEEDBACK MODE
MAX5974AETE+	+AHY	16 TQFN-EP*	20	Sample/Hold
MAX5974BETE+**	+AHZ	16 TQFN-EP*	10	Sample/Hold
MAX5974CETE+	+AIA	16 TQFN-EP*	20	Continuously Connected
MAX5974DETE+**	+AIB	16 TQFN-EP*	10	Continuously Connected

Note: All devices are specified over the -40°C to +85°C operating temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad. **Future product—Contact factory for availability.

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ABSOLUTE MAXIMUM RATINGS

IN to GND	-0.3V to +24V
EN, NDRV, AUXDRV to GND	-0.3V to (V _{IN} + 0.3V)
RT, DT, FFB, COMP, SS, DCLMP, DITHER/SYNC to GND	-0.3V to +6V
FB to GND (MAX5974A/MAX5974B only)	-6V to +6V
FB to GND (MAX5974C/MAX5974D only)	-0.3V to +6V
CS, CSSC to GND	-0.8V to +6V
PGND to GND	-0.3V to +0.3V
Maximum Input/Output Current (continuous)	
NDRV, AUXDRV	100mA
NDRV, AUXDRV (pulsed for less than 100ns)	±1A

Continuous Power Dissipation (T _A = +70°C) (Note 1)	
16-Pin TQFN (derate 20.8mW/°C above +70°C)	1666mW
Junction-to-Case Thermal Resistance (θ _{JC}) (Note 1)	
16-Pin TQFN	7°C/W
Junction-to-Ambient Thermal Resistance (θ _{JA}) (Note 1)	
16-Pin TQFN	48°C/W
Operating Temperature Range	-40°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maxim-ic.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V (for MAX5974A/MAX5974C, bring V_{IN} up to 21V for startup), V_{CS} = V_{CSSC} = V_{DITHER/SYNC} = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GN}, V_{EN} = +2V, NDRV = AUXDRV = SS = COMP = unconnected, R_{RT} = 34.8kΩ, R_{DT} = 25kΩ, C_{IN} = 1μF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
UNDERVOLTAGE LOCKOUT/STARTUP (IN)							
Bootstrap UVLO Wakeup Level	V _{INUVR}	V _{IN} rising	MAX5974A/ MAX5974C	19.1	19.8	20.4	V
			MAX5974B/ MAX5974D	9.4	9.8	10.25	
Bootstrap UVLO Shutdown Level	V _{INUVF}	V _{IN} falling	6.65	7	7.35	V	
IN Supply Current in Undervoltage Lockout	I _{START}	V _{IN} = +18V (for MAX5974A/ MAX5974C); V _{IN} = +9V (for MAX5974B/MAX5974D), when in bootstrap UVLO		100	150	μA	
IN Supply Current After Startup	I _C	V _{IN} = +12V		1.8	3	mA	
ENABLE (EN)							
Enable Threshold	V _{ENR}	V _{EN} rising	1.17	1.215	1.26	V	
	V _{ENF}	V _{EN} falling	1.09	1.14	1.19		
Input Current	I _{EN}				1	μA	
OSCILLATOR (RT)							
RT Bias Voltage	V _{RT}			1.23		V	
NDRV Switching Frequency Range	f _{sw}		100		600	kHz	
NDRV Switching Frequency Accuracy			-8		+8	%	
Maximum Duty Cycle	D _{MAX}	f _{sw} = 250kHz	79	80	82	%	

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ELECTRICAL CHARACTERISTICS (continued)

(VIN = 12V (for MAX5974A/MAX5974C, bring VIN up to 21V for startup), VCS = VCSSC = VDITHER/SYNC = VFB = VFFB = VDCLMP = VGND, VEN = +2V, NDRV = AUXDRV = SS = COMP = unconnected, RRT = 34.8kΩ, RDT = 25kΩ, CIN = 1μF, TA = -40°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
SYNCHRONIZATION (SYNC)							
Synchronization Logic-High Input	V _{IH-SYNC}		2.91			V	
Synchronization Pulse Width				50		ns	
Synchronization Frequency Range	f _{SYNCIN}		1.1 x f _{sw}		2 x f _{sw}	kHz	
Maximum Duty Cycle During Synchronization			D _{MAX} x f _{SYNC} /f _{sw}			%	
DITHERING RAMP GENERATOR (DITHER)							
Charging Current		V _{DITHER} = 0V	45	50	55	μA	
Discharging Current		V _{DITHER} = 2.2V	43	50	57	μA	
Ramp's High Trip Point				2		V	
Ramp's Low Trip Point				0.4		V	
SOFT-START AND RESTART (SS)							
Charging Current	I _{SS-CH}		9.5	10	10.5	μA	
Discharging Current	I _{SS-D}	V _{SS} = 2V, normal shutdown	0.65	1.34	2	mA	
	I _{SS-DH}	(V _{EN} < V _{ENF} or V _{IN} < V _{INUVF}), V _{SS} = 2V, hiccup mode discharge for t _{RESTART} (Note 3)	1.6	2	2.4	μA	
Discharge Threshold to Disable Hiccup and Restart	V _{SS-DTH}			0.15		V	
Minimum Restart Time During Hiccup Mode	t _{RSTRT-MIN}			1024		Clock Cycles	
Normal Operating High Voltage	V _{SS-HI}			5		V	
Duty-Cycle Control Range	V _{SS-DMAX}	D _{MAX} (typ) = (V _{SS-DMAX} /2.46V)	0		2	V	
DUTY-CYCLE CLAMP (DCLMP)							
DCLMP Input Current	I _{DCLMP}	V _{DCLMP} = 0 to 5V	-100	0	+100	nA	
Duty-Cycle Control Range	V _{DCLMP-R}		V _{DCLMP} = 0.5V	73	75.4	77.5	%
			V _{DCLMP} = 1V	54	56	58	
			V _{DCLMP} = 2V	14.7	16.5	18.3	
NDRV DRIVER							
Pulldown Impedance	R _{NDRV-N}	I _{NDRV} (sinking) = 100mA		1.9	3.4	Ω	
Pullup Impedance	R _{NDRV-P}	I _{NDRV} (sourcing) = 50mA		4.7	8.3	Ω	
Peak Sink Current				1		A	
Peak Source Current				0.65		A	
Fall Time	t _{NDRV-F}	C _{NDRV} = 1nF		14		ns	
Rise Time	t _{NDRV-R}	C _{NDRV} = 1nF		27		ns	

MAX5974A/MAX5974B/MAX5974C/MAX5974D

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ELECTRICAL CHARACTERISTICS (continued)

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AUXDRV DRIVER						
Pull-down Impedance	R_{AUX-N}	I_{AUXDRV} (sinking) = 50mA		4.3	7.7	Ω
Pull-up Impedance	R_{AUX-P}	I_{AUXDRV} (sourcing) = 25mA		10.6	18.9	Ω
Peak Sink Current				0.5		A
Peak Source Current				0.3		A
Fall Time	t_{AUX-F}	$C_{AUXDRV} = 1nF$		24		ns
Rise Time	t_{AUX-R}	$C_{AUXDRV} = 1nF$		45		ns
DEAD-TIME PROGRAMMING (DT)						
DT Bias Voltage	V_{DT}			1.215		V
NDRV to AUXDRV Delay (Dead Time)	t_{DT}	From NDRV falling to AUXDRV falling	$R_{DT} = 10k\Omega$	40		ns
			$R_{DT} = 100k\Omega$	300	350	
		AUXDRV rising to NDRV rising	$R_{DT} = 10k\Omega$	40		ns
			$R_{DT} = 100k\Omega$	310	360	
CURRENT-LIMIT COMPARATORS (CS)						
Cycle-by-Cycle Peak Current-Limit Threshold	$V_{CS-PEAK}$		375	393	410	mV
Cycle-by-Cycle Reverse Current-Limit Threshold	V_{CS-REV}	Turns AUXDRV off for the remaining cycle if reverse current limit is exceeded	-118	-100	-88	mV
Current-Sense Blanking Time for Reverse Current Limit	$t_{CS-BLANK-REV}$	From AUXDRV falling edge		115		ns
Number of Consecutive Peak Current-Limit Events to Hiccup	N_{HICCUP}			8		Events
Current-Sense Leading-Edge Blanking Time	$t_{CS-BLANK}$	From NDRV rising edge		115		ns
Propagation Delay from Comparator Input to NDRV	t_{PDCS}	From CS rising (10mV overdrive) to NDRV falling (excluding leading-edge blanking)		35		ns
Minimum On-Time	t_{ON-MIN}		100	150	200	ns
SLOPE COMPENSATION (CSSC)						
Slope Compensation Current Ramp Height		Current ramp's peak added to CSSC input per switching cycle	47	52	58	μA
PWM COMPARATOR						
Comparator Offset Voltage	V_{PWM-OS}	$V_{COMP} - V_{CSSC}$	1.35	1.7	2	V
Current-Sense Gain	$ACS-PWM$	$\Delta V_{COMP}/\Delta V_{CSSC}$ (Note 4)	3.1	3.33	3.6	V/V
Current-Sense Leading-Edge Blanking Time	$t_{CSSC-BLANK}$	From NDRV rising edge		115		ns
Comparator Propagation Delay	t_{PWM}	Change in $V_{CSSC} = 10mV$ (including internal leading-edge blanking)		150		ns

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PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
ERROR AMPLIFIER							
FB Reference Voltage	V_{REF}	V_{FB} when $I_{COMP} = 0$, $V_{COMP} = 2.5V$	MAX5974A/ MAX5974B	1.5	1.52	1.54	V
			MAX5974C/ MAX5974D	1.202	1.215	1.227	
FB Input Bias Current	I_{FB}	$V_{FB} = 0$ to $1.75V$	MAX5974A/ MAX5974B	-250		+250	nA
			MAX5974C/ MAX5974D	-500		+100	
Voltage Gain	A_{EAMP}			80		dB	
Transconductance	g_m		MAX5974A/ MAX5974B	1.8	2.55	3.2	mS
			MAX5974C/ MAX5974D	1.8	2.66	3.5	
Transconductance Bandwidth	BW	Open loop (typical gain = 1) -3dB frequency	MAX5974A/ MAX5974B		2		MHz
			MAX5974C/ MAX5974D		30		
Source Current		$V_{FB} = 1V$, $V_{COMP} = 2.5V$	300	375	455	μA	
Sink Current		$V_{FB} = 1.75V$, $V_{COMP} = 1V$	300	375	455	μA	
FREQUENCY FOLDBACK (FFB)							
V_{CSAVG} -to-FFB Comparator Gain				10		V/V	
FFB Bias Current	I_{FFB}	$V_{FFB} = 0V$, $V_{CS} = 0V$ (not in FFB mode)	26	30	33	μA	
NDRV Switching Frequency During Foldback	f_{SW-FB}			$f_{SW}/2$		kHz	

Note 2: All devices are 100% production tested at $T_A = +25^\circ C$. Limits over temperature are guaranteed by design.

Note 3: See the *Output Short-Circuit Protection with Hiccup Mode* section.

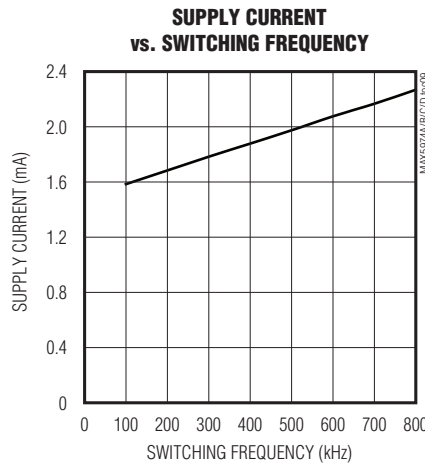
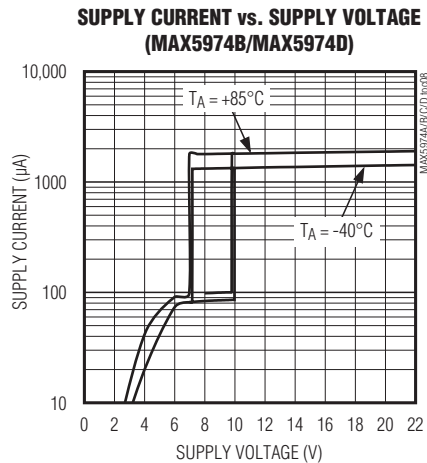
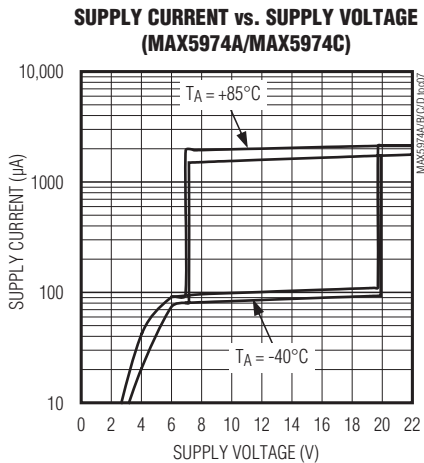
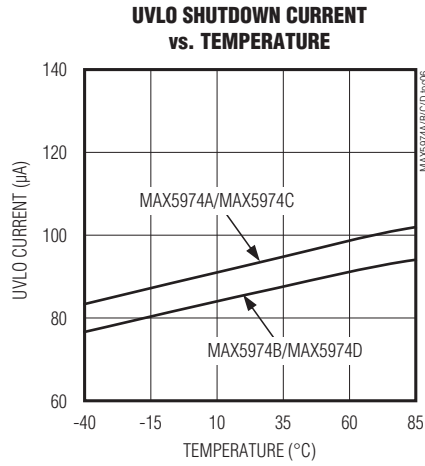
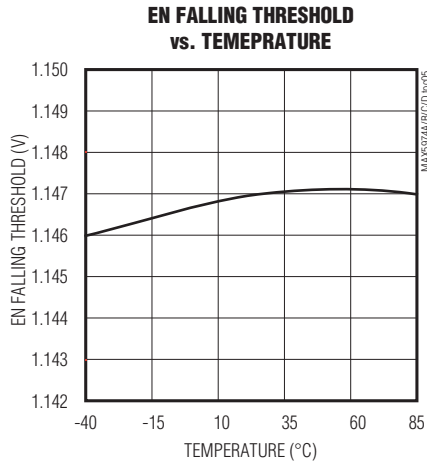
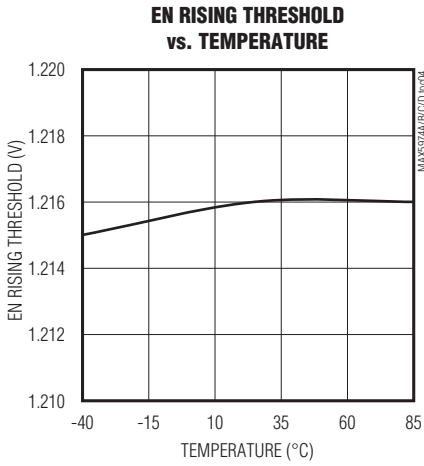
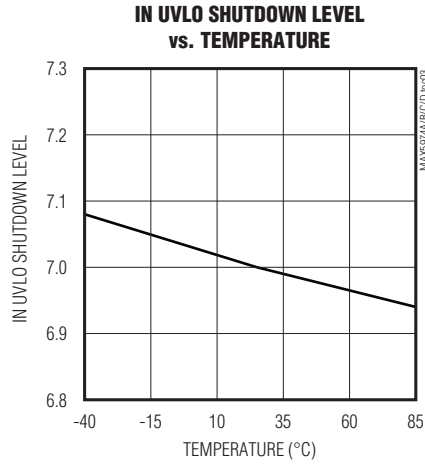
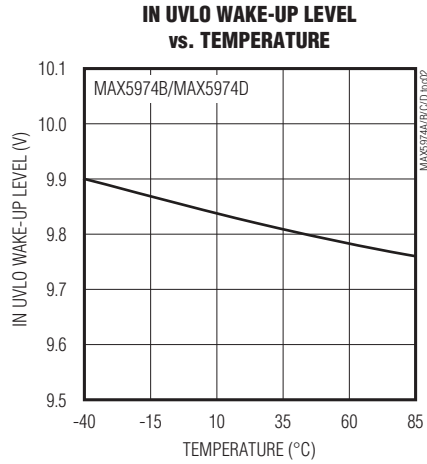
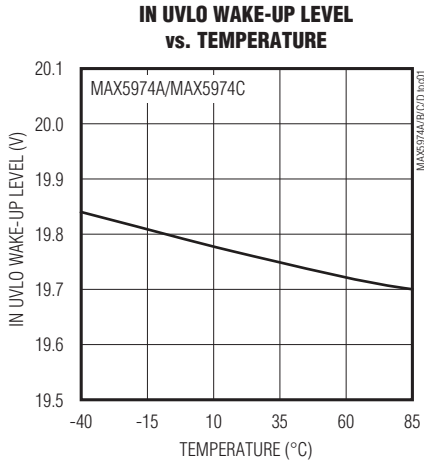
Note 4: The parameter is measured at the trip point of latch with $V_{FB} = 0V$. Gain is defined as $\Delta V_{COMP}/\Delta V_{CSSC}$ for $0.15V < \Delta V_{CSSC} < 0.25V$.

MAX5974A/MAX5974B/MAX5974C/MAX5974D

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Typical Operating Characteristics

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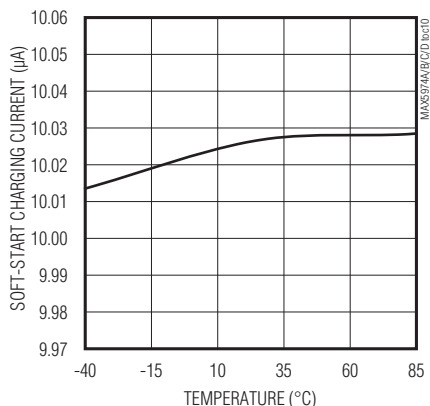
Active-Clamped, Spread-Spectrum, Current-Mode PWM Controllers

Typical Operating Characteristics (continued)

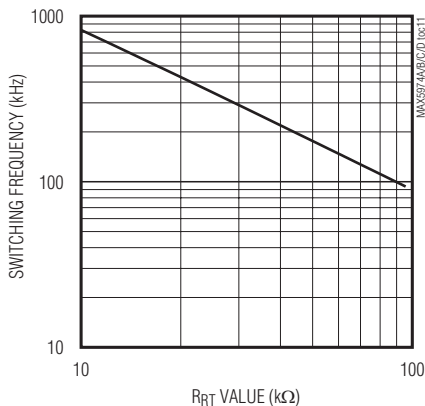
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MAX5974A/MAX5974B/MAX5974C/MAX5974D

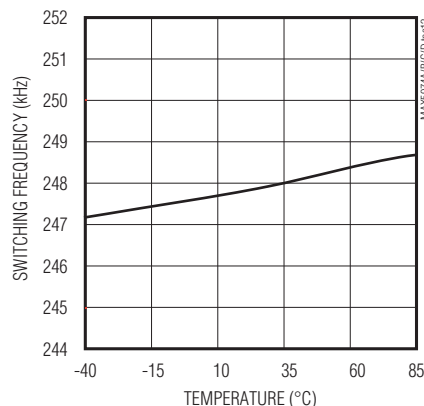
SOFT-START CHARGING CURRENT vs. TEMPERATURE



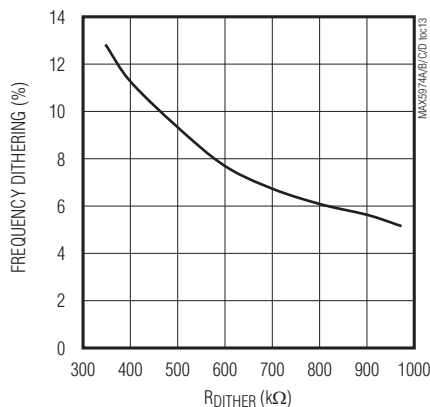
SWITCHING FREQUENCY vs. R_{RT} VALUE



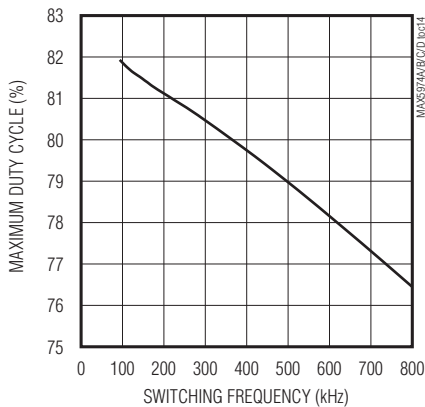
SWITCHING FREQUENCY vs. TEMPERATURE



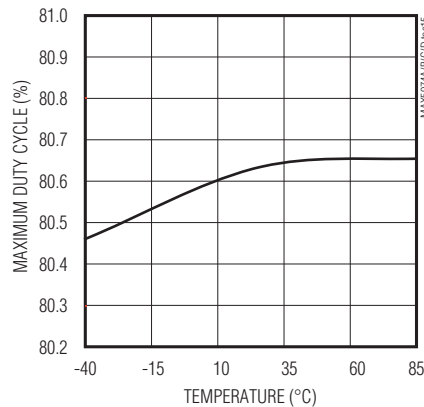
FREQUENCY DITHERING vs. R_{DITHER}



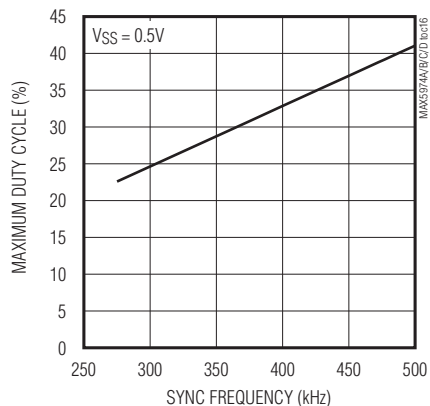
MAXIMUM DUTY CYCLE vs. SWITCHING FREQUENCY



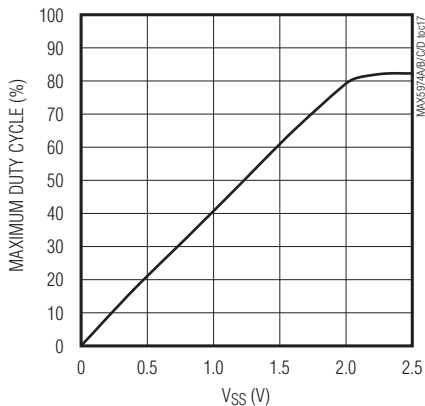
MAXIMUM DUTY CYCLE vs. TEMPERATURE



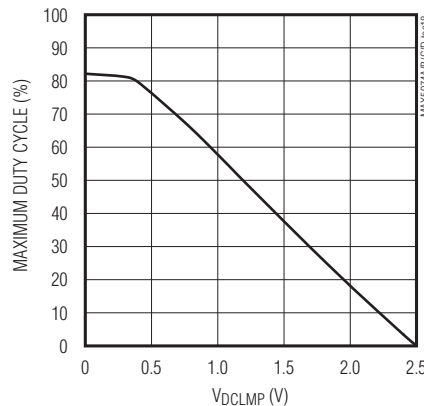
MAXIMUM DUTY CYCLE vs. SYNC FREQUENCY



MAXIMUM DUTY CYCLE vs. V_{SS}



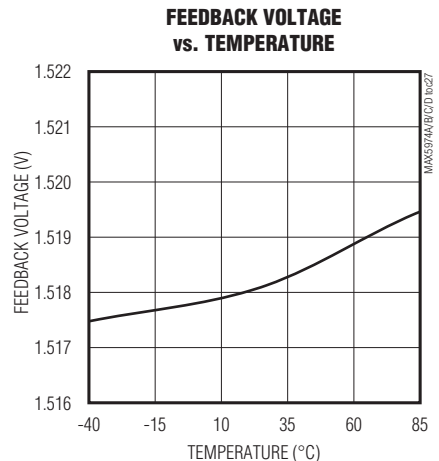
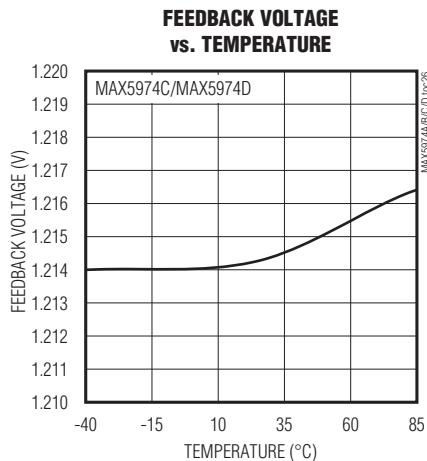
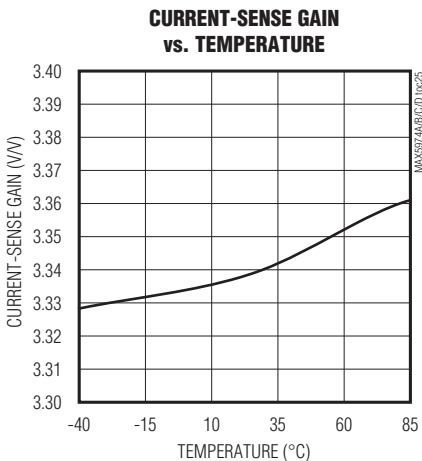
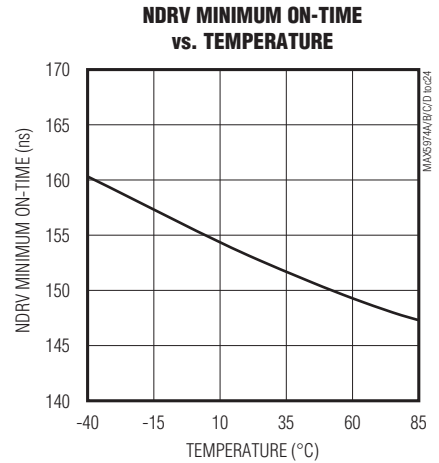
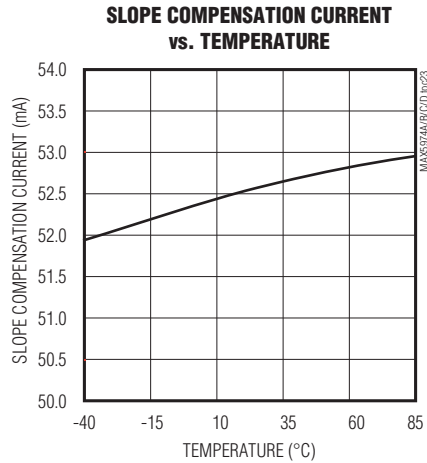
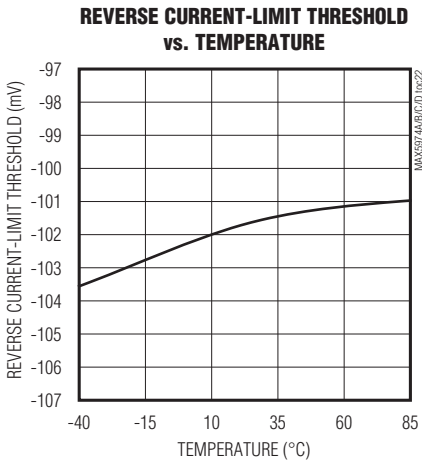
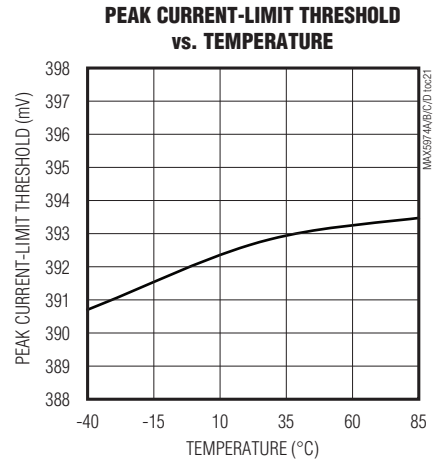
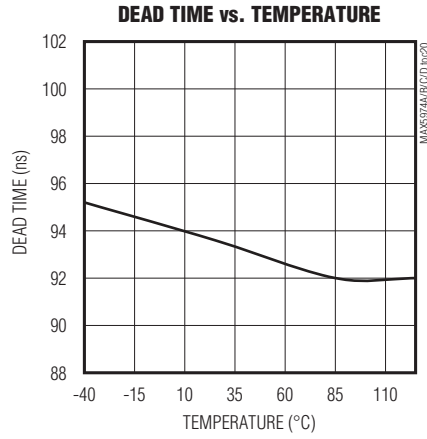
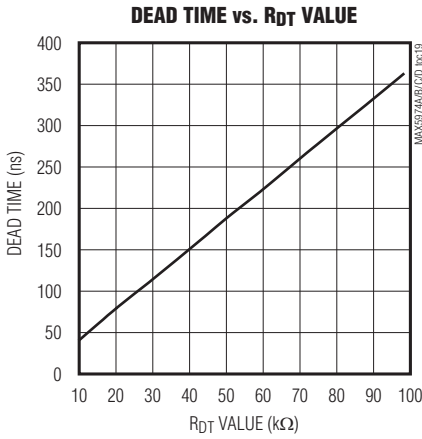
MAXIMUM DUTY CYCLE vs. V_{DCLMP}



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Typical Operating Characteristics (continued)

(VIN = 12V (for MAX5974A/MAX5974C, bring VIN up to 21V for startup), VCS = VCSS = VDITHER/SYNC = VFB = VFFB = VDCLMP = VGND, VEN = 2V, NDRV = AUXDRV = SS = COMP = unconnected, RRT = 34.8kΩ, RDT = 25kΩ, unless otherwise noted.)

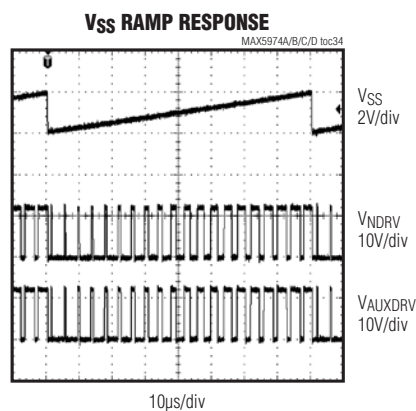
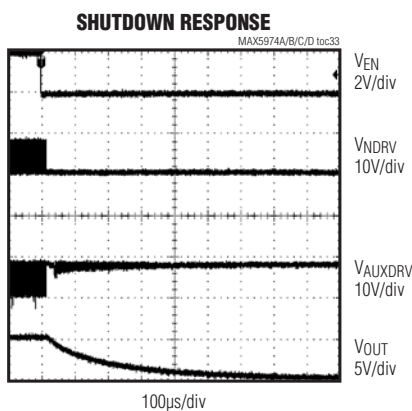
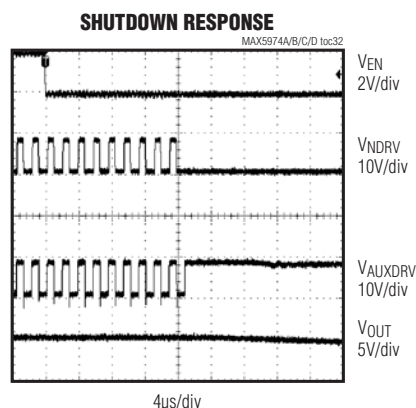
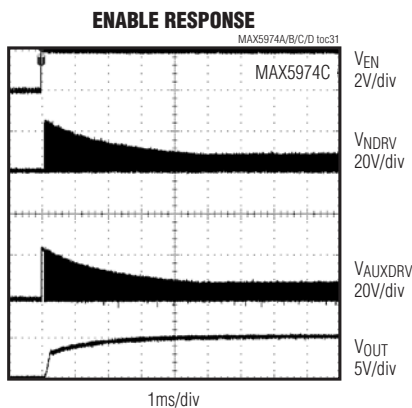
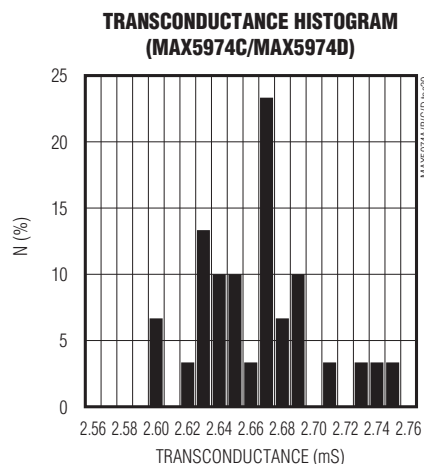
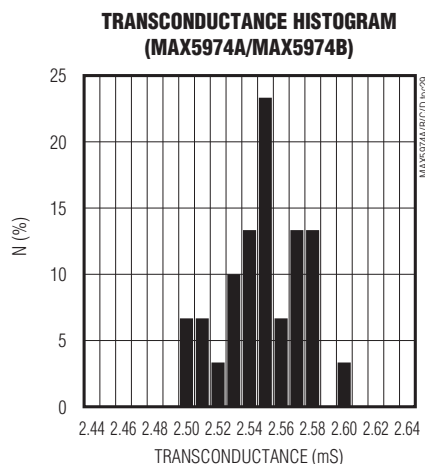
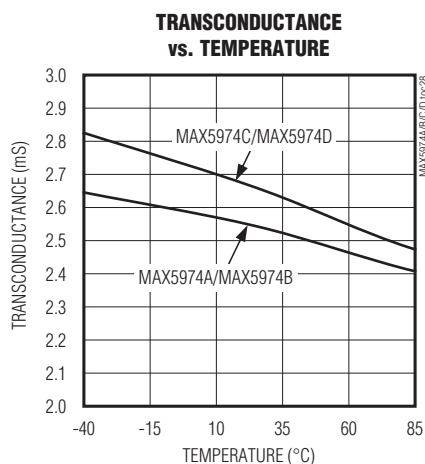


Active-Clamped, Spread-Spectrum, Current-Mode PWM Controllers

Typical Operating Characteristics (continued)

($V_{IN} = 12V$ (for MAX5974A/MAX5974C, bring V_{IN} up to 21V for startup), $V_{CS} = V_{CSSC} = V_{DITHER/SYNC} = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}$, $V_{EN} = 2V$, $NDRV = AUXDRV = SS = COMP =$ unconnected, $R_{RT} = 34.8k\Omega$, $R_{DT} = 25k\Omega$, unless otherwise noted.)

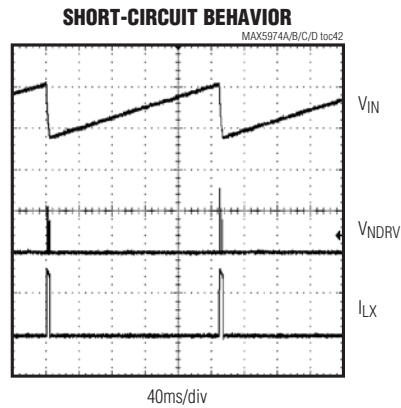
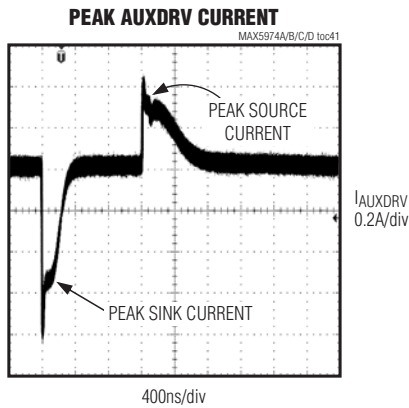
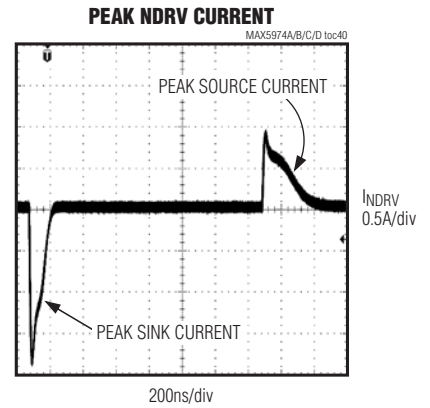
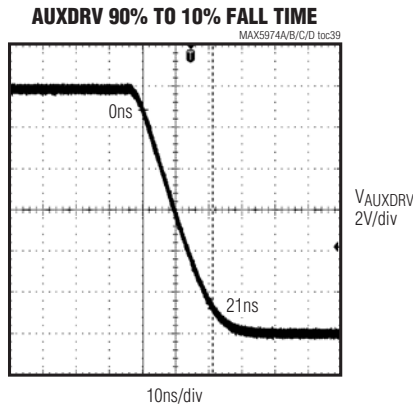
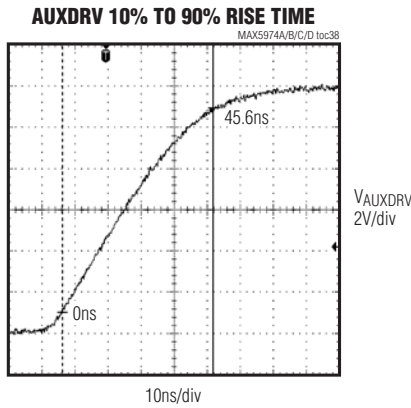
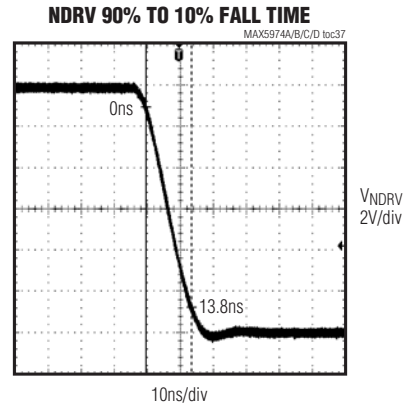
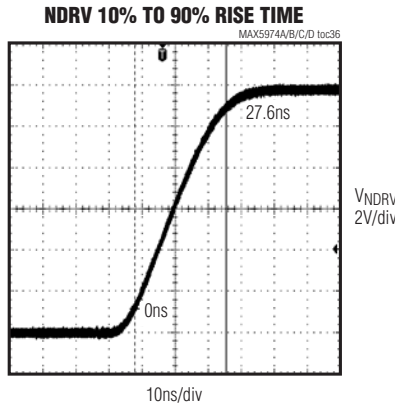
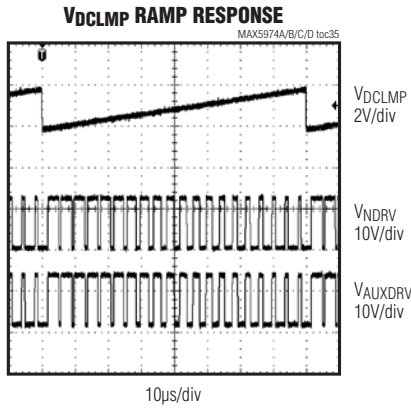
MAX5974A/MAX5974B/MAX5974C/MAX5974D



Active-Clamped, Spread-Spectrum, Current-Mode PWM Controllers

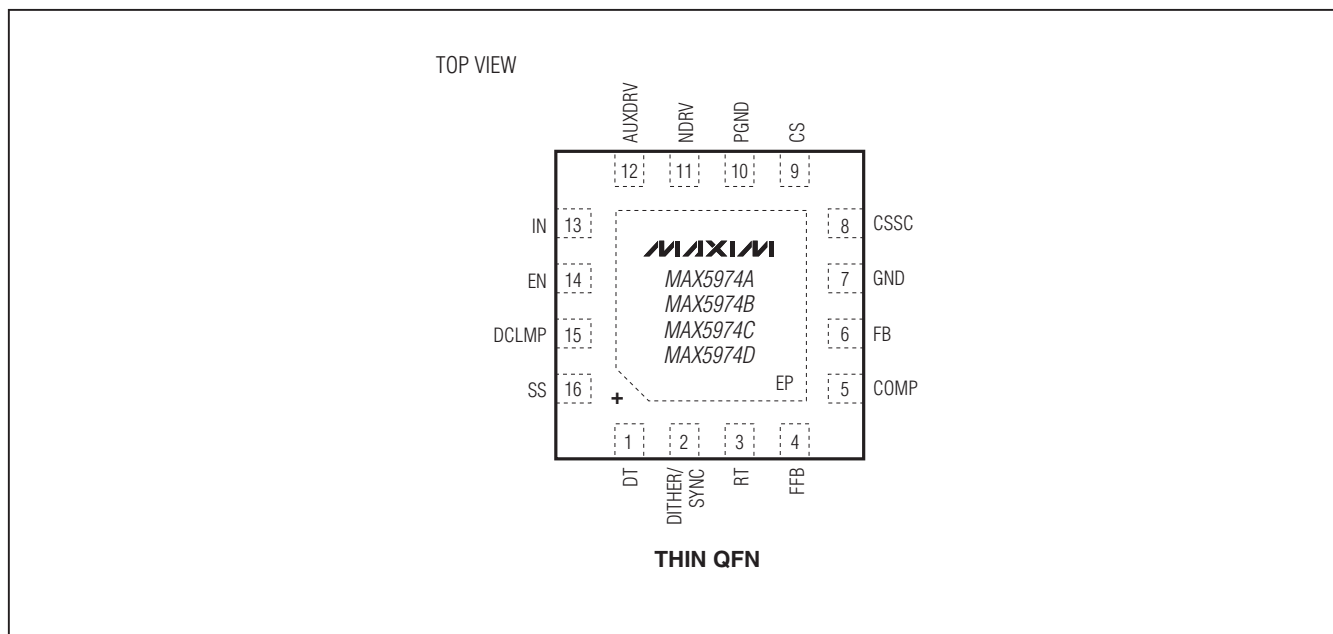
Typical Operating Characteristics (continued)

($V_{IN} = 12V$ (for MAX5974A/MAX5974C, bring V_{IN} up to 21V for startup), $V_{CS} = V_{CSSC} = V_{DITHER/SYNC} = V_{FB} = V_{FFB} = V_{DCLMP} = V_{GND}$, $V_{EN} = 2V$, $NDRV = AUXDRV = SS = COMP =$ unconnected, $R_{RT} = 34.8k\Omega$, $R_{DT} = 25k\Omega$, unless otherwise noted.)



Active-Clamped, Spread-Spectrum, Current-Mode PWM Controllers

Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	DT	Dead-Time Programming Resistor Connection. Connect resistor R_{DT} from DT to GND to set the desired dead time between the NDRV and AUXDRV signals. See the <i>Dead Time</i> section to calculate the resistor value for a particular dead time.
2	DITHER/ SYNC	Frequency Dithering Programming or Synchronization Connection. For spread-spectrum frequency operation, connect a capacitor from DITHER to GND and a resistor from DITHER to RT. To synchronize the internal oscillator to the externally applied frequency, connect DITHER/SYNC to the synchronization pulse.
3	RT	Switching Frequency Programming Resistor Connection. Connect resistor R_{RT} from RT to GND to set the PWM switching frequency. See the <i>Oscillator/Switching Frequency</i> section to calculate the resistor value for the desired oscillator frequency.
4	FFB	Frequency Foldback Threshold Programming Input. Connect a resistor from FFB to GND to set the output average current threshold below which the converter folds back the switching frequency to 1/2 of its original value. Connect to GND to disable frequency foldback.
5	COMP	Transconductance Amplifier Output and PWM Comparator Input. COMP is level shifted down and connected to the inverting input of the PWM comparator.

MAX5974A/MAX5974B/MAX5974C/MAX5974D

Active-Clamped, Spread-Spectrum, Current-Mode PWM Controllers

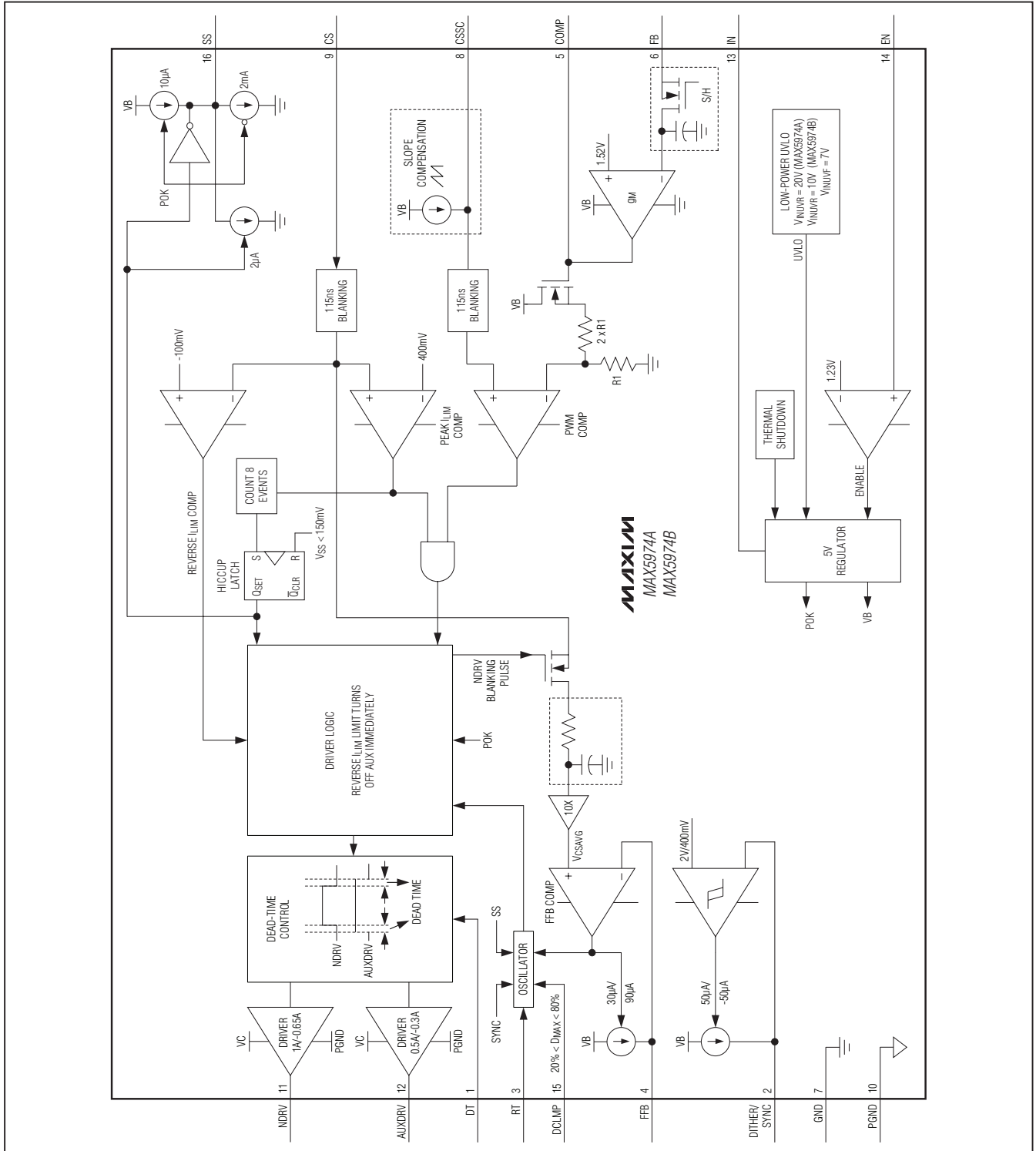
Pin Description (continued)

PIN	NAME	FUNCTION
6	FB	Transconductance Amplifier Inverting Input
7	GND	Signal Ground
8	CSSC	Current Sense with Slope Compensation Input. A resistor connected from CSSC to CS programs the amount of slope compensation. See the <i>Programmable Slope Compensation</i> section.
9	CS	Current-Sense Input. Current-sense connection for average current sense and cycle-by-cycle current limit. Peak current-limit trip voltage is 400mV and reverse current-limit trip voltage is -100mV.
10	PGND	Power Ground. PGND is the return path for gate-driver switching currents.
11	NDRV	Main Switch Gate-Driver Output
12	AUXDRV	pMOS Active Clamp Switch Gate-Driver Output. AUXDRV can also be used to drive a pulse transformer for synchronous flyback application.
13	IN	Converter Supply Input. IN has wide UVLO hysteresis, enabling the design of efficient power supplies. When the enable input EN is used to program a UVLO level for the power source, connect a zener diode between IN and PGND to ensure that V_{IN} is always clamped below its absolute maximum rating of 24V.
14	EN	Enable Input. The gate drivers are disabled and the device is in a low-power UVLO mode when the voltage on EN is below V_{ENF} . When the voltage on EN is above V_{ENR} , the device checks for other enable conditions. See the <i>Enable Input</i> section for more information about interfacing to EN.
15	DCLMP	Feed-Forward Maximum Duty-Cycle Clamp Programming Input. Connect a resistive divider between the input supply voltage DCLMP and GND. The voltage at DCLMP sets the maximum duty cycle (D_{MAX}) of the converter inversely proportional to the input supply voltage, so that the MOSFET remains protected during line transients.
16	SS	Soft-Start Programming Capacitor Connection. Connect a capacitor from SS to GND to program the soft-start period. This capacitor also determines hiccup mode current-limit restart time. A resistor from SS to GND can also be used to set the D_{MAX} below 75%.
—	EP	Exposed Pad. Internally connected to GND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

Active-Clamped, Spread-Spectrum, Current-Mode PWM Controllers

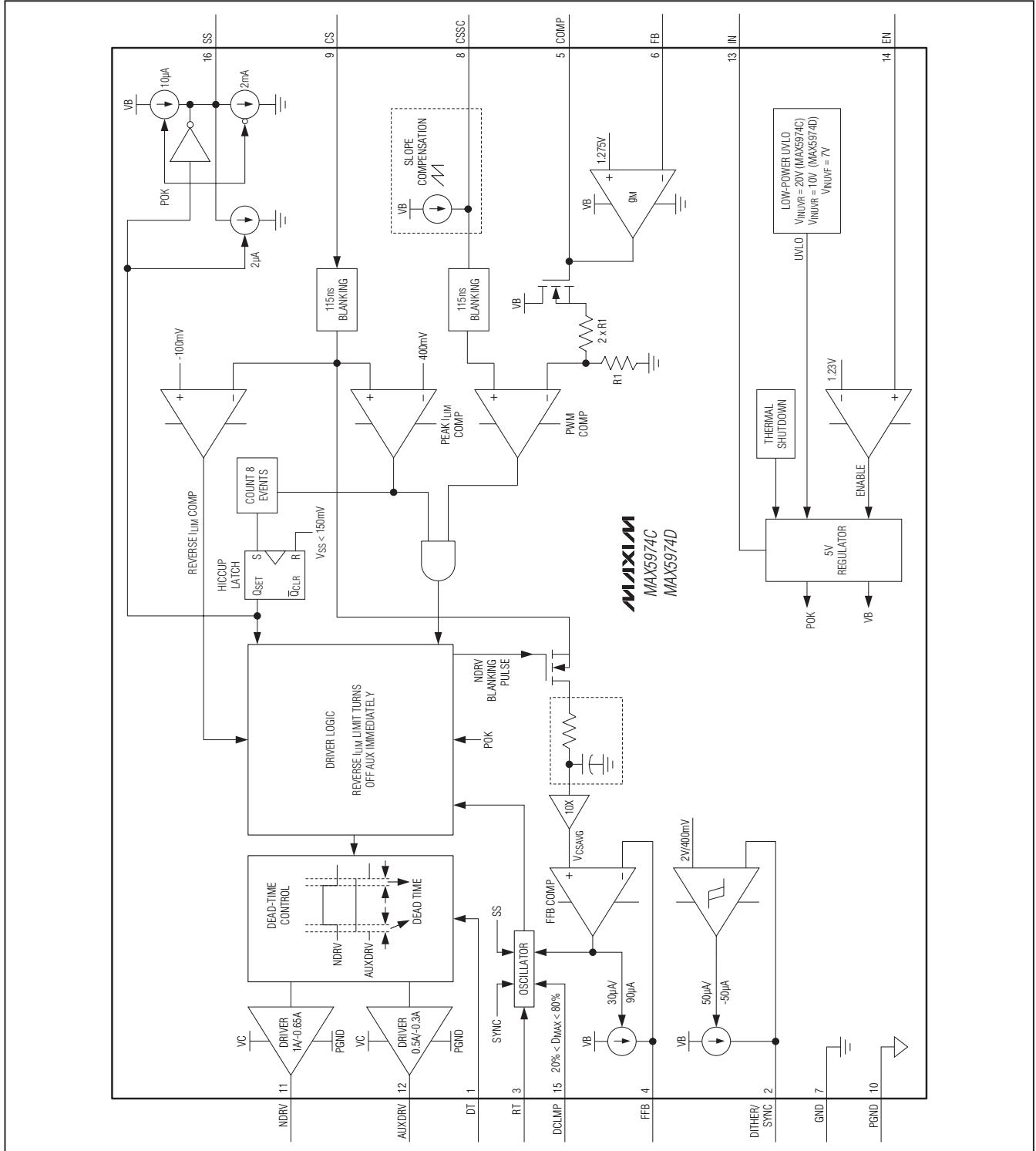
Block Diagrams

MAX5974A/MAX5974B/MAX5974C/MAX5974D



Active-Clamped, Spread-Spectrum, Current-Mode PWM Controllers

Block Diagrams (continued)



Active-Clamped, Spread-Spectrum, Current-Mode PWM Controllers

Detailed Description

The MAX5974A/MAX5974B/MAX5974C/MAX5974D are optimized for controlling a 25W to 50W active-clamped, self-driven synchronous rectification forward converter in continuous-conduction mode. The main switch gate driver (NDRV) and the active-clamped switch driver (AUXDRV) are sized to optimize efficiency for 25W design. The features-rich devices are ideal for PoE IEEE 802.3af/at-powered devices.

The MAX5974A/MAX5974C offer a 20V bootstrap UVLO wake-up level with a 13V wide hysteresis. The low startup and operating currents allow the use of a smaller storage capacitor at the input without compromising startup and hold times. The MAX5974A/MAX5974C are well-suited for universal input (rectified 85V AC to 265V AC) or telecom (-36V DC to -72V DC) power supplies.

The MAX5974B/MAX5974D have a UVLO rising threshold of 10V and can accommodate for low-input voltage (12V DC to 24V DC) power sources such as wall adapters.

Power supplies designed with the MAX5974A/MAX5974C use a high-value startup resistor, R_{IN} , that charges a reservoir capacitor, C_{IN} (see the *Typical Application Circuits*). During this initial period, while the voltage is less than the internal bootstrap UVLO threshold, the device typically consumes only 100 μ A of quiescent current. This low startup current and the large bootstrap UVLO hysteresis help to minimize the power dissipation across R_{IN} even at the high end of the universal AC input voltage (265V AC).

Feed-forward maximum duty-cycle clamping detects changes in line conditions and adjusts the maximum duty cycle accordingly to eliminate the clamp voltage's (i.e., the main power FET's drain voltage) dependence on the input voltage.

For EMI-sensitive applications, the programmable frequency dithering feature allows up to $\pm 10\%$ variation in the switching frequency. This spread-spectrum modulation technique spreads the energy of switching harmonics over a wider band while reducing their peaks, helping to meet stringent EMI goals.

The devices include a cycle-by-cycle current limit that turns off the main and AUX drivers whenever the internally set threshold of 400mV is exceeded. Eight consecutive occurrences of current-limit events trigger hiccup mode, which protects external components by halting switching for a period of time (t_{RSTRT}) and allowing the overload current to dissipate in the load and body diode of the synchronous rectifier before soft-start is reattempted.

The reverse current-limit feature of the devices turns the AUX driver off for the remaining off period when VCS exceeds the -100mV threshold. This protects the transformer core from saturation due to excess reverse current under some extreme transient conditions.

Current-Mode Control Loop

The advantages of current-mode control over voltage-mode control are twofold. First, there is the feed-forward characteristic brought on by the controller's ability to adjust for variations in the input voltage on a cycle-by-cycle basis. Second, the stability requirements of the current-mode controller are reduced to that of a single-pole system, unlike the double pole in voltage-mode control.

The devices use a current-mode control loop where the scaled output of the error amplifier (COMP) is compared to a slope-compensated current-sense signal at CSSC.

Enable Input

The enable input EN is used to enable or disable the device. Connect EN to IN for always enabled applications. Connecting EN to ground disables the device and reduces current consumption to 100 μ A.

The enable input has an accurate threshold of 1.26V (max). For applications that require a UVLO on the power source, connect a resistive divider from the power source to EN to GND as shown in Figure 1. A zener diode between IN and PGND is required to prevent IN from exceeding its absolute maximum rating of 24V when the device is disabled. The zener diode should be inactive below the maximum UVLO rising threshold voltage $V_{INUVR(MAX)}$ (21V for the MAX5974A/MAX5974C and 10.5V for the MAX5974B/MAX5974D). Design the resistive divider by first selecting the value of R_{EN1} to be on the order of 100k Ω . Then calculate R_{EN2} as follows:

$$R_{EN2} = R_{EN1} \frac{V_{EN(MAX)}}{V_{S(UVLO)} - V_{EN(MAX)}}$$

where $V_{EN(MAX)}$ is the maximum enable threshold voltage and is equal to 1.26V and $V_{S(UVLO)}$ is the desired UVLO threshold for the power source, below which the devices are disabled.

In the case where EN is externally controlled and UVLO for the power source is unnecessary, connect EN to IN and an open-drain or open-collector output as shown in Figure 2. The digital output connected to EN should be capable of withstanding IN's absolute maximum voltage of 24V.

Active-Clamped, Spread-Spectrum, Current-Mode PWM Controllers

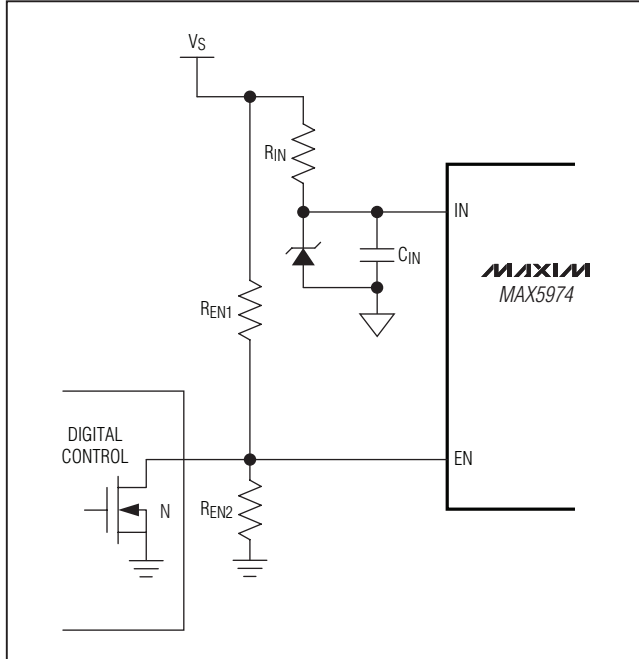


Figure 1. Programmable UVLO for the Power Source

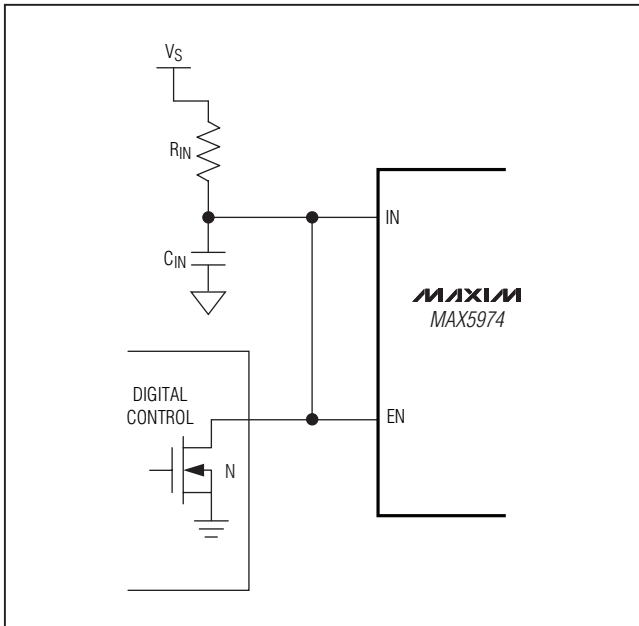


Figure 2. External Control of the Enable Input

Bootstrap Undervoltage Lockout

The devices have an internal bootstrap UVLO that is very useful when designing high-voltage power supplies (see the *Block Diagrams*). This allows the device to bootstrap itself during initial power-up. The MAX5974A/MAX5974C soft-start when V_{IN} exceeds the bootstrap UVLO threshold of V_{INUVR} (20V typ).

Because the MAX5974B/MAX5974D are designed for use with low-voltage power sources such as wall adapters outputting 12V to 24V, they have a lower UVLO wake-up threshold of 10V.

Startup Operation

The device starts up when the voltage at IN exceeds 20V (MAX5974A/MAX5974C) or 10V (MAX5974B/MAX5974D) and the enable input voltage is greater than 1.26V.

During normal operation, the voltage at IN is normally derived from a tertiary winding of the transformer (MAX5974C/MAX5974D). However, at startup there is no energy being delivered through the transformer; hence, a special bootstrap sequence is required. In the *Typical Application Circuits*, C_{IN} charges through the startup resistor, R_{IN} , to an intermediate voltage. Only 100 μ A of the current supplied through R_{IN} is used by the ICs, the remaining input current charges C_{IN} until V_{IN} reaches the bootstrap UVLO wake-up level. Once V_{IN} exceeds this level, NDRV begins switching the n-channel MOSFET and transfers energy to the secondary and tertiary outputs. If the voltage on the tertiary output builds to higher than 7V (the bootstrap UVLO shutdown level), then startup has been accomplished and sustained operation commences. If V_{IN} drops below 7V before startup is complete, the device goes back to low-current UVLO. In this case, increase the value of C_{IN} in order to store enough energy to allow for the voltage at the tertiary winding to build up.

While the MAX5974A/MAX5974B derive their input voltage from the coupled inductor output during normal operation, the startup behavior is similar to that of the MAX5974C/MAX5974D.

Soft-Start

A capacitor from SS to GND, C_{SS} , programs the soft-start time. V_{SS} controls the oscillator duty cycle during

Active-Clamped, Spread-Spectrum, Current-Mode PWM Controllers

startup to provide a slow and smooth increase of the duty cycle to its steady-state value. Calculate the value of C_{SS} as follows:

$$C_{SS} = \frac{I_{SS-CH} \times t_{ss}}{2V}$$

where I_{SS-CH} (10 μ A typ) is the current charging C_{SS} during soft-start and t_{ss} is the programmed soft-start time.

A resistor can also be added from the SS pin to GND to clamp $V_{SS} < 2V$ and, hence, program the maximum duty cycle to be less than 80% (see the *Duty-Cycle Clamping* section).

n-Channel MOSFET Gate Driver

The NDRV output drives an external n-channel MOSFET. NDRV can source/sink in excess of 650mA/1000mA peak current; therefore, select a MOSFET that yields acceptable conduction and switching losses. The external MOSFET used must be able to withstand the maximum clamp voltage.

p-Channel MOSFET Gate Driver

The AUXDRV output drives an external p-channel MOSFET with the aid of a level shifter. The level shifter consists of C_{AUX} , R_{AUX} , and D5 as shown in the *Typical Application Circuits*. When AUXDRV is high, C_{AUX} is recharged through D5. When AUXDRV is low, the gate of the p-channel MOSFET is pulled below the source by the voltage stored on C_{AUX} , turning on the pFET.

Dead Time

Dead time between the main and AUX output edges allow ZVS to occur, minimizing conduction losses and improving efficiency. The dead time (t_{DT}) is applied to both leading and trailing edges of the main and AUX outputs as shown in Figure 3. Connect a resistor between DT and GND to set t_{DT} to any value between 40ns and 400ns:

$$R_{DT} = \frac{10k\Omega}{40ns} \times t_{DT}$$

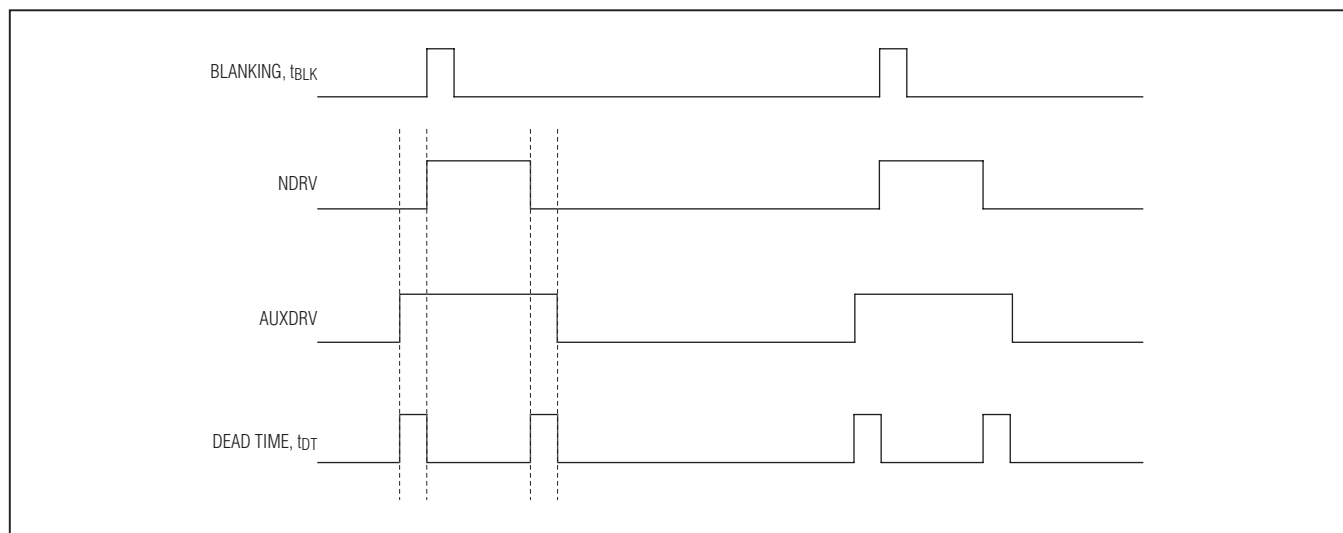


Figure 3. Dead Time Between AUXDRV and NDRV

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Oscillator/Switching Frequency

The ICs' switching frequency is programmable between 100kHz and 600kHz with a resistor R_{RT} connected between RT and GND. Use the following formula to determine the appropriate value of R_{RT} needed to generate the desired output-switching frequency (f_{SW}):

$$R_{RT} = \frac{8.7 \times 10^9}{f_{SW}}$$

where f_{SW} is the desired switching frequency.

Peak Current Limit

The current-sense resistor (R_{CS} in the *Typical Application Circuits*), connected between the source of the n-channel MOSFET and PGND, sets the current limit. The current-limit comparator has a voltage trip level ($V_{CS-PEAK}$) of 400mV. Use the following equation to calculate the value of R_{CS} :

$$R_{CS} = \frac{400\text{mV}}{I_{PRI}}$$

where I_{PRI} is the peak current in the primary side of the transformer, which also flows through the MOSFET. When the voltage produced by this current (through the current-sense resistor) exceeds the current-limit comparator threshold, the MOSFET driver (NDRV) terminates the current on-cycle, within 35ns (typ).

The devices implement 115ns of leading-edge blanking to ignore leading-edge current spikes. These spikes are caused by reflected secondary currents, current-

discharging capacitance at the FET's drain, and gate-charging current. Use a small RC network for additional filtering of the leading-edge spike on the sense waveform when needed. Set the corner frequency between 10MHz and 20MHz.

After the leading-edge blanking time, the device monitors V_{CS} for any breaches of the peak current limit of 400mV. The duty cycle is terminated immediately when V_{CS} exceeds 400mV.

Reverse Current Limit

The devices protect the transformer against saturation due to reverse current by monitoring the voltage across R_{CS} while the AUX output is low and the p-channel FET is on.

Output Short-Circuit Protection with Hiccup Mode

When the device detects eight consecutive peak current-limit events, both NDRV and AUXDRV driver outputs are turned off for a restart period, t_{RSTRT} . After t_{RSTRT} , the device undergoes soft-start. The duration of the restart period depends on the value of the capacitor at SS (C_{SS}). During this period, C_{SS} is discharged with a pulldown current of I_{SS-DH} ($2\mu\text{A}$ typ). Once its voltage reaches 0.15V, the restart period ends and the device initiates a soft-start sequence. An internal counter ensures that the minimum restart period ($t_{RSTRT-MIN}$) is 1024 clock cycles when the time required for C_{SS} to discharge to 0.15V is less than 1024 clock cycles. Figure 4 shows the behavior of the device prior and during hiccup mode.

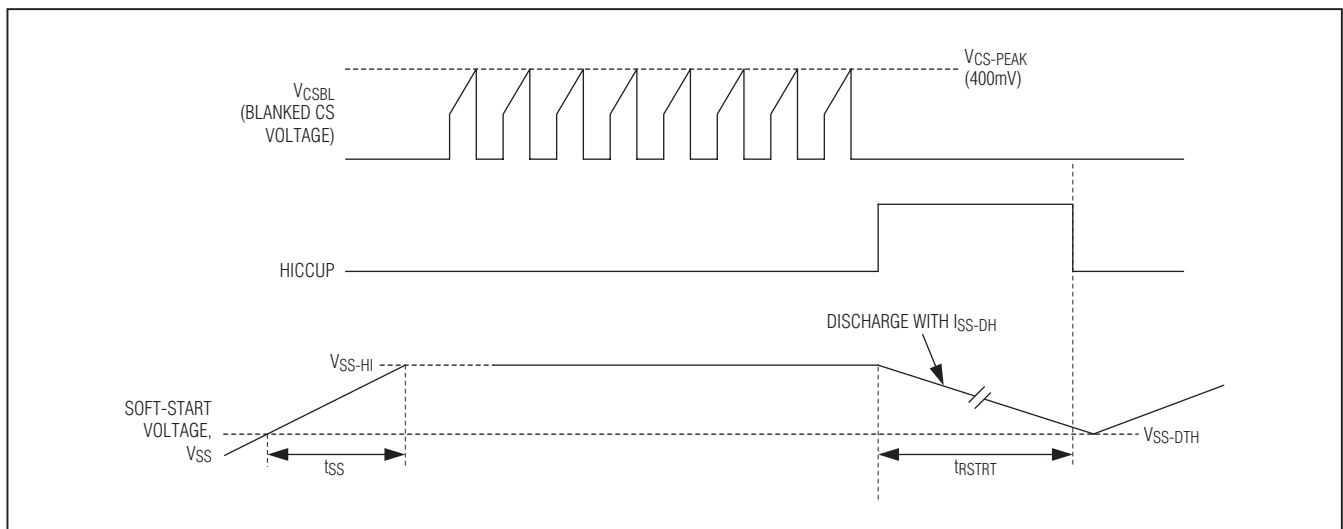


Figure 4. Hiccup Mode Timing Diagram

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Frequency Foldback for High-Efficiency Light-Load Operation

The frequency foldback threshold can be programmed from 0 to 20% of the full load current using a resistor from FFB to GND.

The CS voltage is sampled during the NDRV on-time, averaged using an internal RC filter, and gained up by 10 to generate a voltage, VCSAVG. When VCSAVG falls below VFFB, the device folds back the switching frequency to 1/2 the original value to reduce switching losses and increase the converter efficiency. The new switching frequency starts at the beginning of a new cycle as shown in Figure 5. Calculate the value of RFFB as follows:

$$R_{FFB} = \frac{10 \times I_{LOAD(LIGHT)} \times R_{CS}}{I_{FFB}}$$

where RFFB is the resistor between FFB and GND, I_{LOAD(LIGHT)} is the current at light-load conditions that triggers frequency foldback, RCS is the value of the sense resistor connected between CS and PGND, and I_{FFB} is the current sourced from FFB to RFFB (30µA typ).

Duty-Cycle Clamping

The maximum duty cycle is determined by the lowest of three voltages: 2V, the voltage at SS (V_{SS}), and the voltage (2.43V - VDCLMP). The maximum duty cycle is calculated as:

$$D_{MAX} = \frac{V_{MIN}}{2.43V}$$

where V_{MIN} = minimum (2V, V_{SS}, 2.43V - VDCLMP).

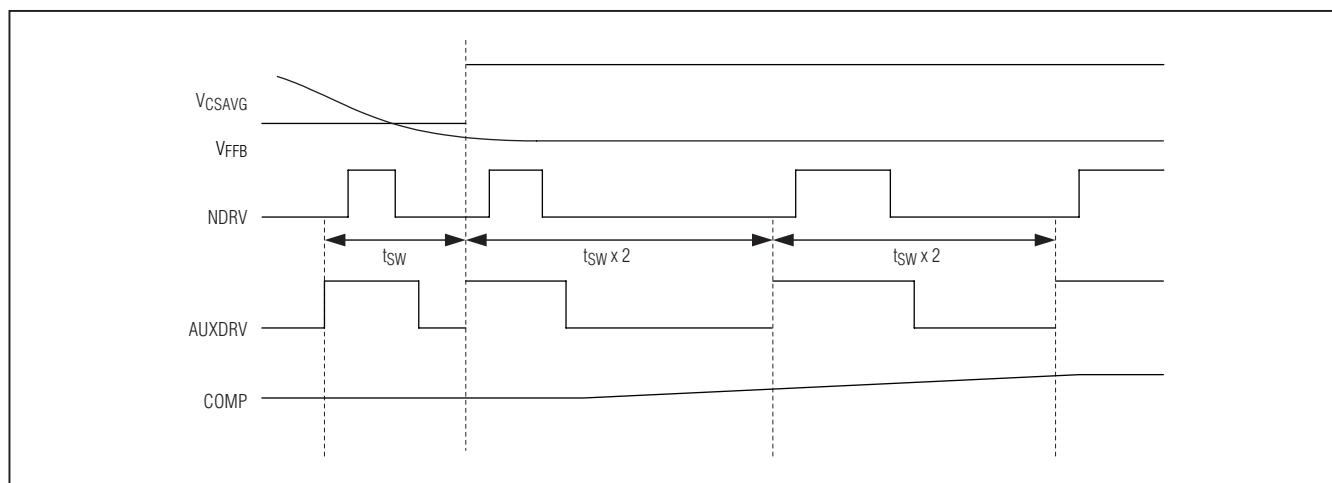


Figure 5. Entering Frequency Foldback

SS

By connecting a resistor between SS and ground, the voltage at SS can be made to be lower than 2V. V_{SS} is calculated as follows:

$$V_{SS} = R_{SS} \times I_{SS-CH}$$

where R_{SS} is the resistor connected between SS and GND, and I_{SS-CH} is the current sourced from SS to R_{SS} (10µA typ).

DCLMP

To set D_{MAX} using supply voltage feed-forward, connect a resistive divider between the supply voltage, DCLMP, and GND as shown in the *Typical Application Circuits*. This feed-forward duty-cycle clamp ensures that the external n-channel MOSFET is not stressed during supply transients. V_{DCLMP} is calculated as follows:

$$V_{DCLMP} = \frac{R_{DCLMP2}}{R_{DCLMP1} + R_{DCLMP2}} \times V_S$$

where RDCLMP1 and RDCLMP2 are the resistive divider values shown in the *Typical Application Circuits* and V_S is the input supply voltage.

Oscillator Synchronization

The internal oscillator can be synchronized to an external clock by applying the clock to DITHER/SYNC directly. The external clock frequency can be set anywhere between 1.1x to 2x the internal clock frequency.

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Using an external clock increases the maximum duty cycle by a factor equal to $f_{\text{SYNC}}/f_{\text{SW}}$. This factor should be accounted for in setting the maximum duty cycle using any of the methods described in the *Duty-Cycle Clamping* section. The formula below shows how the maximum duty cycle is affected by the external clock frequency:

$$D_{\text{MAX}} = \frac{V_{\text{MIN}}}{2.43\text{V}} \times \frac{f_{\text{SYNC}}}{f_{\text{SW}}}$$

where V_{MIN} is described in the *Duty-Cycle Clamping* section, f_{SW} is the switching frequency as set by the resistor connected between RT and GND, and f_{SYNC} is the external clock frequency.

Frequency Dithering for Spread-Spectrum Applications (Low EMI)

The switching frequency of the converter can be dithered in a range of $\pm 10\%$ by connecting a capacitor from DITHER/SYNC to GND, and a resistor from DITHER to RT as shown in the *Typical Application Circuits*. This results in lower EMI.

A current source at DITHER/SYNC charges the capacitor C_{DITHER} to 2V at $50\mu\text{A}$. Upon reaching this trip point, it discharges C_{DITHER} to 0.4V at $50\mu\text{A}$. The charging and discharging of the capacitor generates a triangular waveform on DITHER/SYNC with peak levels at 0.4V and 2V and a frequency that is equal to:

$$f_{\text{TRI}} = \frac{50\mu\text{A}}{C_{\text{DITHER}} \times 3.2\text{V}}$$

Typically, f_{TRI} should be set close to 1kHz. The resistor R_{DITHER} connected from DITHER/SYNC to RT determines the amount of dither as follows:

$$\% \text{DITHER} = \frac{4}{3} \times \frac{R_{\text{RT}}}{R_{\text{DITHER}}}$$

where $\% \text{DITHER}$ is the amount of dither expressed as a percentage of the switching frequency. Setting R_{DITHER} to $10 \times R_{\text{RT}}$ generates $\pm 10\%$ dither.

Programmable Slope Compensation

The device generates a current ramp at CSSC such that its peak is $50\mu\text{A}$ at 80% duty cycle of the oscillator. An external resistor connected from CSSC to the CS then converts this current ramp into programmable slope-

compensation amplitude, which is added to the current-sense signal for stability of the peak current-mode control loop. The ramp rate of the slope compensation signal is given by:

$$m = \frac{R_{\text{CSSC}} \times 50\mu\text{A} \times f_{\text{SW}}}{80\%}$$

where m is the ramp rate of the slope-compensation signal, R_{CSSC} is the value of the resistor connected between CSSC and CS used to program the ramp rate, and f_{SW} is the switching frequency.

Error Amplifier

The MAX5974A/MAX5974B include an internal error amplifier with a sample-and-hold input. The feedback input of the MAX5974C/MAX5974D is continuously connected. The noninverting input of the error amplifier is connected to the internal reference and feedback is provided at the inverting input. High open-loop gain and unity-gain bandwidth allow good closed-loop bandwidth and transient response. Calculate the power-supply output voltage using the following equation:

$$V_{\text{OUT}} = V_{\text{REF}} \times \frac{R_{\text{FB1}} + R_{\text{FB2}}}{R_{\text{FB2}}}$$

where $V_{\text{REF}} = 1.52\text{V}$ for the MAX5974A/MAX5974B and $V_{\text{REF}} = 1.215\text{V}$ for the MAX5974C/MAX5974D. The amplifier's noninverting input is internally connected to a soft-start circuit that gradually increases the reference voltage during startup. This forces the output voltage to come up in an orderly and well-defined manner under all load conditions.

Applications Information

Startup Time Considerations

The bypass capacitor at IN, C_{IN} , supplies current immediately after the devices wake up (see the *Typical Application Circuits*). Large values of C_{IN} increase the startup time, but also supply gate charge for more cycles during initial startup. If the value of C_{IN} is too small, V_{IN} drops below 7V because NDRV does not have enough time to switch and build up sufficient voltage across the tertiary output (MAX5974C/MAX5974D) or coupled inductor output (MAX5974A/MAX5974B), which powers the device. The device goes back into UVLO and does not start. Use a low-leakage capacitor for C_{IN} .

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Typically, offline power supplies keep startup times to less than 500ms even in low-line conditions (85V AC input for universal offline or 36V DC for telecom applications). Size the startup resistor, R_{IN} , to supply both the maximum startup bias of the device (100 μ A) and the charging current for C_{IN} . C_{IN} must be charged to 20V within the desired 500ms time period. C_{IN} must store enough charge to deliver current to the device for at least the soft-start time (t_{SS}) set by C_{SS} . To calculate the approximate amount of capacitance required, use the following formula:

$$I_G = Q_{GTOT}f_{SW}$$

$$C_{IN} = \frac{(I_{IN} + I_G)(t_{SS})}{V_{HYST}}$$

where I_{IN} is the ICs' internal supply current (1.8mA) after startup, Q_{GTOT} is the total gate charge for the n-channel and p-channel FETs, f_{SW} is the ICs' switching frequency, V_{HYST} is the bootstrap UVLO hysteresis (13V typ), and t_{SS} is the soft-start time. R_{IN} is then calculated as follows:

$$R_{IN} \cong \frac{V_{S(MIN)} - V_{INUVR}}{I_{START}}$$

where $V_{S(MIN)}$ is the minimum input supply voltage for the application (36V for telecom), V_{INUVR} is the bootstrap UVLO wake-up level (20V), and I_{START} is the IN supply current at startup (150 μ A max).

Choose a higher value for R_{IN} than the one calculated above if a longer startup time can be tolerated in order to minimize power loss on this resistor.

Active Clamp Circuit

Traditional clamp circuits prevent transformer saturation by channeling the magnetizing current (I_M) of the transformer onto a dissipative RC network. To improve efficiency, the active clamp circuit recycles I_M between the magnetizing inductance and clamp capacitor. V_{CLAMP} is given by:

$$V_{CLAMP} = \frac{V_S}{1-D}$$

where V_S is the voltage of the power source and D is the duty cycle. To select n-channel and p-channel FETs

with adequate breakdown voltages, use the maximum value of V_{CLAMP} . $V_{CLAMP(MAX)}$ occurs when the input voltage is at its minimum and the duty cycle is at its maximum. $V_{CLAMP(MAX-NORMAL)}$ during normal operation is therefore:

$$V_{CLAMP(MAX-NORMAL)} = \frac{V_{S(MIN)}}{1 - \frac{N_P \times V_O}{N_S \times V_{S(MIN)}}}$$

where $V_{S(MIN)}$ is the minimum voltage of the power source, N_P/N_S is the primary to secondary turns ratio, and V_O is the output voltage. The clamp capacitor, n-channel, and p-channel FETs must have breakdown voltages exceeding this level.

If feed-forward maximum duty-cycle clamp is used then:

$$D_{MAX-FF} = \frac{V_{MIN}}{2.43} = \left(1 - \frac{V_{DCLMP}}{2.43}\right)$$

$$= \left(1 - \frac{V_S}{2.43} \times \frac{R_{DCLMP2}}{R_{DCLMP1} + R_{DCLMP2}}\right)$$

Therefore, $V_{CLAMP(MAX-FF)}$ during feed-forward maximum duty clamp is:

$$V_{CLAMP(MAX-FF)} = \frac{V_S}{1 - D_{MAX-FF}}$$

$$= \frac{2.43 \times (R_{DCLMP1} + R_{DCLMP2})}{R_{DCLMP2}}$$

The AUX driver controls the p-channel FET through a level shifter. The level shifter consists of an RC network (formed by C_{AUX} and R_{AUX}) and diode D5, as shown in the *Typical Application Circuits*. Choose R_{AUX} and C_{AUX} so that the time constant exceeds 100/ f_{SW} . Diode D5 is a small-signal diode with a voltage rating exceeding 25V.

Additionally, C_{CLAMP} should be chosen such that the complex poles formed with magnetizing inductance (L_{MAG}) and C_{CLAMP} are 2x to 4x away from the loop bandwidth:

$$\frac{1-D}{2\pi\sqrt{L_{MAG} \times C_{CLAMP}}} > 3 \times f_{BW}$$

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Bias Circuit

Optocoupler Feedback (MAX5974C/MAX5974D)

An in-phase tertiary winding is needed to power the bias circuit when using optocoupler feedback. The voltage across the tertiary V_T during the on-time is:

$$V_T = V_{OUT} \times \frac{N_T}{N_S}$$

where V_{OUT} is the output voltage and N_T/N_S is the turns ratio from the tertiary to the secondary winding. Select the turns ratio so that V_T is above the UVLO shutdown level (7.5V max) by a margin determined by the holdup time needed to “ride through” a brownout.

Coupled-Inductor Feedback (MAX5974A/MAX5974B)

When using coupled-inductor feedback, the power for the devices can be taken from the coupled inductor during the off-time. The voltage across the coupled inductor, $V_{COUPLED}$, during the off-time is:

$$V_{COUPLED} = V_{OUT} \times \frac{N_C}{N_O}$$

where V_{OUT} is the output voltage and N_C/N_O is the turns ratio from the coupled output to the main output winding. Select the turns ratio so that $V_{COUPLED}$ is above the UVLO shutdown level (7.5V max) by a margin determined by the holdup time needed to “ride through” a brownout.

This voltage appears at the input of the devices, less a diode drop. An RC network consisting of R_{SNUB} and C_{SNUB} is for damping the reverse recovery transients of diode D6.

During on-time, the coupled output is:

$$V_{COUPLED-ON} = -(V_S \times \frac{N_S}{N_P} - V_{OUT}) \frac{N_C}{N_O}$$

where V_S is the input supply voltage.

Care must be taken to ensure that the voltage at FB (equal to $V_{COUPLED-ON}$ attenuated by the feedback resistive divider) is not more than 5V:

$$V_{FB-ON} = V_{COUPLED-ON} \times \frac{R_{FB2}}{(R_{FB1} + R_{FB2})} < 5V$$

If this condition is not met, a signal diode should be placed from GND (anode) to FB (cathode).

Layout Recommendations

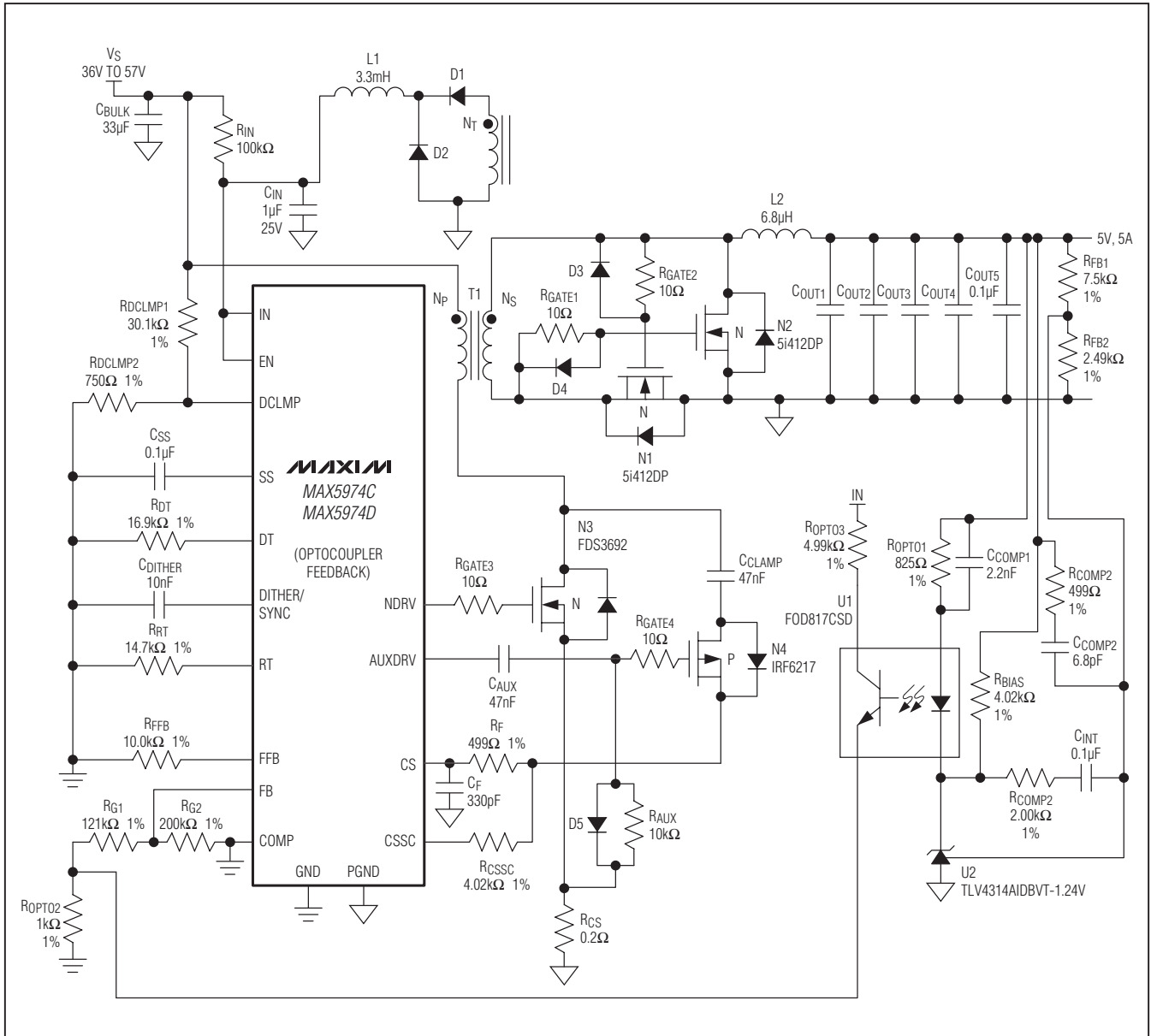
Typically, there are two sources of noise emission in a switching power supply: high di/dt loops and high dV/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly, the heatsink of the main MOSFET presents a dV/dt source; therefore, minimize the surface area of the MOSFET heatsink as much as possible. Keep all PCB traces carrying switching currents as short as possible to minimize current loops. Use a ground plane for best results.

For universal AC input design, follow all applicable safety regulations. Offline power supplies can require UL, VDE, and other similar agency approvals.

Active-Clamped, Spread-Spectrum, Current-Mode PWM Controllers

Typical Application Circuits

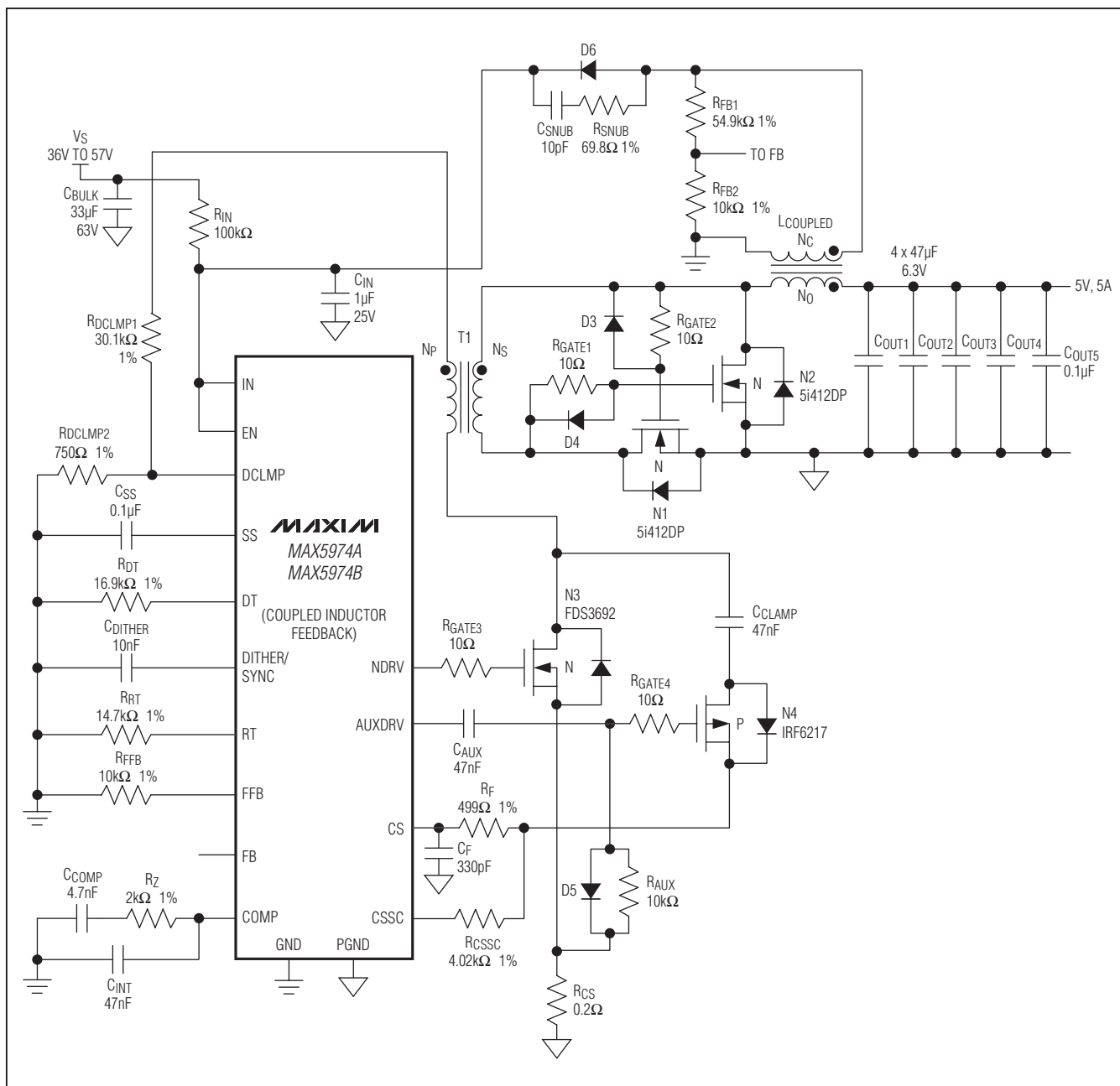
MAX5974A/MAX5974B/MAX5974C/MAX5974D



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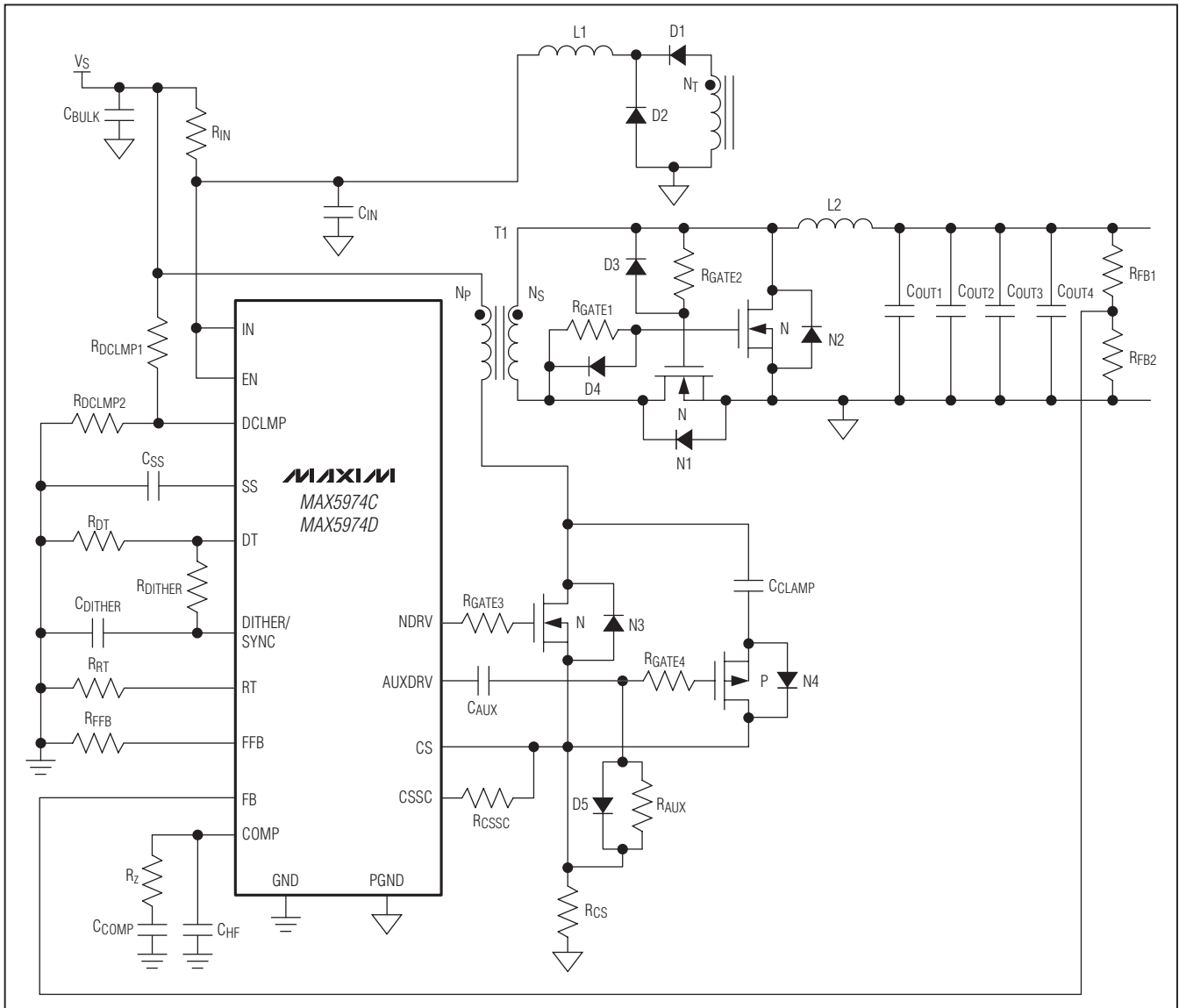
Typical Application Circuits (continued)

MAX5974A/MAX5974B/MAX5974C/MAX5974D



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Typical Application Circuits (continued)



MAX5974A/MAX5974B/MAX5974C/MAX5974D

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1633+4	21-0136	90-0031

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/10	Initial release	—

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