SY54016R

Low Voltage 1.2V/1.8V CML Differential Line Driver/Receiver with Fail Safe Input 3.2Gbps, 2.5GHz

Precision Edge®

General Description

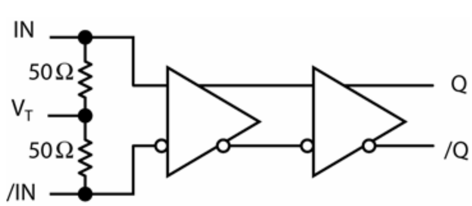
The SY54016R is a fully differential, low voltage 1.2V/1.8V CML Line Driver/Receiver with Fail-Safe Input. The SY54016R can process clock signals as fast as 2.5GHz or data patterns up to 3.2Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals, as small as 100mV ($200mV_{PP}$) without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an internal voltage reference is provided to bias the V_T pin. The outputs are CML, with extremely fast rise/fall times guaranteed to be less than 95ps.

The SY54016R operates from a 2.5V ±5% core supply and a 1.8V or 1.2V ±5% output supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). The SY54016R is part of Micrel's high-speed, Precision Edge® product line.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Functional Block Diagram



Features

- 1.2V/1.8V CML Line Driver/Receiver with Fail-Safe Input
- Guaranteed AC performance over temperature and voltage:
  - DC-to- > 3.2Gbps throughput
  - <370ps propagation delay (IN-to-Q)
  - <95ps rise/fall times
- Ultra-low jitter design
  - $<1ps_{RMS}$ cycle-to-cycle jitter
  - $<10ps_{PP}$ total jitter
  - $<1ps_{RMS}$ random jitter
  - $<10ps_{PP}$ deterministic jitter
- High-speed CML outputs
- 2.5V ±5% , 1.8/1.2V ±5% power supply operation
- Industrial temperature range: –40°C to +85°C
- Available in 8-pin (2mm x 2mm) MLF® package

Applications

- Data Distribution: OC-48, OC-48+FEC
- SONET clock and data distribution
- Fibre Channel clock and data distribution
- Gigabit Ethernet clock and data distribution

Markets

- Storage
- ATE
- Test and measurement
- Enterprise networking equipment
- High-end servers
- Metro area network equipment

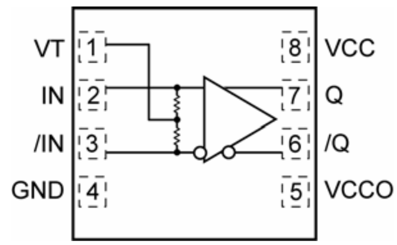
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY54016RMGTR[2]	MLF-8	Industrial	016R with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



8-Pin MLF® (MLF-8)

Pin Description

Pin Number	Pin Name	Pin Function
2,3	IN, /IN	Differential Input: This input pair is the differential signal input to the device. Input accepts differential signals as small as 100mV (200mV$_{PP}$). Each input pin internally terminates with 50Ω to the VT pin. If the input swing falls below a certain threshold (typical 30mV), the Fail Safe Input (FSI) feature will guarantee a stable output by latching the output to its last valid state.
1	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to VT pin. This pin provides a center-tap to a termination network for maximum interface flexibility. An internal high impedance resistor divider biases VT to allow input AC coupling. For AC-coupling, bypass VT with 0.1µF low ESR capacitor to VCC. See “Interface Applications” subsection and Figure 2a.
8	VCC	Positive Power Supply: Bypass with 0.1uF//0.01uF low ESR capacitors as close to the V_{CC} pin as possible. Supplies input and core circuitry.
5	VCCO	Output Supply: Bypass with 0.1uF//0.01uF low ESR capacitors as close to the V_{CCO} pin as possible. Supplies the output buffer.
4	GND, Exposed pad	Ground: Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
7,6	Q, /Q	CML Differential Output Pair: Differential buffered copy of the input signal. The output swing is typically 390mV. See “Interface Applications” subsection for termination information.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) .... –0.5V to +3.0V
Supply Voltage (V_{CCO}) .... –0.5V to +2.7V
V_{CC} - V_{CCO} .... <1.8V
V_{CCO} - V_{CC} .... <0.5V
Input Voltage (V_{IN}) .... –0.5V to V_{CC}
CML Output Voltage (V_{OUT}) .... 0.6V to V_{CCO}+0.5V
Current (V_T)
  Source or sink current on VT pin .... ±100mA
Input Current
  Source or sink current on (IN, /IN) .... ±50mA
Maximum operating Junction Temperature .... 125°C
Lead Temperature (soldering, 20sec.) .... 260°C
Storage Temperature (T_s) .... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) .... 2.375V to 2.625V
  (V_{CCO}) .... 1.14V to 1.9V
Ambient Temperature (T_A) .... –40°C to +85°C
Package Thermal Resistance[3]
  MLF®
    Still-air ($\square_{JA}$) .... 93°C/W
    Junction-to-board ($\square_{JB}$) .... 56°C/W

DC Electrical Characteristics[4]

T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage Range	V_{CC} V_{CCO} V_{CCO}	2.375 1.14 1.7	2.5 1.2 1.8	2.625 1.26 1.9	V V V
I_{CC}	Power Supply Current	Max. V_{CC}		13	19	mA
I_{CCO}	Power Supply Current	No Load. Max. V_{CCO}		16	21	mA
R_{IN}	Input Resistance (IN-to-V_T, /IN-to-V_T)		45	50	55	Ω
R_{DIFF_IN}	Differential Input Resistance (IN-to-/IN)		90	100	110	Ω
V_{IH}	Input HIGH Voltage (IN, /IN)	IN, /IN	1.2		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)	V_{IL} with V_{IH} = 1.2V	0.2		V_{IH}–0.1	V
V_{IH}	Input HIGH Voltage (IN, /IN)	IN, /IN	1.14		V_{CC}	V
V_{IL}	Input LOW Voltage (IN, /IN)	V_{IL} with V_{IH} = 1.14V, (1.2V-5%)	0.66		V_{IH}–0.1	V
V_{IN}	Input Voltage Swing (IN, /IN)	see Figure 3a	0.1		1.0	V
V_{DIFF_IN}	Differential Input Voltage Swing (|IN - /IN|)	see Figure 3b	0.2		2.0	V
V_{IN_FSI}	Input Voltage Threshold that Triggers FSI			30	100	mV
V_{T_IN}	Voltage from Input to V_T				1.28	V

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

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CML Outputs DC Electrical Characteristics[5]

V_{CCO} = 1.14V to 1.26V R_L = 50Ω to V_{CCO},
V_{CCO} = 1.7V to 1.9V, R_L = 50Ω to V_{CCO} or 100Ω across the outputs,
V_{CC} = 2.375V to 2.625V. T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	R_L = 50Ω to V_{CCO}	V_{CCO}-0.020	V_{CCO}-0.010	V_{CCO}	V
V_{OUT}	Output Voltage Swing	See Figure 3a	300	390	475	mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 3b	600	780	950	mV
R_{OUT}	Output Source Impedance		45	50	55	Ω

Note:

5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics

V_{CCO} = 1.14V to 1.26V R_L = 50Ω to V_{CCO},
V_{CCO} = 1.7V to 1.9V, R_L = 50Ω to V_{CCO} or 100Ω across the outputs,
V_{CC} = 2.375V to 2.625V. T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Frequency	NRZ Data	3.2			Gbps
		V_{OUT} > 200mV Clock	2.5			GHz
t_{PD}	Propagation Delay IN-to-Q	V_{IN}: 100mV-200mV, Note 6, Figure 1a	180	300	420	ps
		V_{IN}: >200mV, Note 6, Figure 1a	170	250	370	ps
t_{Skew}	Part-to-Part Skew	Note 7			75	ps
t_{Jitter}	Data Random Jitter	Note 8			1	ps_{RMS}
	Deterministic Jitter	Note 9			10	ps_{PP}
	Clock Cycle-to-Cycle Jitter	Note 10			1	ps_{RMS}
	Total Jitter	Note 11			10	ps_{PP}
t_R t_F	Output Rise/Fall Times (20% to 80%)	At full output swing.	30	60	95	ps
	Duty Cycle	Differential I/O	47		53	%

Notes:

6. Propagation delay is measured with input t_r/t_f ≤300ps (20% to 80%).
7. Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs. V_{IN} >200mV with input t_r/t_f ≤300ps (20% to 80%).
8. Random jitter is measured with a K28.7 pattern, measured at ≤ f_{MAX}.
9. Deterministic jitter is measured at 2.5Gbps with both K28.5 and 2^{23}–1 PRBS pattern.
10. Cycle-to-cycle jitter definition: the variation period between adjacent cycles over a random sample of adjacent cycle pairs. $t_{JITTER\_CC} = T_n - T_{n+1}$, where T is the time between rising edges of the output signal.
11. Total jitter definition: with an ideal clock input frequency of ≤ f_{MAX} (device), no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

Functional Description

Fail-Safe Input (FSI)

The input includes a special failsafe circuit to sense the amplitude of the input signal and to latch the output when there is no input signal present, or when the amplitude of the input signal drops sufficiently below $100mV_{PK}$ ($200mV_{PP}$), typically $30mV_{PK}$. Maximum frequency of the SY54016R is limited by the FSI function.

Input Clock Failure Case

If the input clock fails to a floating, static, or extremely low signal swing, the FSI function will eliminate a metastable condition and guarantee a stable output. No ringing and no undetermined state will occur at the output under these conditions.

Note that the FSI function will not prevent duty cycle distortion in case of a slowly deteriorating (but still toggling) input signal close to the FSI threshold. Due to the FSI function, the propagation delay will depend on rise and fall time of the input signal and on its amplitude. Refer to "Typical Characteristics" for detailed information

Interface Applications

For Input Interface Applications see Figures 4a-f and for CML Output Termination see Figures 5a-d.

CML Output Termination with VCCO 1.2V

For VCCO of 1.2V, Figure 5a, terminate the output with 50Ω-to-1.2V, DC-coupled, not 100Ω differentially across the outputs.

If AC-coupling is used, Figure 5d, terminate into 50Ω-to-1.2V before the coupling capacitor and then connect to a high value resistor to a reference voltage.

Do not AC couple with internally terminated receiver. For example, 50Ω ANY-IN input. AC-coupling will offset the output voltage by 200mV and this offset voltage will be too low for proper driver operation.

CML Output Termination with VCCO 1.8V

For VCCO of 1.8V, Figure 5a and Figure b, terminate with either 50Ω to 1.8V or 100Ω differentially across the outputs. AC- or DC-coupling is fine.

Input AC-Coupling

The SY54016R input can accept AC-coupling from any driver. Tie VT to VCC with a capacitor as shown in Figures 4c and 4d. VT has an internal high impedance resistor divider as shown in Figure 2a, to provide a bias voltage for AC-coupling.

Timing Diagrams

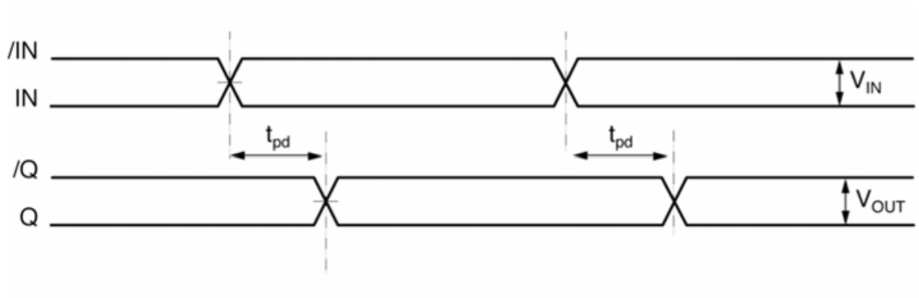


Figure 1a. Propagation Delay

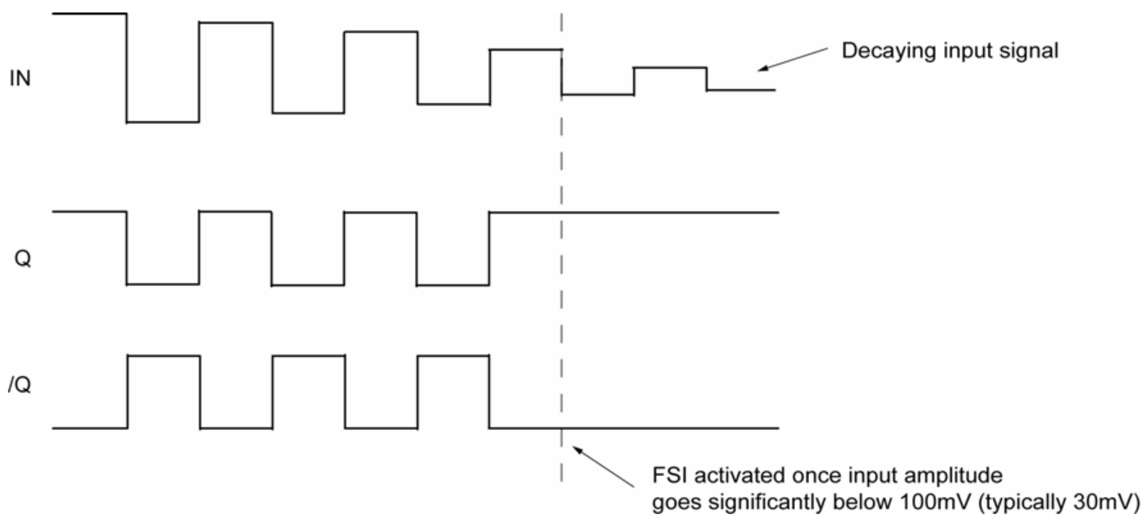
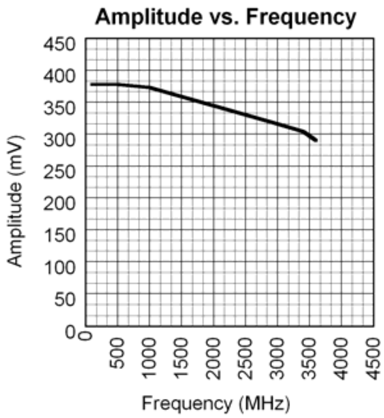
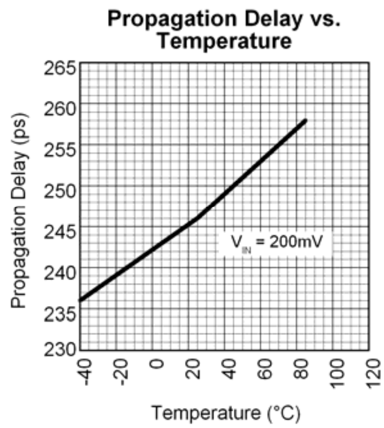


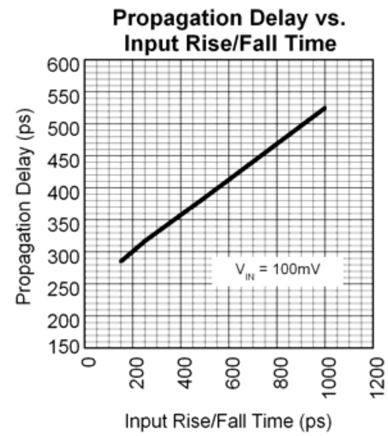
Figure 1b. Fail-Safe Feature

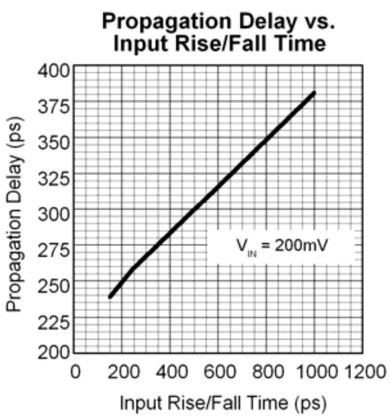
Typical Characteristics

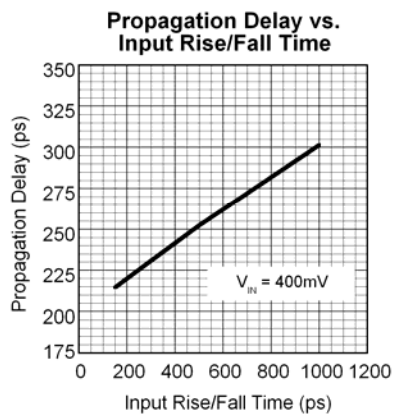
V_{CC} = 2.5V, GND = 0V, R_L = 50Ω to 1.2V, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.









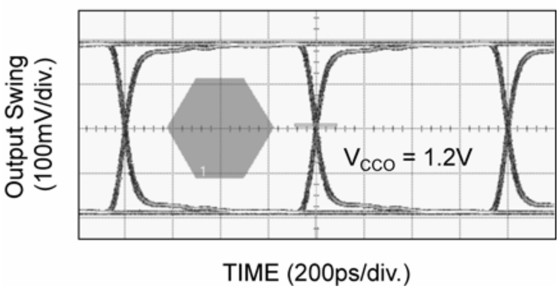


Functional Characteristics

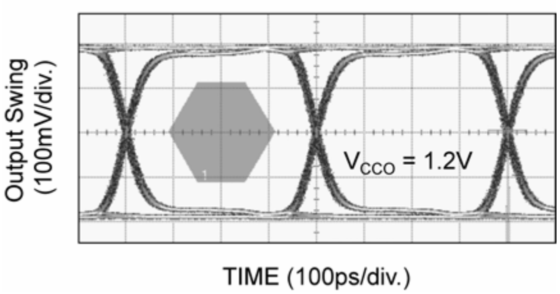
V_{CC} = 2.5V, GND = 0V, V_{IN} = 400mV, R_L = 50Ω to V_{CCO}, Data Pattern: 2^{23}-1, T_A = 25°C, unless otherwise stated.

Output Eyes with V_{CCO} = 1.2V

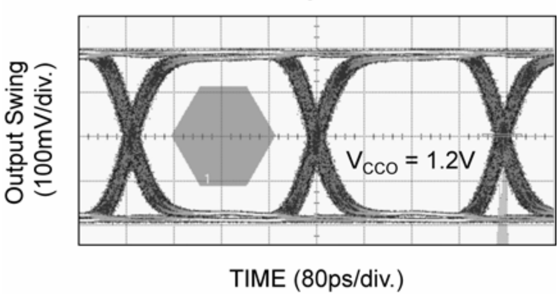
1.25Gbps Data



2.5Gbps Data

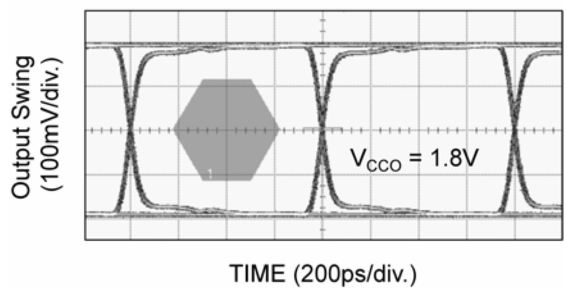


3.2Gbps Data

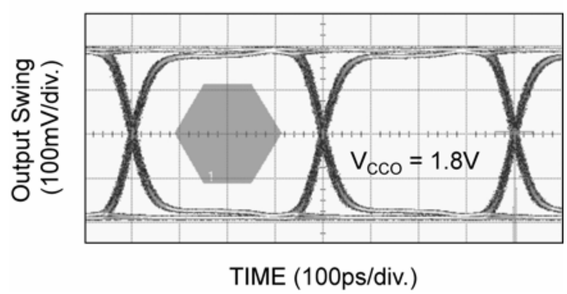


Output Eyes with V_{CCO} = 1.8V

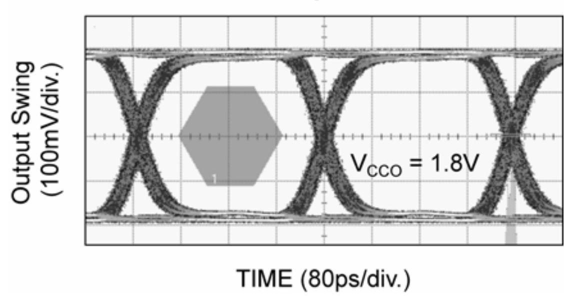
1.25Gbps Data



2.5Gbps Data

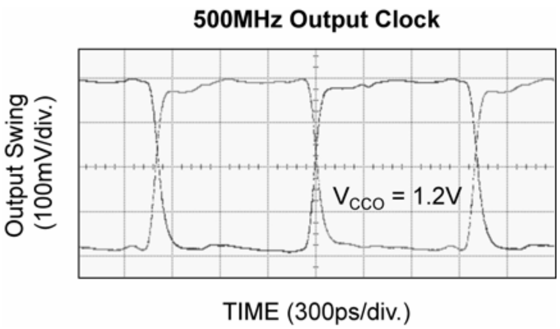


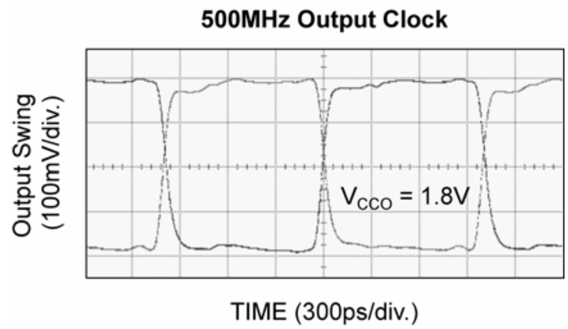
3.2Gbps Data

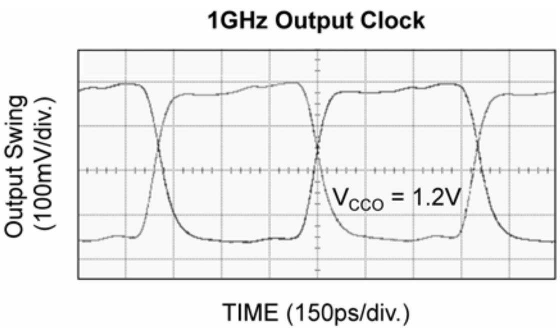


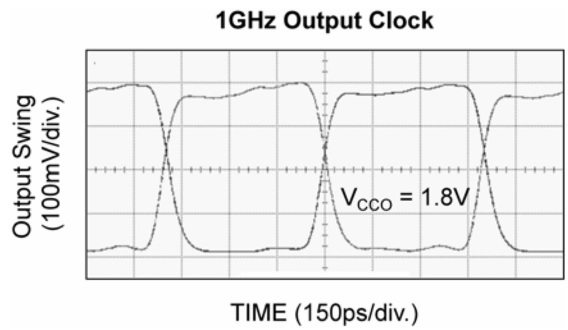
Functional Characteristics

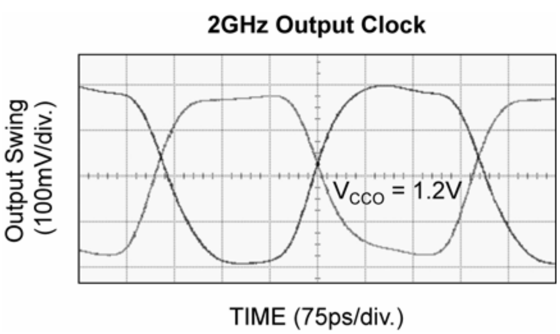
V_{CC} = 2.5V, GND = 0V, V_{IN} = 400mV, R_L = 50Ω to V_{CCO}, T_A = 25°C, unless otherwise stated.

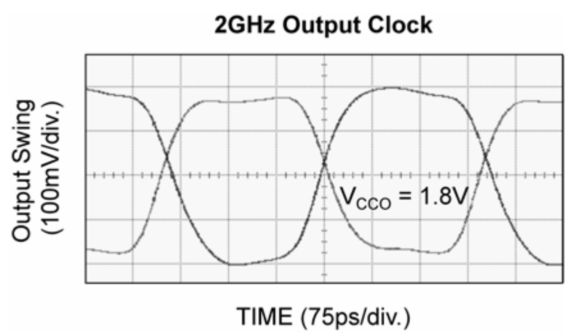


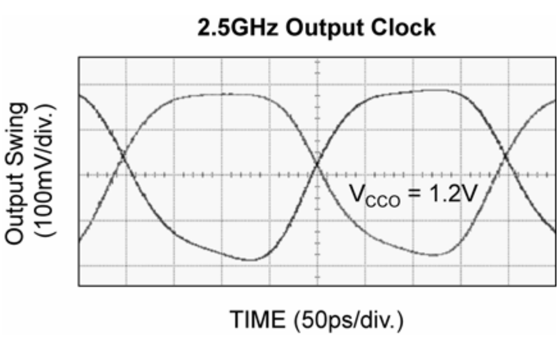


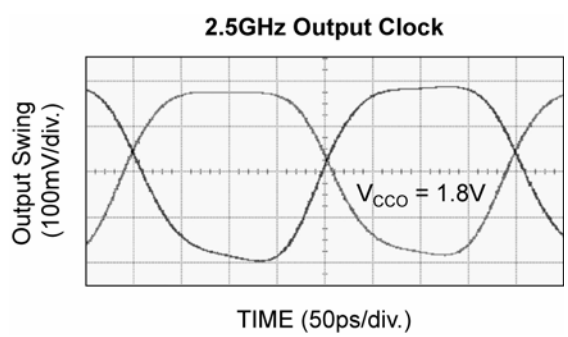












Input and Output Stage

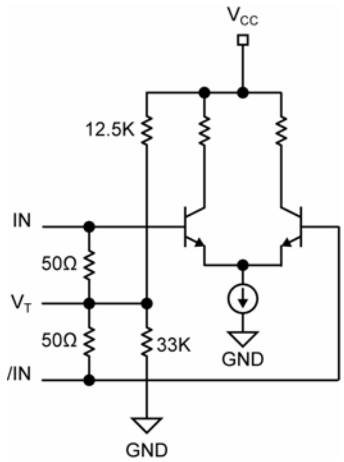


Figure 2a. Simplified Differential Input Buffer

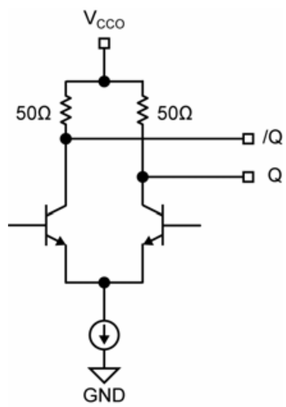


Figure 2b. Simplified CML Output Buffer

Single-Ended and Differential Swings

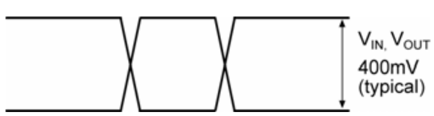


Figure 3a. Single-Ended Swing

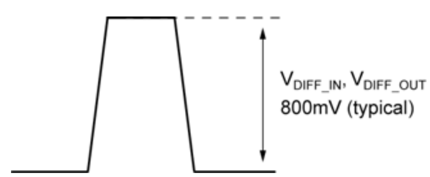


Figure 3b. Differential Swing

Input Interface Applications

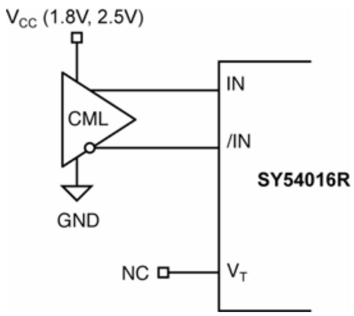


Figure 4a. CML Interface (DC-Coupled, 1.8V, 2.5V)

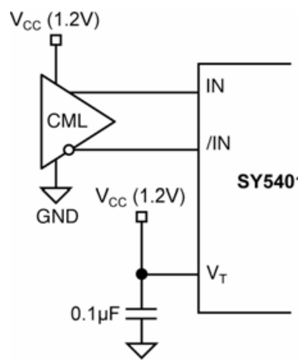


Figure 4b. CML Interface (DC-Coupled, 1.2V)

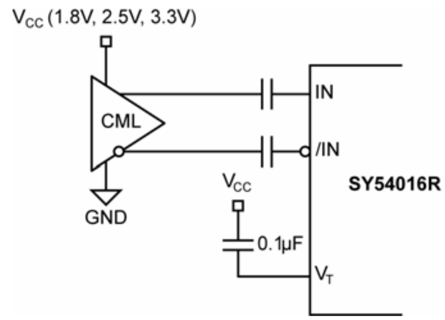


Figure 4c. CML Interface (AC-Coupled)

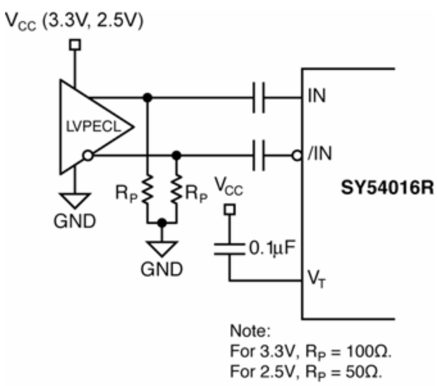


Figure 4d. LVPECL Interface (AC-Coupled)

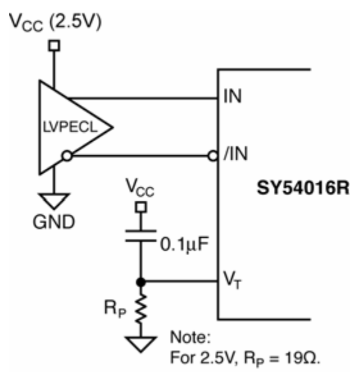


Figure 4e. LVPECL Interface (DC-Coupled)

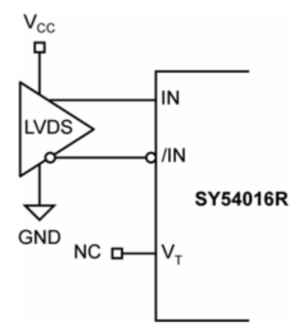


Figure 4f. LVDS Interface

CML Output Termination

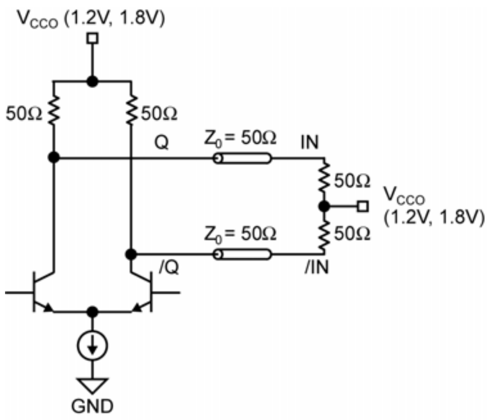


Figure 5a. 1.2 or 1.8V CML DC-Coupled Termination

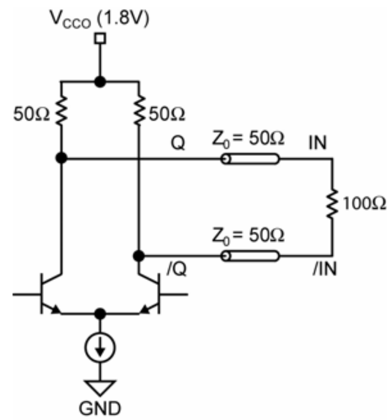


Figure 5b. 1.8V CML DC-Coupled Termination

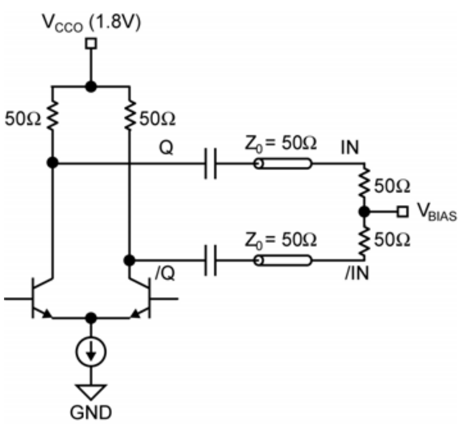


Figure 5c. CML AC-Coupled Termination
(V_{CCO} 1.8V Only)

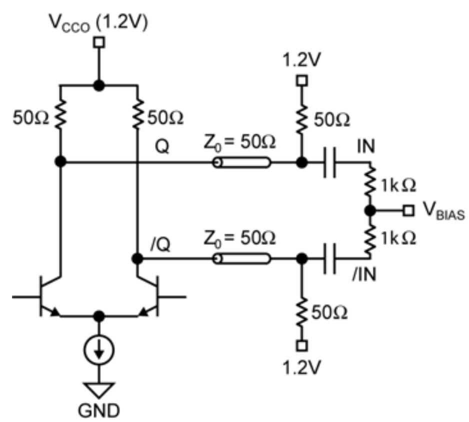
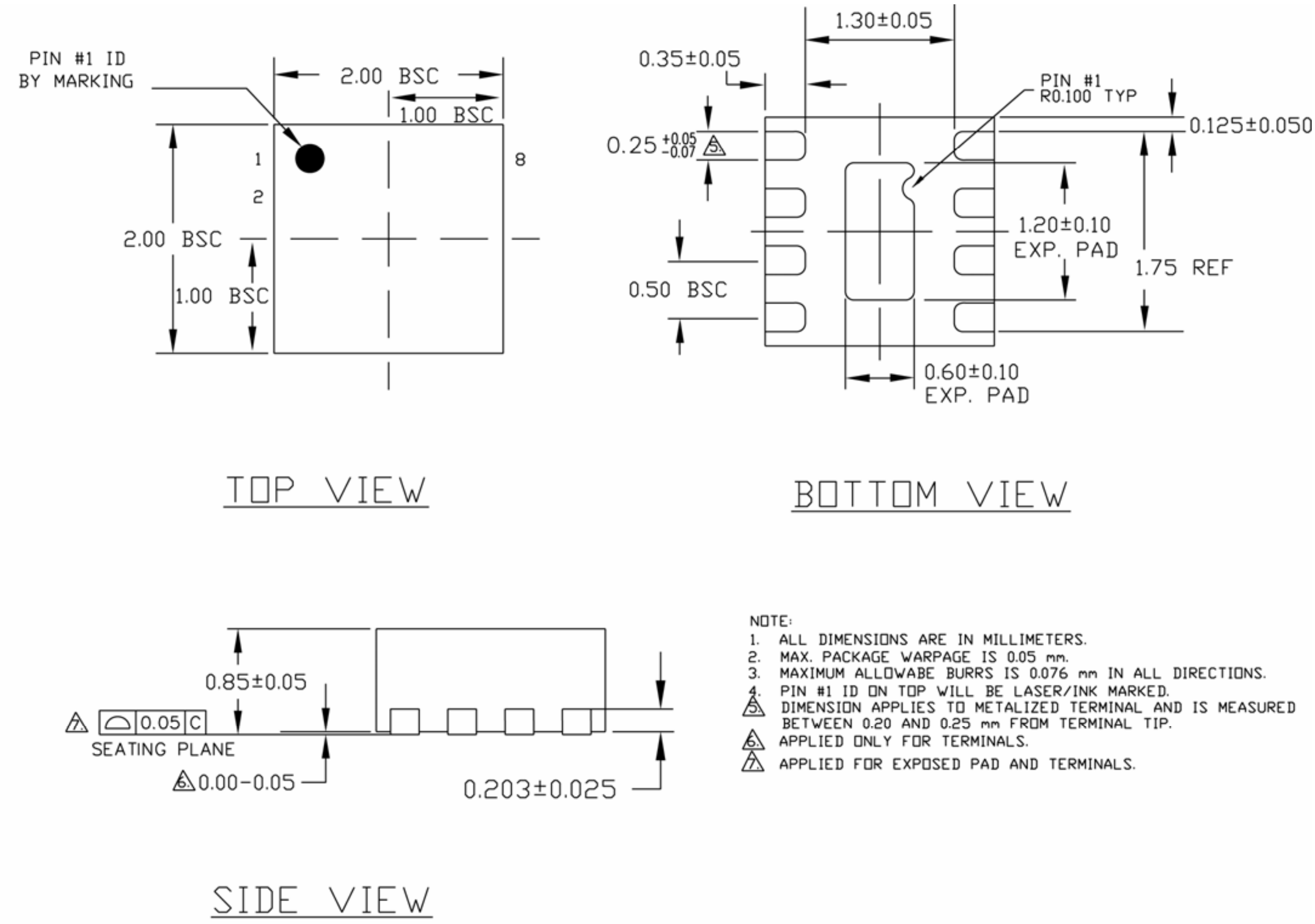


Figure 5d. CML AC-Coupled Termination
(V_{CCO} 1.2V Only)

Related Product and Support Documents

Part Number	Function	Datasheet Link
SY54016AR	3.2Gbps Precision, 1:1 Low Voltage CML Buffer with Internal Termination	http://www.micrel.com/page.do?page=/product-info/products/sy54016ar.shtml
HBW Solutions	New Products and Termination Application Notes	http://www.micrel.com/page.do?page=/product-info/as/HBWsolutions.shtml

Package Information



8-Pin MLF® (2mm x 2mm) (MLF-8)

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