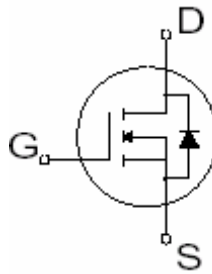


- Extremely high dv/dt capability
- Low Gate Charge Qg results in Simple Drive Requirement
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances
- Very good manufacturing repeatability



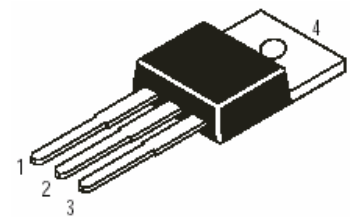
$$V_{DSS} = 900V$$

$$I_{D25} = 8.0A$$

$$R_{DS(ON)} = 1.4 \Omega$$

Description

StarMOS is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimises the JFET effect, increases packing density and reduces the on-resistance. StarMOS also achieves faster switching speeds through optimised gate layout with planar stripe DMOS technology.



Pin1-Gate
Pin2-Drain
Pin3-Source

Application

- Switching application

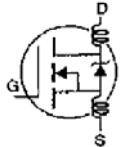
Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS}@10V$	8.0	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS}@10V$	2.8	
I_{DM}	Pulsed Drain Current ①	32	
$P_D@T_C=25^\circ C$	Power Dissipation	205	W
	Linear Derating Factor	1.64	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy ②	900	mJ
I_{AR}	Avalanche Current ①	8.0	A
E_{AR}	Repetitive Avalanche Energy ①	20.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	°C
	Soldering Temperature, for 10 seconds	300(1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw	10 lbf.in(1.1N.m)	

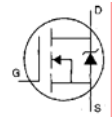
Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case	—	—	0.61	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.5	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62.5	

Electrical Characteristics @T_J=25 °C(unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	900	—	—	V	V _{GS} =0V, I _D =250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp.Coefficient	—	0.99	—	V/°C	Reference to 25°C, I _D =250μA
R _{DS(on)}	Static Drain-to-Source On-resistance	—	1.12	1.4	Ω	V _{GS} =10V, I _D =4A ④
V _{GS(th)}	Gate Threshold Voltage	3.0	—	5.0	V	V _{DS} =V _{GS} , I _D =250μA
g _{fs}	Forward Transconductance	—	9.2	—	S	V _{DS} =50V, I _D =4A
I _{DSS}	Drain-to-Source Leakage current	—	—	10	μA	V _{DS} =900V, V _{GS} =0V
		—	—	100		V _{DS} =720V, V _{GS} =0V, T _J =125°C
I _{GSS}	Gate-to-Source Forward leakage	—	—	100	nA	V _{GS} =30V
	Gate-to-Source Reverse leakage	—	—	-100		V _{GS} =-30V
Q _g	Total Gate Charge	—	45	58	nC	I _D =9A
Q _{gs}	Gate-to-Source charge	—	13	—		V _{DS} =720V
Q _{gd}	Gate-to-Drain("Miller") charge	—	18	—		V _{GS} =10V
t _{d(on)}	Turn-on Delay Time	—	50	110	nS	V _{DD} =450V
t _r	Rise Time	—	120	250		I _D =9A
t _{d(off)}	Turn-Off Delay Time	—	100	210		R _G =25Ω
t _f	Fall Time	—	75	160		
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm(0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	2100	2730	pF	V _{GS} =0V
C _{oss}	Output Capacitance	—	175	230		V _{DS} =25V
C _{rss}	Reverse Transfer Capacitance	—	14	18		f=1.0MHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	8.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	32		
V _{SD}	Diode Forward Voltage	—	—	1.4	V	T _J =25°C, I _S =8A, V _{GS} =0V ④
t _{rr}	Reverse Recovery Time	—	550	—	nS	T _J =25°C, I _S =9A
Q _{rr}	Reverse Recovery Charge	—	6.5	—	nC	di/dt=100A/μs ④
t _{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S + L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max.junction temperature(see figure 11)
- ② L = 21mH, I_{AS} = 9A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
- ③ I_{SD} ≤ 9.0A, di/dt ≤ 200A/μS, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 25°C
- ④ Pulse width ≤ 300 μS; duty cycle ≤ 2%