CMLDM7003
CMLDM7003G*
CMLDM7003J

SURFACE MOUNT PICOmini™
DUAL N-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET

PICOmini™

SOT-563 CASE

* Device is ***Halogen Free*** by design

Central™
Semiconductor Corp.

DESCRIPTION:

These CENTRAL SEMICONDUCTOR devices are dual Enhancement-mode N-Channel Field Effect Transistors, manufactured by the N-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. The CMLDM7003 utilizes the USA pinout configuration, while the CMLDM7003J utilizes the Japanese pinout configuration. These devices offer low $r_{DS\ (ON)}$ and ESD protection up to 2kV.

MARKING CODES: **CMLDM7003: C30**
CMLDM7003G*: C3G
CMLDM7003J: C3J

MAXIMUM RATINGS: (T_A=25°C)	**SYMBOL**		**UNITS**
Drain-Source Voltage	V_{DS}	50	V
Drain-Gate Voltage	V_{DG}	50	V
Gate-Source Voltage	V_{GS}	12	V
Continuous Drain Current	I_D	280	mA
Maximum Pulsed Drain Current	I_{DM}	1.5	A
Power Dissipation (Note 1)	P_D	350	mW
Power Dissipation (Note 2)	P_D	300	mW
Power Dissipation (Note 3)	P_D	150	mW
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	°C
Thermal Resistance	Θ_{JA}	357	°C/W

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: (T_A=25°C unless otherwise noted)

SYMBOL	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
I_{GSSF}, I_{GSSR}	V_{GS}=5.0V			100	nA
I_{GSSF}, I_{GSSR}	V_{GS}=10V			2.0	μA
I_{GSSF}, I_{GSSR}	V_{GS}=12V			2.0	μA
I_{DSS}	V_{DS}=50V, V_{GS}=0V			50	nA
BV_{DSS}	V_{GS}=0V, I_D=10μA	50			V
$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	0.49		1.0	V
V_{SD}	V_{GS}=0V, I_S=115mA			1.4	V
$r_{DS(ON)}$	V_{GS}=1.8V, I_D=50mA		1.6	3.0	Ω
$r_{DS(ON)}$	V_{GS}=2.5V, I_D=50mA		1.3	2.5	Ω
$r_{DS(ON)}$	V_{GS}=5.0V, I_D=50mA		1.1	2.0	Ω
g_{FS}	V_{DS}=10V, I_D=200mA	200			mS
C_{rss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz			5.0	pF
C_{iss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz			50	pF
C_{oss}	V_{DS}=25V, V_{GS}=0, f=1.0MHz			25	pF

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0 mm^2
(2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0 mm^2
(3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4 mm^2

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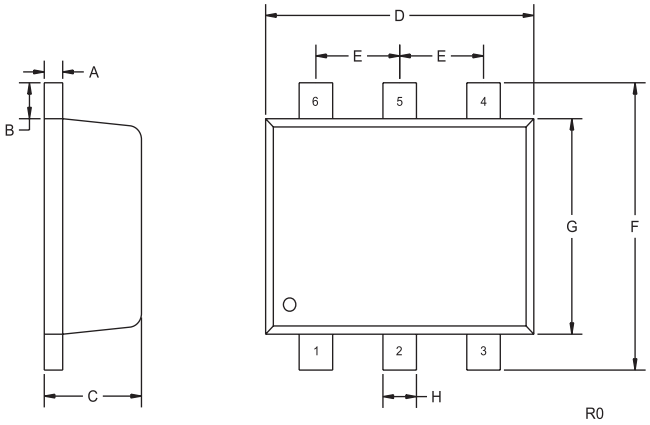
SOT-563 CASE - MECHANICAL OUTLINE

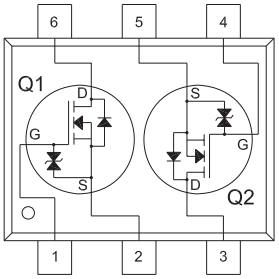


DIMENSIONS				
	INCHES		MILLIMETERS	
SYMBOL	MIN	MAX	MIN	MAX
A	0.004	0.007	0.10	0.18
B	0.008		0.20	
C	0.022	0.024	0.56	0.60
D	0.059	0.067	1.50	1.70
E	0.020		0.50	
F	0.061	0.067	1.55	1.70
G	0.047		1.20	
H	0.006	0.012	0.15	0.30

SOT-563 (REV: R0)

PIN CONFIGURATIONS

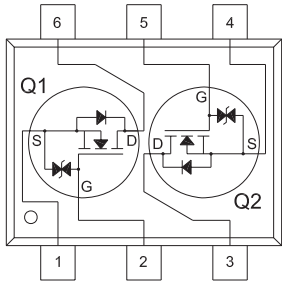
CMLDM7003 (USA Pinout)
CMLDM7003G*



LEAD CODE:
1) GATE Q1
2) SOURCE Q1
3) DRAIN Q2
4) GATE Q2
5) SOURCE Q2
6) DRAIN Q1

MARKING CODES: CMLDM7003: C30
CMLDM7003G*: C3G

CMLDM7003J (Japanese Pinout)



LEAD CODE:
1) SOURCE Q1
2) GATE Q1
3) DRAIN Q2
4) SOURCE Q2
5) GATE Q2
6) DRAIN Q1

MARKING CODE: C3J

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R5 (8-January 2009)