

Silicon PNP Power Transistors

2N5871 2N5872

DESCRIPTION

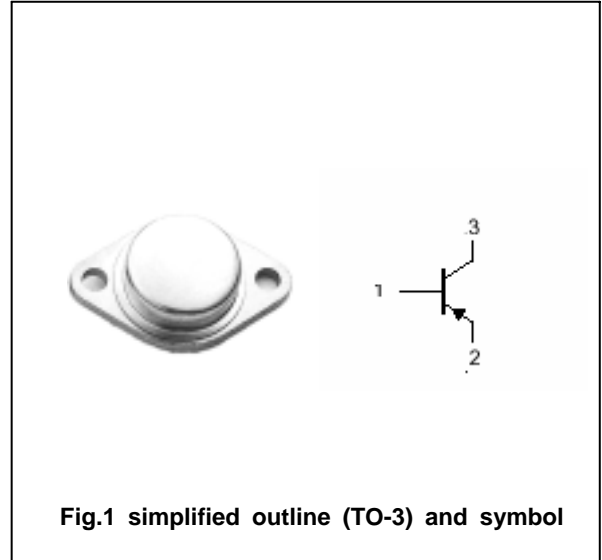
- With TO-3 package
- Low collector saturation voltage

APPLICATIONS

- For medium-speed switching and amplifier applications

PINNING

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector



Absolute maximum ratings(Ta=)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	2N5871	-60	V
		2N5872	-80	
V _{CEO}	Collector-emitter voltage	2N5871	-60	V
		2N5872	-80	
V _{EBO}	Emitter-base voltage	Open collector	-5	V
I _C	Collector current		-7	A
P _D	Total Power Dissipation	T _C =25	115	W
T _j	Junction temperature		150	
T _{stg}	Storage temperature		-65~200	

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
R _{th j-c}	Thermal resistance junction to case	1.17	/W

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CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CEO(SUS)}	Collector-emitter sustaining voltage	2N5871	-60			V
		2N5872	-80			
V _{CEsat}	Collector-emitter saturation voltage	I _C =-5A; I _B =-0.5A			-1.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =-5A; I _B =-0.5A			-1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =rated V _{CBO} ; I _B =0			-1.0	mA
I _{CEO}	Collector cut-off current	2N5871			-2.0	mA
		2N5872				
I _{EBO}	Emitter cut-off current	V _{EB} =-5V; I _C =0			-1.0	mA
h _{FE}	DC current gain	I _C =-2.5A; V _{CE} =-4V	20		100	
f _T	Transistion frequency	I _C =-0.5A; V _{CE} =-10V	4			MHz

PACKAGE OUTLINE

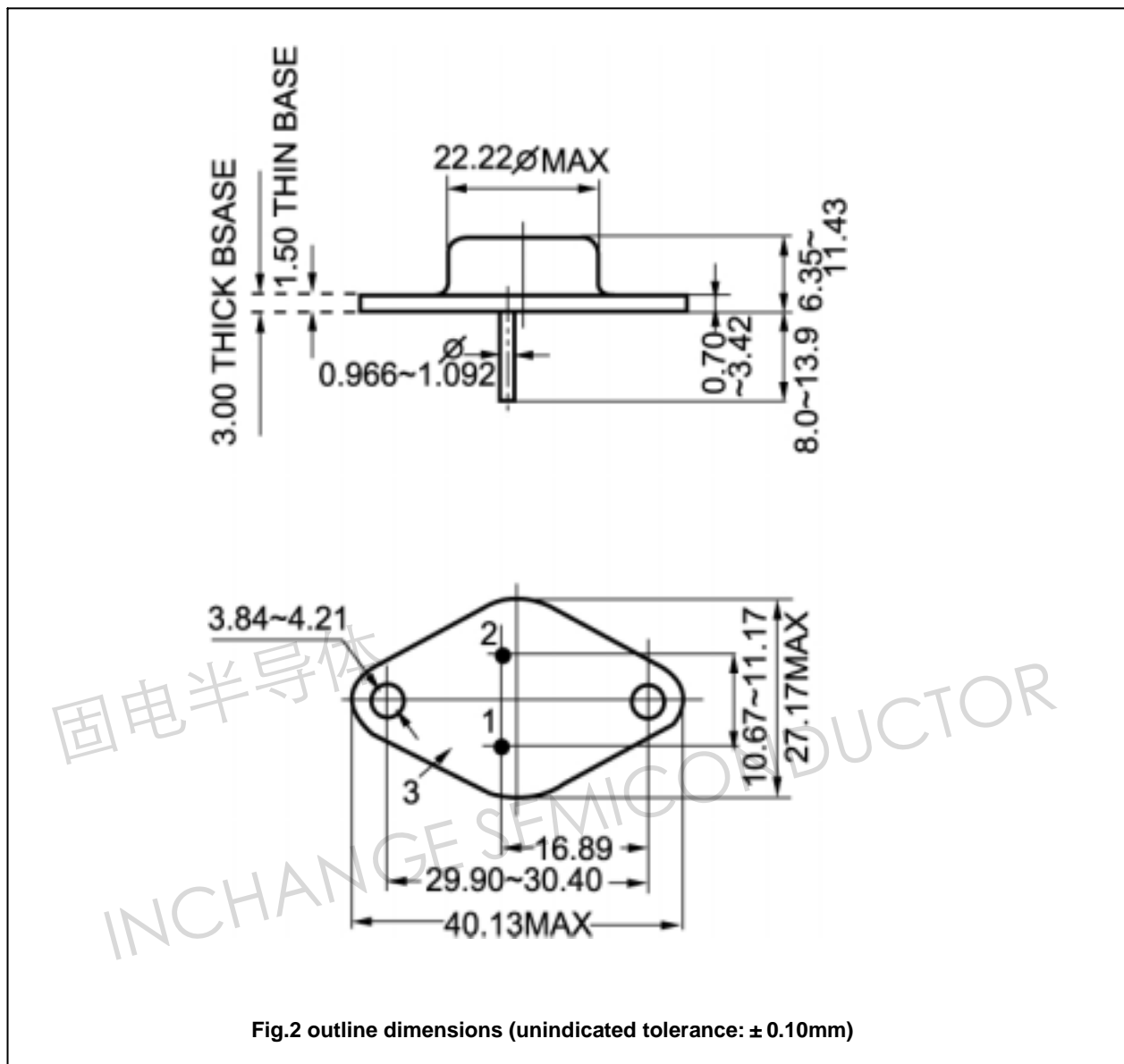


Fig.2 outline dimensions (unindicated tolerance: $\pm 0.10\text{mm}$)