

## NPN power transistor

### Features

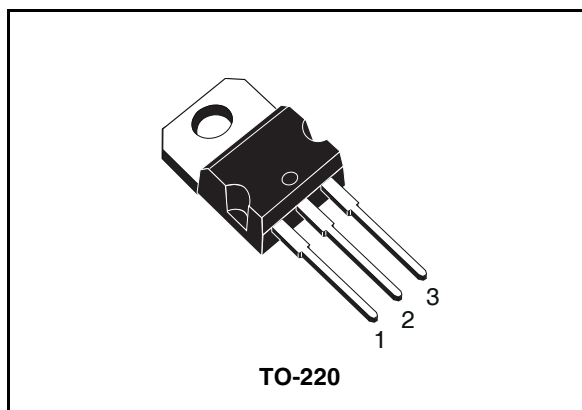
- NPN transistor

### Applications

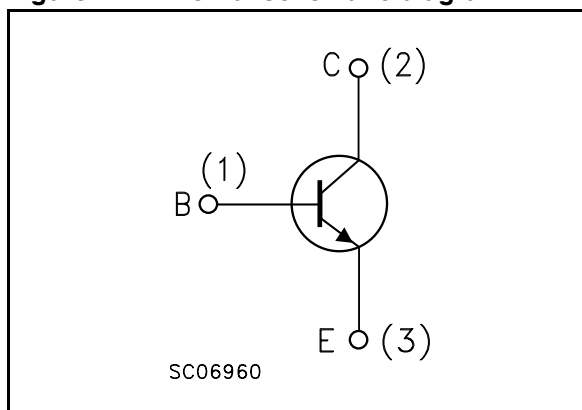
- General purpose switching and amplifier transistor

### Description

The device is manufactured in Planar technology with “Base Island” layout. The resulting transistor shows exceptional high gain performance coupled with very low saturation voltage. The PNP type is the BD240C.



**Figure 1. Internal schematic diagram**



**Table 1. Device summary**

Order code	Marking	Package	Packaging
BD239C	BD239C	TO-220	Tube

# 1 Electrical ratings

**Table 2. Absolute maximum rating**

Symbol	Parameter	Value	Unit
$V_{CER}$	Collector-emitter voltage ( $R_{BE} = 100\Omega$ )	115	V
$V_{CEO}$	Collector-base voltage ( $I_B = 0$ )	100	V
$V_{EBO}$	Emitter-base voltage ( $I_C = 0$ )	5	V
$I_C$	Collector current	2	A
$I_{CM}$	Collector peak current	4	A
$I_B$	Base current	0.6	A
$P_{TOT}$	Total dissipation at $T_{case} \leq 25^\circ\text{C}$	30	W
$P_{TOT}$	Total dissipation at $T_{amb} \leq 25^\circ\text{C}$	2	W
$T_{stg}$	Storage temperature	-65 to 150	$^\circ\text{C}$
$T_J$	Max. operating junction temperature	150	$^\circ\text{C}$

## 2 Electrical characteristics

( $T_{case} = 25^{\circ}C$  unless otherwise specified)

**Table 3. Electrical characteristics**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{CES}$	Collector cut-off current ( $V_{BE} = 0$ )	$V_{CE} = 100V$			0.2	mA
$I_{CEO}$	Collector cut-off current ( $I_B = 0$ )	$V_{CE} = 60V$			0.3	mA
$I_{EBO}$	Emitter cut-off current ( $I_C = 0$ )	$V_{EB} = 5V$			1	mA
$V_{CEO(sus)}^{(1)}$	Collector-emitter sustaining voltage ( $I_B = 0$ )	$I_C = 30mA$	100			V
$V_{CE(sat)}^{(1)}$	Collector-emitter saturation voltage	$I_C = 1A$ $I_B = 0.2A$			0.7	V
$V_{BE}^{(1)}$	Base-emitter voltage	$I_C = 1A$ $V_{CE} = 4V$			1.3	V
$h_{FE}$	DC current gain	$I_C = 0.2A$ $V_{CE} = 4V$ $I_C = 1A$ $V_{CE} = 4V$	40 15			

Note (1) Pulsed duration = 300  $\mu s$ , duty cycle  $\leq 1.5\%$

### 2.1 Electrical characteristic (curves)

**Figure 2. Safe operating area**

**Figure 3. Derating curve**

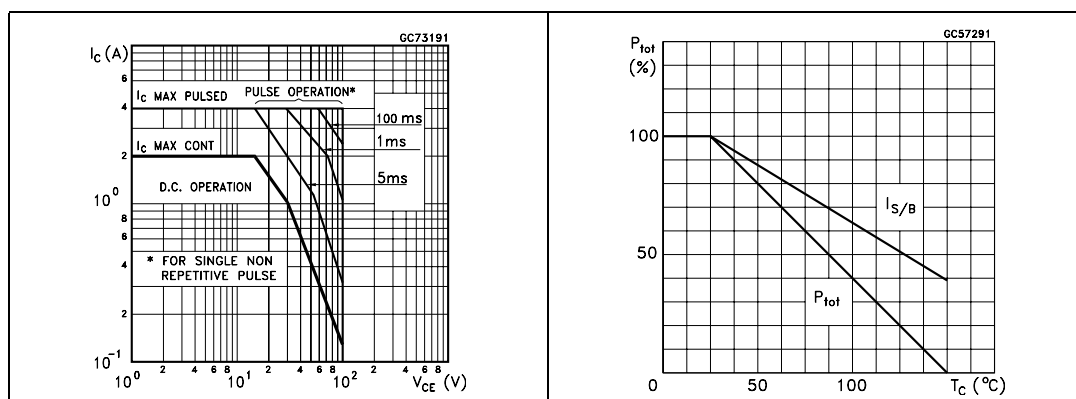


Figure 4. DC current gain

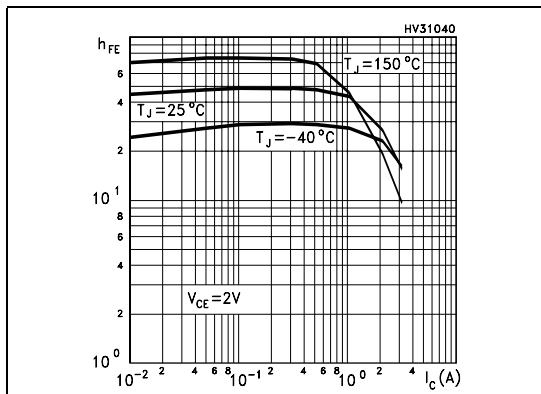


Figure 5. DC current gain

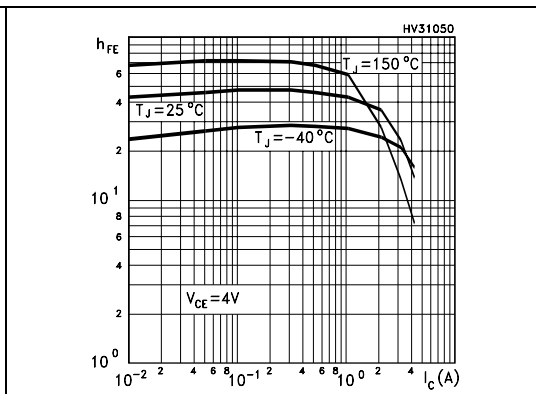


Figure 6. Collector-emitter saturation voltage

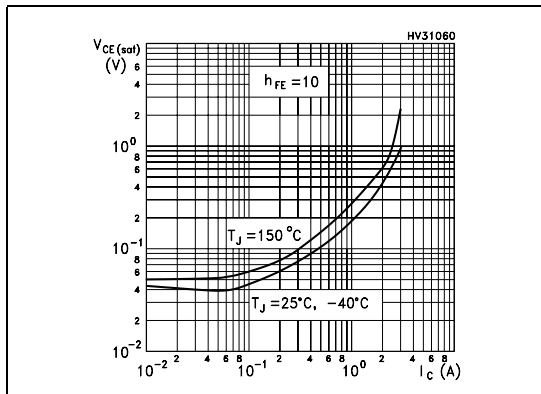


Figure 7. Base-emitter saturation voltage

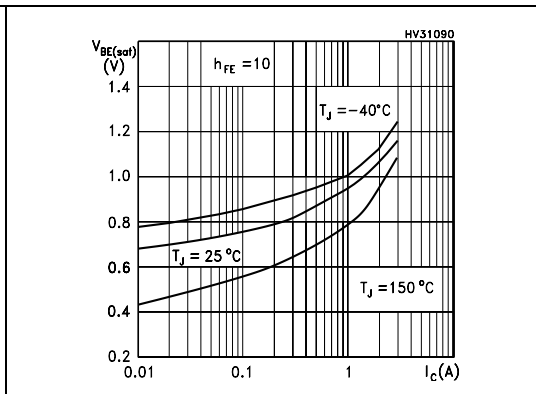


Figure 8. Base-emitter on voltage

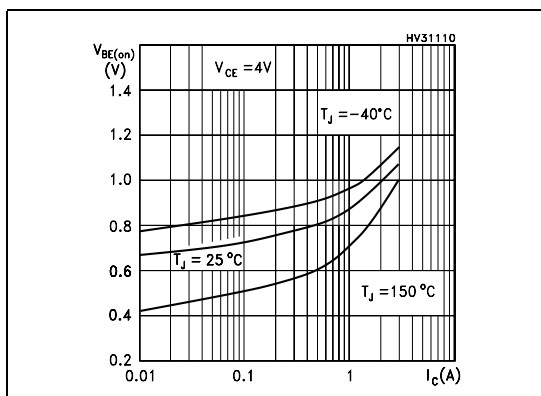


Figure 9. Resistive load switching time

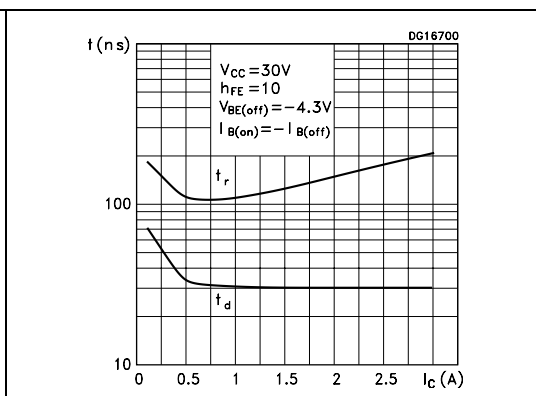
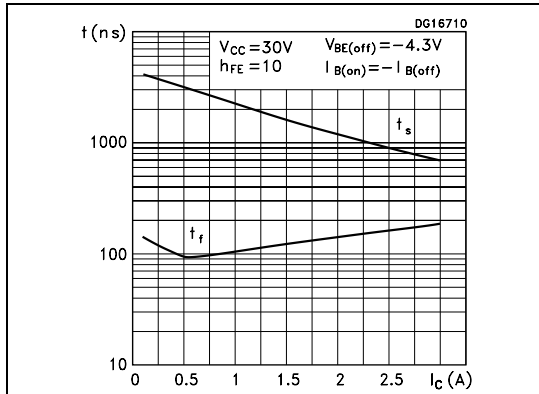
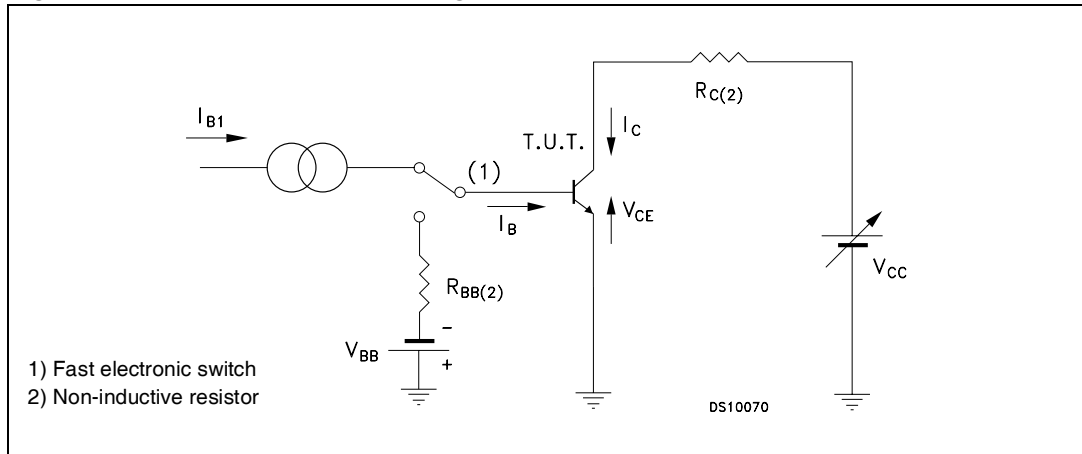


Figure 10. Resistive load switching time



## 2.2 Test circuit

Figure 11. Resistive load switching test circuit

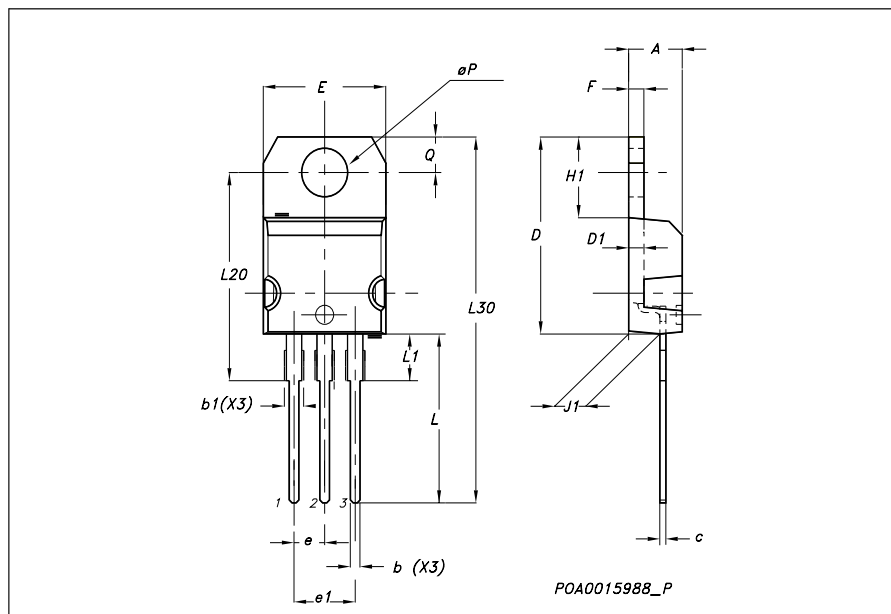


### 3 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

**TO-220 Mechanical data**

DIM.	mm.		
	MIN.	TYP	MAX.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95



## 4 Revision history

**Table 4. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
01-April-1999	1	Initial release.
02-Jul-2007	2	Figures 2,3,4,5,6,7,8,9 and figure 10 have been added.



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