Features

- Incorporates the ARM7TDMI® ARM® Thumb® Processor
  - 72 MIPS at 80MHz
  - EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support
- Additional Embedded Memories
  - One 256 Kbyte Internal ROM, Single-cycle Access at Maximum Matrix Speed
  - 160 Kbytes of Internal SRAM, Single-cycle Access at Maximum Processor or Matrix Speed (Configured in blocks of 96 KB and 64 KB with separate AHB slaves)
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, NAND Flash/SmartMedia® and CompactFlash®
- USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 2,432-byte Configurable Integrated DPRAM
- Metal Programmable Block
  - 200000 Gates Via Programmable Logic (through 3 Metal Layers) for CAP7L
  - Two 4Kbytes Dual Port RAMs for buffer space
  - High Connectivity for up to two AHB Masters and two AHB Slaves for CAP7L
  - Up to twenty-eight AIC interrupt inputs
  - Access to Atmel AHB/APB library
  - Up to 90 dedicated I/Os
  - Optional PIO controller for up to 32 of the available I/Os
- 10-bit Analog to Digital Converter (ADC)
  - Up to 8 multiplexed channels
  - 440 kSample / s
- Bus Matrix
  - Six-layer, 32-bit Matrix, Allowing 15.4 Gbps of On-chip Bus Bandwidth
- Fully-featured System Controller, including
  - Reset Controller, Shut Down Controller
  - Twenty 32-bit Battery Backup Registers for a Total of 80 Bytes
  - Clock Generator
  - Advanced Power Management Controller (APMC)
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Real-Time Timer
- Boot Mode Select Option and Remap Command
- Reset Controller
  - Based on Two Power-on Reset Cells, Reset Source Identification and Reset Output Control
- Shut Down Controller
  - Programmable Shutdown Pin Control and Wake-up Circuitry
- Clock Generator (CKGR)
  - 32768Hz Low-power Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - Internal 32kHz RC oscillator for fast start-up
  - 8 to 16 MHz On-chip Oscillator, 50 to 100 MHz PLL, and 80 to 240 MHz PLL
- Advanced Power Management Controller (APMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Four Programmable External Clock Output Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources

Customizable Microcontroller

AT91CAP7L200A

Preliminary Summary

8685AS–CAP–05/09

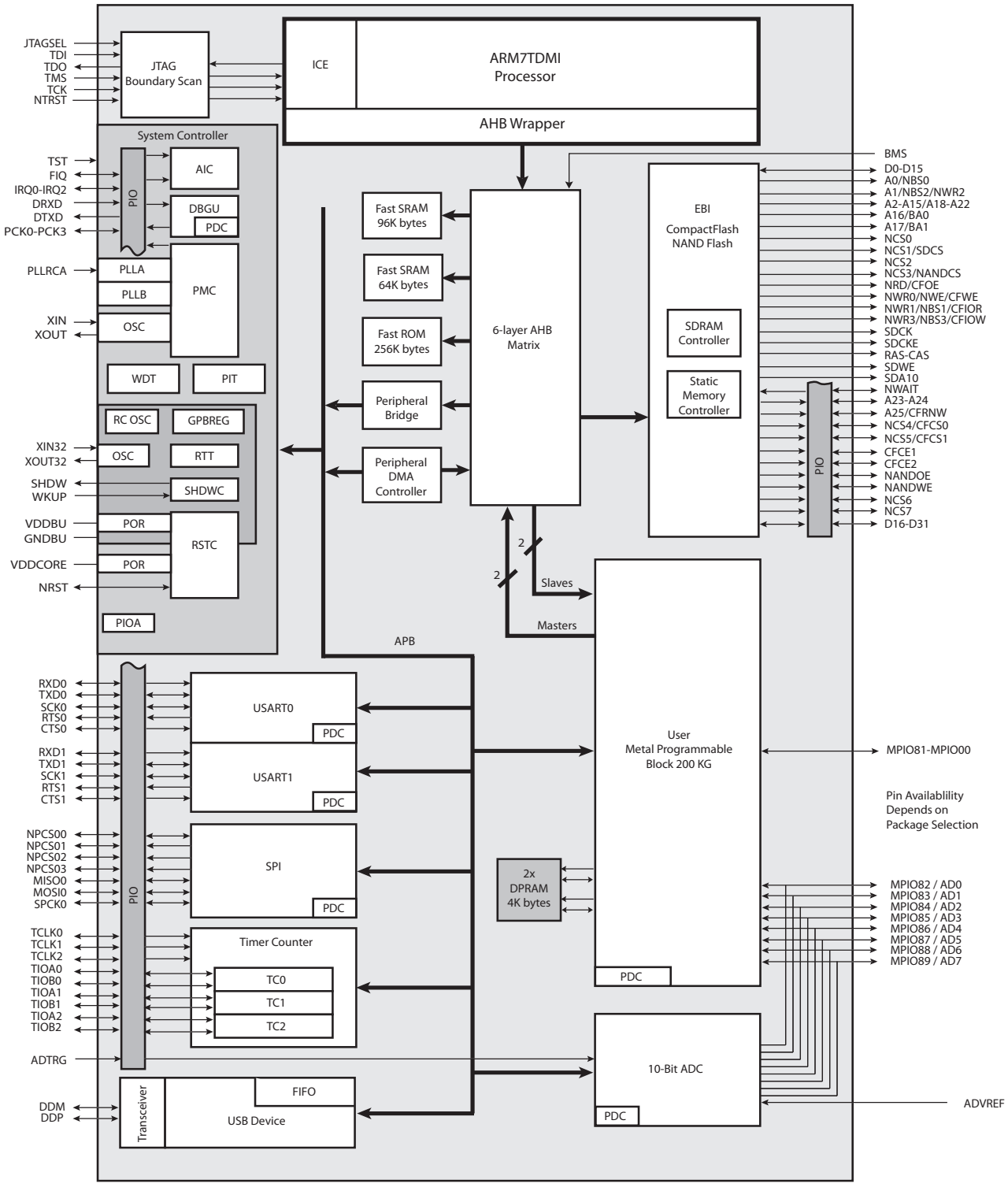
  - Two External Interrupt Sources and one Fast Interrupt Source, Spurious interrupt protected
- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit interval Timer plus 12-bit interval Counter
- Watchdog Timer (WDT)
  - Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Real-Time Timer (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- One 32-bit Parallel Input/Output Controllers (PIOA)
  - 32 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os each
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor, Bus Holder and Synchronous Output
  - Additional PIO Controllers can be added in the Metal Programmable Block
- 22 Peripheral DMA Controller Channels (PDC)
- Two Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation, Manchester Encoding/Decoding
- Master/Slave Serial Peripheral Interface (SPI)
  - 8- to 16-bit Programmable Data Length, External Peripheral Chip Select
  - Synchronous Communications at up to 80Mbits/sec
- One Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- IEEE 1149.1 JTAG Boundary Scan on All Digital Pins
- Required Power Supplies:
- 1.08V to 1.32V for VDDCORE and VDDBU
- 1.08V to 1.32V for VDDOSC, VDDOSC32, and VDDPLLB
- 3.0V to 3.6V for VDDPLLA and VDDIO
- 3.0V to 3.6V for AVDD (ADC)
- Package Options: 144 LQFP, 176 LQFP, 208 PQFP, 144 LFBGA, 176TFBGA, 208 TFBGA, 225 LFBGA

1. Description

The AT91CAP7 semi-custom System on a Chip (SoC) provides Atmel's ASIC customers a microcontroller platform for rapid integration of their own Intellectual Property (IP) in metal programmable cells. Fabrication time is greatly reduced since only the metal layers will remain to be generated on the silicon. In addition to 200K gates of metal programmable logic, the AT91CAP7 includes an ARM7TDMI core with a high-speed bus (AHB), on-chip ROM and SRAM, a full-featured system controller, and various general-purpose peripheral subsystems. It is implemented in a 130 nm CMOS 1.2V process and supports 3.3V I/O.

2. Block Diagram

Figure 2-1. AT91CAP7L Block Diagram



3. Signal Description

Table 3-1. Signal Description by Peripheral

Signal Name	Function	Type	Active Level	Comments
Power Supplies				
VDDCORE	Core Chip Power Supply	Power		1.08V to 1.32V
VDDBU	Backup Power Supply, includes Backup I/O and Logic	Power		1.08V to 1.32V, required for all operational modes.
VDDIO	I/O Lines Power Supply, except Backup I/O	Power		3.0V to 3.6V
VDDPLLA	PLL A Power Supply	Power		3.0V to 3.6V
VDDPLLB	PLL B Power Supply	Power		1.08V to 1.32V
VDDOSC	Oscillator Power Supply	Power		1.08V to 1.32V
VDDOSC32	Oscillator Power Supply	Power		1.08V to 1.32V, required for all operational modes.
AVDD	ADC Analog Power Supply	Power		3.0V to 3.6V
GND	VDDIO and VDDCORE Ground	Ground		
GNDPLLA	PLL Ground A	Ground		
GNDPLLB	PLL Ground B	Ground		
GNDOSC	Main Oscillator Ground	Ground		
GNDOSC32	32 kHz Oscillator Ground	Ground		
GNDBU	Backup Ground	Ground		
AGND	ADC Analog Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Oscillator Input	Input	Analog	Connect to an external crystal or drive with a 1.2V nominal square wave clock input
XOUT	Main Oscillator Output	Output	Analog	Connect to external crystal or leave unconnected
XIN32	Slow Clock Oscillator Input	Input	Analog	Connect to a 32768Hz crystal or drive with a 1.2V, 32kHz nominal square wave Input, leave unconnected (32kHz RC OSC only)
XOUT32	Slow Clock Oscillator Output	Output	Analog	Connect to a 32768Hz crystal or leave unconnected
PLLRCA	PLL A Filter	Input	Analog	Must connect to an appropriate RC network for proper PLL operation
PCK0 - PCK3	Programmable Clock Output	Output	Clock	access via PIOA
Analog to Digital Converter				
AD0	ADC Input 0	An. Input	Analog	shared with MPIO82

Table 3-1. Signal Description by Peripheral (Continued)

Signal Name	Function	Type	Active Level	Comments
AD1	ADC Input 1	An. Input	Analog	shared with MPIO83
AD2	ADC Input 2	An. Input	Analog	shared with MPIO84
AD3	ADC Input 3	An. Input	Analog	shared with MPIO85
AD4	ADC Input 4	An. Input	Analog	shared with MPIO86
AD5	ADC Input 5	An. Input	Analog	shared with MPIO87
AD6	ADC Input 6	An. Input	Analog	shared with MPIO88
AD7	ADC Input 7	An. Input	Analog	shared with MPIO89
ADVREF	ADC Voltage Reference Input	An. Input	Analog	Do not leave floating - Connect to AVDD externally or another analog voltage reference up to 3.3V
ADTRG	ADC External Trigger	Dig. Input	High	Tie to AGND externally if enabled and not used - access via PIOA
Shutdown, Wake-up Logic				
SHDW	Shut-Down Control	Output	High	Driven at 0V only. Do not tie over VDDBU
WKUP0WKUP0	Wake-Up Input	Input		Accept between 0V and VDDBU.
ICE and JTAG				
TCK	Test Clock	Input		Pull-down resistor
TDI	Test Data In	Input		Pull-up resistor
TDO	Test Data Out	Output		Pull-up resistor
TMS	Test Mode Select	Input		Pull-up resistor
NTRST	Test Reset Signal	Input	Low	Pull-up resistor
JTAGSEL	JTAG Selection	Input	High	Pull-down resistor
Reset/Test				
NRST	Microcontroller Reset	I/O	Low	Pull-up resistor Accept between 0V and VDDBU
TST	Chip Test Enable	Input	High	Pull-down resistor Accept between 0V and VDDBU
BMS	Boot Mode Select	Input		Pull-up resistor 1=embedded ROM 0=EBI CS0
Debug Unit - DBGU				
DRXD	Debug Receive Data	Input		access via PIOA
DTXD	Debug Transmit Data	Output		access via PIOA

Table 3-1. Signal Description by Peripheral (Continued)

Signal Name	Function	Type	Active Level	Comments
Advanced Interrupt Controller - AIC				
IRQ0 - IRQ1	External Interrupt Inputs	Input	High	access via PIOA
FIQ	Fast Interrupt Input	Input	High	access via PIOA
PIO Controller - PIOA				
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
External Bus Interface - EBI				
D0 - D31	Data Bus	I/O		Pulled-up input at reset; access D16 - D31 via PIOA
A0 - A25	Address Bus	Output		0 at reset; access A23-A25 via PIOA
NWAIT	External Wait Signal	Input	Low	access via PIOA
Static Memory Controller - SMC				
NCS0 - NCS7	Chip Select Lines	Output	Low	access NCS4 - NCS7 via PIOA
NWR0 -NWR3	Write Signal	Output	Low	
NRD	Read Signal	Output	Low	
NWE	Write Enable	Output	Low	
NBS0 - NBS3	Byte Mask Signal	Output	Low	
CompactFlash Support				
CFCE1 - CFCE2	CompactFlash Chip Enable	Output	Low	access via PIOA
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash IO Read	Output	Low	
CFIOW	CompactFlash IO Write	Output	Low	
CFRNW	CompactFlash Read Not Write	Output		access via PIOA
CFCS0 - CFCS1	CompactFlash Chip Select Lines	Output	Low	access via PIOA
NAND Flash Support				
NANDCS	NAND Flash Chip Select	Output	Low	
NANDOE	NAND Flash Output Enable	Output	Low	access via PIOA
NANDWE	NAND Flash Write Enable	Output	Low	access via PIOA
SDRAM Controller				
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output	High	
SDCS	SDRAM Controller Chip Select	Output	Low	
BA0 - BA1	Bank Select	Output		

Table 3-1. Signal Description by Peripheral (Continued)

Signal Name	Function	Type	Active Level	Comments
SDWE	SDRAM Write Enable	Output	Low	
RAS - CAS	Row and Column Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
Universal Synchronous Asynchronous Receiver Transmitter USART				
SCKx	USARTx Serial Clock	I/O		access via PIOA
TXDx	USARTx Transmit Data	I/O		access via PIOA
RXDx	USARTx Receive Data	Input		access via PIOA
RTSx	USARTx Request To Send	Output		access via PIOA
CTSx	USARTx Clear To Send	Input		access via PIOA
Timer/Counter - TC				
TCLKx	TC Channel x External Clock Input	Input		access via PIOA
TIOAx	TC Channel x I/O Line A	I/O		access via PIOA
TIOBx	TC Channel x I/O Line B	I/O		access via PIOA
Serial Peripheral Interface - SPI				
SPI_MISO	Master In Slave Out	I/O		access via PIOA
SPI_MOSI	Master Out Slave In	I/O		access via PIOA
SPI_SPCK	SPI Serial Clock	I/O		access via PIOA
SPI_NPCS0	SPI Peripheral Chip Select 0	I/O	Low	access via PIOA
SPI_NPCS1 - SPI_NPCS3	SPI Peripheral Chip Select	Output	Low	access via PIOA
USB Device Port				
DDM	USB Device Port Data -	Analog		
DDP	USB Device Port Data +	Analog		
Metal Programmable Block - MPB				
MPIO0 - MPIO89	MPB general purpose I/O	I/O		

4. Package and Pinout

The AT91CAP7 is available in a variety of RoHS-compliant packages. The following AT91CAP7 package options have pre-defined, fixed pinouts listed in various sections below:

- 225-ball LFBGA 13x13x1.4mm, 0.8 mm ball pitch
- 208-PQFP 28x28x3.4mm, 0.5 mm pin pitch
- 176-LQFP 20x20x1.4 mm, 0.5 mm pin pitch
- 144-LQFP 20x20x1.4 mm, 0.5 mm pin pitch.

The following packages are also available for AT91CAP7 on advance request. These package options may require custom BGA substrate design. The pinouts for these packages are not yet published but will be similar to their QFP counterparts listed above.

- 208-TFBGA 15x15x1.2mm, 0.8 mm ball pitch
- 176-TFBGA 10x10 12x12x1.2mm, 0.8 mm ball pitch
- 144-LFBGA 10x10x1.4mm, 0.8 mm ball pitch

4.1 Package Selection Guide

The following table summarizes the functions and interfaces available in each package.

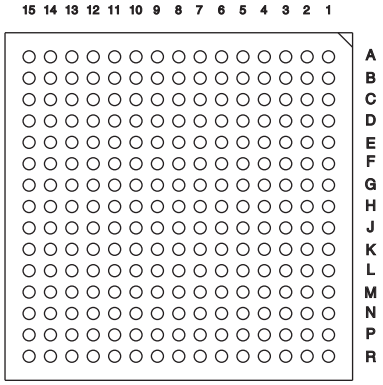
Table 4-1. AT91CAP7 Package Selection Guide

I/O Features	225 LFBGA	208 PQFP	176 LQFP	144 LQFP
MPIO pins available	82	44	33	16
MPIO / ADC Channels	8	5	8	4
Total PIOA pins available	32	32	13	11
EBI Data Bus Width	16 or 32	16 or 32	16	16
EBI Address Bus Width	26	25	23	23
SDRAM	yes	yes	yes	no
Static Memory	yes (8 cs)	yes (8 cs)	yes (7 cs)	yes (5 cs)
Compact Flash	yes	yes	yes (1 ce)	yes (1 cs/ce)
NAND Flash	yes	yes	yes	yes
Boot Mode Select	yes	yes	yes	yes
ADC External Trigger	yes	yes	yes	yes
Debug Unit	yes	yes	yes	yes
USART0	yes	yes	yes	yes
USART1	yes	yes	no	no
SPI	yes (4 cs)	yes (4 cs)	yes (3 cs)	yes (1 cs)
Timer I/O	yes	yes	no	no
External IRQ's	2	2	2	1
External FIQ	1	1	1	1
Main Clock Oscillator	yes	yes	yes	yes
32 kHz Oscillator	yes	yes	yes	yes
External APMC Clocks	4	4	no	no

4.2 Mechanical Overview of the 225-ball LFBGA Package

Figure 4-1 shows the orientation of the 225-ball LFBGA Package. A detailed mechanical description is given in the Mechanical Characteristics section of the product datasheet.

Figure 4-1. 225-ball LFBGA Pinout (Bottom View)



4.3 225-ball LFBGA Package Pinout

Warning: This package pinout is preliminary and is subject to change.

Table 4-2. AT91CAP7 Pinout for 225-ball LFBGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	MPIO81	D13	MPIO01	H10	VDDC	M7	PA22
A2	PA9	D14	MPIO75	H11	D5	M8	MPIO89/AD7
A3	PA8	D15	MPIO34	H12	PA3	M9	PA14
A4	MPIO45	E1	A3	H13	PA2	M10	MPIO70
A5	MPIO25	E2	A4	H14	A9	M11	GNDPLLA
A6	PA4	E3	MPIO80	H15	A10	M12	TDO
A7	MPIO13	E4	MPIO56	J1	D7	M13	TDI
A8	MPIO23	E5	BMS	J2	D6	M14	PA28
A9	MPIO20	E6	PA10	J3	MPIO31	M15	NWR0
A10	MPIO43	E7	NCS2	J4	D8	N1	MPIO61
A11	MPIO41	E8	MPIO09	J5	DDP	N2	MPIO64
A12	MPIO40	E9	MPIO08	J6	D2	N3	VDDBU
A13	MPIO03	E10	MPIO05	J7	GND	N4	XOUT32
A14	MPIO76	E11	MPIO39	J8	GND	N5	MPIO85/AD3
A15	A18	E12	MPIO00	J9	GND	N6	AVDD
B1	A6	E13	MPIO35	J10	A12	N7	PA20
B2	MPIO49	E14	MPIO32	J11	MPIO17	N8	PA13
B3	MPIO48	E15	SDA10	J12	PA0	N9	MPIO67
B4	MPIO46	F1	SDWE	J13	PA1	N10	NRD
B5	PA5	F2	A2	J14	MPIO19	N11	PLLRCA
B6	MPIO24	F3	MPIO55	J15	A8	N12	XIN
B7	MPIO15	F4	SDRAMCKE	K1	MPIO29	N13	VDDPLLA

Table 4-2. AT91CAP7 Pinout for 225-ball LFBGA Package (Continued)

Pin	Signal Name
B8	MPIO11
B9	MPIO22
B10	MPIO44
B11	MPIO06
B12	MPIO04
B13	MPIO37
B14	MPIO74
B15	A20
C1	MPIO52
C2	NCS3
C3	MPIO50
C4	MPIO79
C5	PA7
C6	MPIO27
C7	PA6
C8	MPIO12
C9	MPIO21
C10	MPIO07
C11	MPIO38
C12	MPIO78
C13	A22
C14	A21
C15	A17
D1	MPIO54
D2	A5
D3	A7
D4	NCS0
D5	MPIO51
D6	MPIO47
D7	NWR3
D8	MPIO14
D9	MPIO10
D10	MPIO42
D11	MPIO77
D12	MPIO02

Pin	Signal Name
F5	MPIO53
F6	A0
F7	VDDIO
F8	MPIO26
F9	VDDIO
F10	A19
F11	MPIO36
F12	MPIO33
F13	A14
F14	A16
F15	A15
G1	MPIO28
G2	SDRAMCLK
G3	A1
G4	D14
G5	D15
G6	VDDC
G7	GND
G8	GND
G9	GND
G10	VDDIO
G11	RAS
G12	N/C
G13	A11
G14	CAS
G15	A13
H1	D10
H2	D9
H3	D13
H4	D11
H5	D12
H6	VDDIO
H7	GND
H8	GND
H9	GND

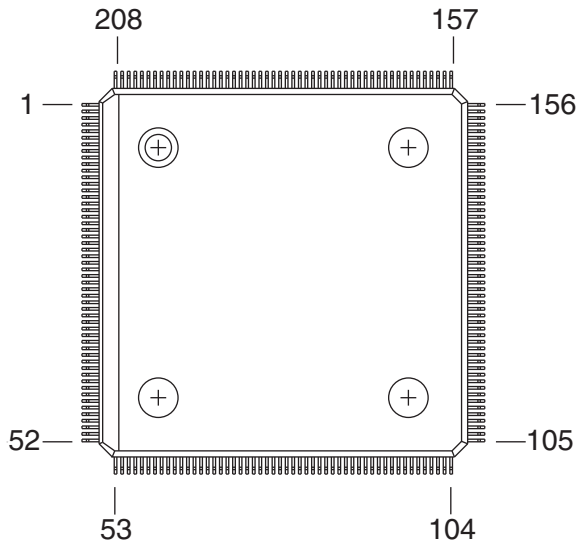
Pin	Signal Name
K2	MPIO30
K3	MPIO60
K4	MPIO59
K5	MPIO62
K6	WKUP0
K7	VDDIO
K8	VDDC
K9	VDDIO
K10	XOUT
K11	PA25
K12	TMS
K13	PA24
K14	MPIO16
K15	MPIO18
L1	MPIO57
L2	MPIO58
L3	D1
L4	MPIO65
L5	VDDOSC32
L6	GNDBU
L7	MPIO86/AD4
L8	NCS1
L9	PA17
L10	GNDPLLB
L11	PA31
L12	NTRST
L13	MPIO73
L14	PA30
L15	PA18
M1	DDM
M2	MPIO63
M3	D0
M4	XIN32
M5	GNDOSC32
M6	MPIO83/AD1

Pin	Signal Name
N14	PA29
N15	NRST
P1	D4
P2	D3
P3	SHDW
P4	TST
P5	MPIO82/AD0
P6	MPIO87/AD5
P7	PA21
P8	PA16
P9	PA11
P10	MPIO68
P11	GNDOSC
P12	NWR1
P13	VDDOSC
P14	TCK
P15	PA27
R1	JTAGSEL
R2	ADVREF
R3	MPIO84/AD2
R4	MPIO88/AD6
R5	AGND
R6	PA23
R7	PA19
R8	PA15
R9	PA12
R10	MPIO66
R11	MPIO69
R12	MPIO71
R13	MPIO72
R14	VDDPLLB
R15	PA26

4.4 Mechanical Overview of the 208-pin PQFP Package

Figure 4-2 shows the orientation of the 208-pin PQFP Package. A detailed mechanical description is given in the Mechanical Characteristics section of the product datasheet.

Figure 4-2. 208-pin PQFP Pinout (Top View)



4.5 208-pin PQFP Package Pinout

Warning: The package pinout is preliminary and is subject to change.

Table 4-3. AT91CAP7 Pinout for 208-pin PQFP Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	NTRST	53	MPIO01	105	A7	157	VDDOSC32
2	TDI	54	MPIO02	106	GND	158	XIN32
3	PA31	55	VDDIO	107	VDDIO	159	XOUT32
4	TDO	56	GND	108	A6	160	GNDOSC32
5	PA30	57	MPIO03	109	A5	161	VDDBU
6	TMS	58	MPIO04	110	VDDCORE	162	SHDW
7	PA29	59	MPIO05	111	MPIO55	163	WKUP0
8	TCK	60	MPIO41	112	A4	164	JTAGSEL
9	PA28	61	MPIO06	113	MPIO56	165	TST
10	GND	62	MPIO42	114	GND	166	GNDBU
11	PA27	63	MPIO07	115	NCS2	167	ADVREF
12	VDDIO	64	MPIO43	116	A3	168	MPIO82/AD0
13	PA26	65	GND	117	SDRAMCKE	169	MPIO83/AD1
14	NRST	66	GND	118	A2	170	MPIO84/AD2
15	PA25	67	MPIO44	119	SDWE	171	MPIO85/AD3
16	NWR0	68	VDDIO	120	VDDIO	172	MPIO86/AD4

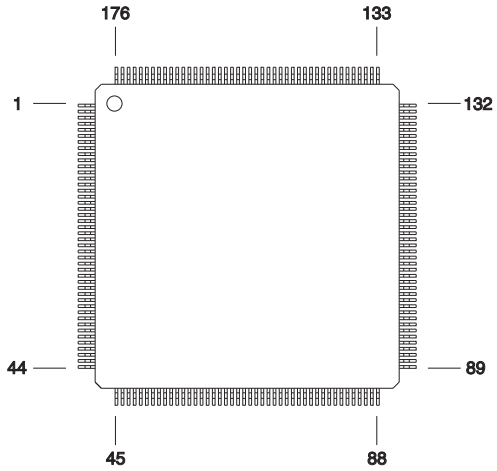
Table 4-3. AT91CAP7 Pinout for 208-pin PQFP Package (Continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
17	PA24	69	MPIO20	121	SDRAMCLK	173	AVDD
18	PA0	70	MPIO08	122	A1	174	AGND
19	MPIO16	71	MPIO21	123	MPIO28	175	GND
20	PA1	72	MPIO09	124	GND	176	PA23
21	MPIO17	73	MPIO22	125	A0	177	VDDIO
22	VDDCORE	74	MPIO10	126	D15	178	PA22
23	MPIO18	75	MPIO23	127	D14	179	GND
24	GND	76	VDDCORE	128	D13	180	PA21
25	MPIO19	77	VDDIO	129	D12	181	NCS1
26	PA2	78	MPIO11	130	D11	182	PA20
27	PA3	79	GND	131	D10	183	VDDCORE
28	A8	80	MPIO12	132	D9	184	PA19
29	A9	81	MPIO13	133	D8	185	PA18
30	VDDIO	82	MPIO14	134	D7	186	PA17
31	A10	83	MPIO15	135	GND	187	PA16
32	A11	84	PA4	136	D6	188	PA15
33	A12	85	NWR3	137	VDDIO	189	PA14
34	A13	86	PA5	138	D5	190	PA13
35	A14	87	MPIO24	139	MPIO29	191	PA12
36	VDDCORE	88	GND	140	GND	192	PA11
37	GND	89	MPIO25	141	MPIO30	193	GND
38	GND	90	PA6	142	MPIO31	194	VDDCORE
39	CAS	91	MPIO26	143	MPIO57	195	GND
40	A15	92	PA7	144	VDDCORE	196	NWR1
41	RAS	93	MPIO27	145	MPIO58	197	NRD
42	A16	94	VDDIO	146	GND	198	VDDIO
43	SDA10	95	MPIO45	147	MPIO59	199	VDDPLLB
44	VDDIO	96	VDDCORE	148	DDM	200	GNDPLLB
45	A17	97	MPIO46	149	DDP	201	GNDOSC
46	A18	98	PA8	150	MPIO60	202	XIN
47	A19	99	PA9	151	VDDIO	203	XOUT
48	A20	100	GND	152	D4	204	VDDOSC
49	A21	101	PA10	153	D3	205	VDDPLLA
50	GND	102	NCS3	154	D2	206	GNDPLLA
51	A22	103	NCS0	155	D1	207	PLLRCA
52	MPIO00	104	BMS	156	D0	208	GNDPLLA

4.6 Mechanical Overview of the 176-pin LQFP Package

Figure 4-3 shows the orientation of the 176-pin LQFP Package. A detailed mechanical description is given in the Mechanical Characteristics section of the product datasheet.

Figure 4-3. 176-pin LQFP Pinout (Top View)



4.7 176-pin LQFP Package Pinout

Warning: The package pinout is preliminary and is subject to change.

Table 4-4. AT91CAP7 Pinout for 176-pin LQFP Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	NTRST	45	MPIO01	89	A7	133	VDDOSC32
2	TDI	46	MPIO02	90	GND	134	XIN32
3	TDO	47	VDDIO	91	VDDIO	135	XOUT32
4	TMS	48	GND	92	A6	136	GNDOSC32
5	TCK	49	MPIO03	93	A5	137	VDDBU
6	GND	50	MPIO04	94	VDDCORE	138	SHDW
7	VDDIO	51	MPIO05	95	A4	139	WKUP0
8	NRST	52	MPIO06	96	GND	140	JTAGSEL
9	NWR0	53	MPIO07	97	A3	141	TST
10	PA0	54	GND	98	SDRAMCKE	142	GNDBU
11	MPIO16	55	VDDIO	99	A2	143	ADVREF
12	PA1	56	MPIO20	100	SDWE	144	MPIO82/AD0
13	MPIO17	57	MPIO8	101	VDDIO	145	MPIO83/AD1
14	VDDCORE	58	MPIO21	102	SDRAMCLK	146	MPIO84/AD2
15	MPIO18	59	MPIO09	103	A1	147	MPIO85/AD3
16	GND	60	MPIO22	104	MPIO28	148	MPIO86/AD4
17	MPIO19	61	MPIO10	105	GND	149	MPIO87/AD5
18	PA2	62	MPIO23	106	A0	150	MPIO88/AD6

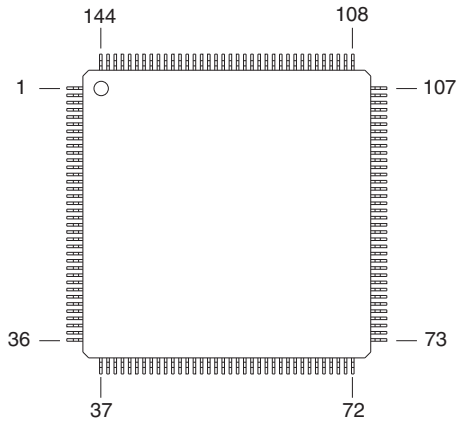
Table 4-4. AT91CAP7 Pinout for 176-pin LQFP Package (Continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
19	PA3	63	VDDCORE	107	D15	151	MPIO89/AD7
20	A8	64	MPIO11	108	D14	152	AVDD
21	A9	65	GND	109	D13	153	AGND
22	VDDIO	66	MPIO12	110	D12	154	GND
23	A10	67	MPIO13	111	D11	155	VDDIO
24	A11	68	MPIO14	112	D10	156	GND
25	A12	69	MPIO15	113	D9	157	NCS1
26	A13	70	PA4	114	D8	158	VDDCORE
27	A14	71	NWR3	115	D7	159	PA12
28	VDDCORE	72	PA5	116	GND	160	PA11
29	GND	73	MPIO24	117	D6	161	GND
30	CAS	74	GND	118	D5	162	VDDCORE
31	A15	75	MPIO25	119	MPIO29	163	GND
32	RAS	76	PA6	120	GND	164	NWR1
33	A16	77	MPIO26	121	MPIO30	165	NRD
34	SDA10	78	PA7	122	MPIO31	166	VDDIO
35	VDDIO	79	MPIO27	123	VDDCORE	167	VDDPLLB
36	MPIO32	80	VDDIO	124	GND	168	GNDPLLB
37	A17	81	VDDCORE	125	DDM	169	GNDOSC
38	A18	82	PA8	126	DDP	170	XIN
39	A19	83	PA9	127	VDDIO	171	XOUT
40	A20	84	GND	128	D4	172	VDDOSC
41	A21	85	PA10	129	D3	173	VDDPLLA
42	GND	86	NCS3	130	D2	174	GNDPLLA
43	A22	87	NCS0	131	D1	175	PLLRCA
44	MPIO00	88	BMS	132	D0	176	GNDPLLA

4.8 Mechanical Overview of the 144-pin LQFP Package

Figure 4-4 shows the orientation of the 144-pin LQFP Package. A detailed mechanical description is given in the Mechanical Characteristics section of the product datasheet.

Figure 4-4. 144-pin LQFP Pinout (Top View)



4.9 144-pin LQFP Package Pinout

Warning: This package pinout is preliminary and is subject to change.

Table 4-5. AT91CAP7 Pinout for 144-pin LQFP Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	NTRST	37	MPIO01	73	A7	109	VDDOSC32
2	TDI	38	MPIO02	74	GND	110	XIN32
3	TDO	39	VDDIO	75	VDDIO	111	XOUT32
4	TMS	40	GND	76	A6	112	GNDOSC32
5	TCK	41	MPIO03	77	A5	113	VDDBU
6	GND	42	MPIO04	78	VDDCORE	114	SHDW
7	VDDIO	43	MPIO05	79	A4	115	WKUP0
8	NRST	44	MPIO06	80	GND	116	JTAGSEL
9	NWR0	45	MPIO07	81	A3	117	TST
10	PA0	46	GND	82	A2	118	GNDBU
11	PA1	47	VDDIO	83	VDDIO	119	ADVREF
12	VDDCORE	48	MPIO8	84	A1	120	MPIO82/AD0
13	GND	49	MPIO09	85	GND	121	MPIO83/AD1
14	PA2	50	MPIO10	86	A0	122	MPIO84/AD2
15	PA3	51	VDDCORE	87	D15	123	MPIO85/AD3
16	A8	52	MPIO11	88	D14	124	AVDD
17	A9	53	GND	89	D13	125	AGND
18	VDDIO	54	MPIO12	90	D12	126	GND
19	A10	55	MPIO13	91	D11	127	VDDIO

Table 4-5. AT91CAP7 Pinout for 144-pin LQFP Package (Continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
20	A11	56	MPIO14	92	D10	128	GND
21	A12	57	MPIO15	93	D9	129	VDDCORE
22	A13	58	PA4	94	D8	130	GND
23	A14	59	NWR3	95	D7	131	VDDCORE
24	VDDCORE	60	PA5	96	D6	132	NWR1
25	GND	61	GND	97	D5	133	NRD
26	A15	62	PA6	98	GND	134	VDDIO
27	A16	63	PA7	99	VDDCORE	135	VDDPLLB
28	VDDIO	64	VDDIO	100	GND	136	GNDPLLB
29	A17	65	VDDCORE	101	DDM	137	GNDOSC
30	A18	66	PA8	102	DDP	138	XIN
31	A19	67	PA9	103	VDDIO	139	XOUT
32	A20	68	GND	104	D4	140	VDDOSC
33	A21	69	PA10	105	D3	141	VDDPLLA
34	GND	70	NCS3	106	D2	142	GNDPLLA
35	A22	71	NCS0	107	D1	143	PLLRCA
36	MPIO00	72	BMS	108	D0	144	GNDPLLA

5. Power Considerations

5.1 Power Supplies

The AT91CAP7 has several types of power supply pins:

- VDDCORE pins: Power the core, including the processor, the embedded memories and the peripherals; voltage ranges from 1.08V and 1.32V (1.2V nominal). The associated ground pins for this supply and the VDDIO supply are the GND pins.
- VDDIO pins: Power the non-backup I/O lines; voltage ranges between 3.0V and 3.6V (3.3V nominal). The associated ground pins for this supply and the VDDCORE supply are the GND pins.
- VDDBU pin: Powers the RC oscillator, Backup I/O and part of the System Controller; voltage ranges from 1.08V and 1.32V, (1.2V nominal). The associated ground pin for this supply is the GNDBU pin. Required for all operational modes.
- VDDPLLA pin: Powers the PLLA cell; voltage ranges from 3.0V and 3.6V (3.3V nominal). The associated ground pin for this supply is the GNDPLLA pin.
- VDDPLLB pin: Powers the PLLB cell and related internal loop filter cell; voltage ranges from 1.08V and 1.32V (1.2V nominal). The associated ground pin for this supply is the GNDPLLB pin.
- VDDOSC pins: Powers the Main Oscillator cell; voltage ranges from 1.08V and 1.32V (1.2V nominal). The associated ground pin for this supply is the GNDOSC pin.
- VDDOSC32 pins: Powers the 32 kHz oscillator cell; voltage ranges from 1.08V and 1.32V (1.2V nominal). The associated ground pin for this supply is the GNDOSC32 pin. Required for all operational modes.
- AVDD pin: Powers the 10-bit Analog to Digital Converter and associated cells; voltage ranges from 3.0V and 3.6V (3.3V nominal). The associated ground pin for this supply is the AGND pin.

5.2 Power Consumption

Note: The following figures are preliminary figures based on prototype silicon. They are subject to change for the production silicon.

The AT91CAP7 consumes about 600 µA of static current on VDDCORE at typical conditions (1.2V, 25°C).

On VDDBU, the current does not exceed 30 µA at typical conditions.

For dynamic power consumption, the AT91CAP7 consumes about 0.33 mW/MHz of power or 275 µA/MHz of current on VDDCORE at typical conditions (1.2V, 25°C) and with the ARM sub-system running full-performance algorithm with on-chip memories, and no peripherals active.

5.3 Power Supply Isolation

All power supplies must be active in normal operation. CAP7 supports a low power backup mode in which most of the core including the processor can be powered down. In backup mode, it is mandatory to keep VDDBU and VDDOSC32 active; all other supplies must be inactive.

6. I/O Line Considerations

6.1 JTAG Port Pins

TMS and TDI are Schmitt trigger inputs with pull-up resistors. TCK is a Schmitt trigger input with pull-down resistor.

TDO is an output, driven at up to VDDIO, with a pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. It integrates a permanent pull-down resistor of about 100kohm to GNDBU, so that it can be left unconnected for normal operations.

The NTRST signal is described in the Reset Pins paragraph. JTAGSEL is supplied with VDDBU, all other JTAG signals are supplied with VDDIO.

6.2 Test Pin

The TST pin is used for manufacturing test purposes when asserted high. It integrates a permanent pull-down resistor of about 100 kΩ to GNDBU, so that it can be left unconnected for normal operations. Driving this line at a high level leads to unpredictable results.

This pin is supplied with VDDBU.

6.3 Reset Pins

NRST is an open-drain output integrating a non-programmable pull-up resistor. It can be driven with voltage at up to VDDIO.

NTRST is an input which allows reset of the JTAG Test Access port. It has no action on the processor for both ARM core and boundary scan.

As the product integrates power-on reset cells, which manages the processor and the JTAG reset, the NRST and NTRST pins can be left unconnected.

The NRST and NTRST pins both integrate a permanent pull-up resistor of 100 kΩ minimum to VDDIO.

6.4 PIO Controllers

All the I/O lines which are managed by a PIO Controller integrate a programmable pull-up resistor of 100 kΩ minimum. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers.

After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that must be enabled as Peripheral at reset. This is explicitly indicated in the column “Reset State” of the PIO Controller multiplexing tables.

6.5 Shut Down Logic pins

The SHDW pin is an output only, which is driven by the Shut Down Controller only at low level. It can be tied high with an external pull-up resistor at VDDBU only.

7. Processor and Architecture

7.1 ARM7TDMI Processor

- **RISC Processor Based on ARMv4T Von Neumann Architecture**
  - **Runs at up to 80 MHz, providing up to 72 MIPS**
- **Two instruction sets**
  - **ARM high-performance 32-bit Instruction Set**
  - **Thumb high code density 16-bit Instruction Set**
- **Three-stage pipeline architecture**
  - **Instruction Fetch (F)**
  - **Instruction Decode (D)**
  - **Execute (E)**

7.2 Debug and Test Features

- **Integrated embedded in-circuit emulator**
  - **Two watchpoint units**
  - **Test access port accessible through a JTAG protocol**
  - **Debug communication channel**
- **Debug Unit**
  - **Two-pin UART**
  - **Debug communication channel interrupt handling**
  - **Chip ID and EXTended Chip ID Register**
- **IEEE1149.1 JTAG Boundary-scan on all digital pins, except reset, backup reset, and test pins**

7.3 Bus Matrix

- 6 Layers Matrix, handling requests from 6 masters
- Programmable Arbitration strategy
  - Fixed-priority Arbitration
  - Round-Robin Arbitration, either with no default master, last accessed default master or fixed default master
- Burst Management
  - Breaking with Slot Cycle Limit Support
  - Undefined Burst Length Support
- One Address Decoder provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal boot, one for external boot, one after remap
- Boot Mode Select
  - Non-volatile Boot Memory can be internal or external
  - Selection is made by BMS pin sampled at reset
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory
  - Allows Handling of Dynamic Exception Vectors

7.3.1 Matrix Masters

The Bus Matrix of the AT91CAP7 manages six Masters, which means that each master can perform an access concurrently with others, as long as the slave it accesses is available.

Each Master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decoding. There are four independent masters available for the Metal Programmable Block (MP Block).

Table 7-1. List of Bus Matrix Masters

Master 0	ARM7TDMI
Master 1	Peripheral DMA Controller
Master 2	MP Block Master A
Master 3	MP Block Master B
Master 4	MP Block Master C
Master 5	MP Block Master D

7.3.2 Matrix Slaves

The Bus Matrix of the AT91CAP7 manages ten Slaves. Each Slave has its own arbiter, thus allowing to program a different arbitration per Slave.

There are four independent slaves available for the Metal Programmable Block (MP Block).

Table 7-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM 96 Kbytes
Slave 1	Internal SRAM 64 Kbytes
Slave 2	Internal ROM 256 Kbytes
Slave 3	MP Block Slave A
Slave 4	MP Block Slave B
Slave 5	MP Block Slave C
Slave 6	MP Block Slave D
Slave 7	MP Block Slave for ARM control of AHB masters*
Slave 8	External Bus Interface
Slave 9	Peripheral Bridge

* **Note:** Slave7 may only be accessed by the ARM7TDMI master and can be used to access control and status registers for AHB master devices in the metal programmable block that do not also have APB connections for this purpose.

7.4 Peripheral DMA Controller

- Acting as one Matrix Master
- Allows data transfers from/to peripheral to/from any memory space without any intervention of the processor.
- Next Pointer Support, avoids strong real-time constraints on buffer management.
- 22 channels
  - Two for each USART

- Two for the Debug Unit
- Two for the Serial Peripheral Interface
- One for the Analog to Digital Converter (ADC)
- 13 for peripherals implemented in the Metal Programmable Block

8. Memories

8.1 Embedded Memories

- 256 Kbyte Fast ROM
  - Single Cycle Access at full matrix speed
- 96 Kbyte Fast SRAM
  - Single Cycle Access at full matrix speed
- 64 Kbyte Fast SRAM
  - Single Cycle Access at full matrix speed
- Two 4 Kbyte DPRAMs
  - Accessed from the Metal Programmable Block

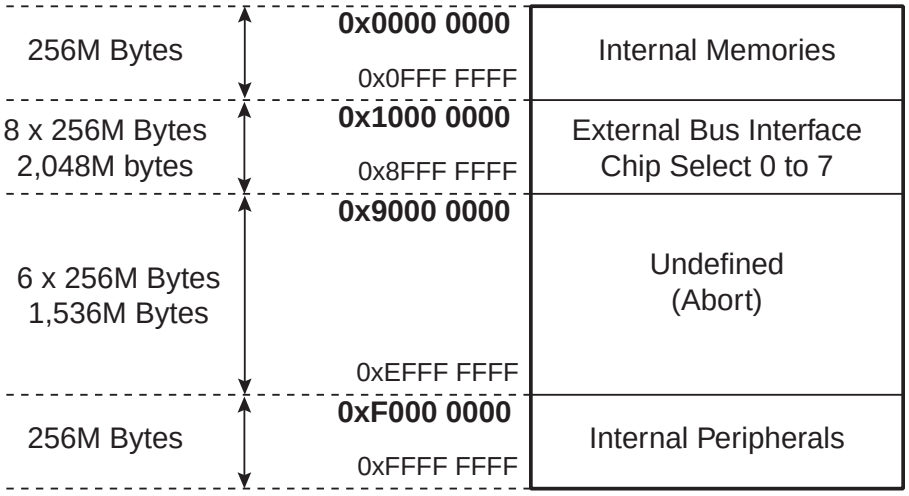
8.2 Memory Mapping

A first level of address decoding is performed by the Bus Matrix, i.e., the implementation of the Advanced High performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4G bytes of address space into 16 banks of 256M bytes. The banks 1 to 9 are directed to the EBI that associates these banks to the external chip selects NCS0 to NCS7. The bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1M byte of internal memory area. The bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

Figure 8-1. AT91CAP7 Product Memory Mapping



Each Master has its own bus and its own decoder, thus allowing a different memory mapping per Master. However, in order to simplify the mappings, all the masters have a similar address decoding.

Regarding Master 0 (ARM7TDMI), two different Slaves are assigned to the memory space decoded at address 0x0: one for internal boot and one for external boot.

8.3 Internal Memory Mapping

8.3.1 Internal 160-kBytes Fast SRAM

The AT91CAP7 embeds 160-Kbytes of high-speed SRAM configured in blocks of 96 KB and 64KB. When accessed from the AHB, each SRAM block is independently single cycle accessible at full matrix speed (MCK).

8.3.2 Boot Memory

The remappable memory area is between 0x0 and 0x000F FFFF.

If BMS is detected at logic 0, the boot memory is the memory connected on the Chip Select 0 of the External Bus Interface. The default configuration for the Static Memory Controller, byte select mode, 16-Bit data bus, Read/Write controlled by Chip Select, allows the device to boot on 16Bit nonvolatile memory.

If BMS is detected at logic 1, the boot memory is the embedded ROM.

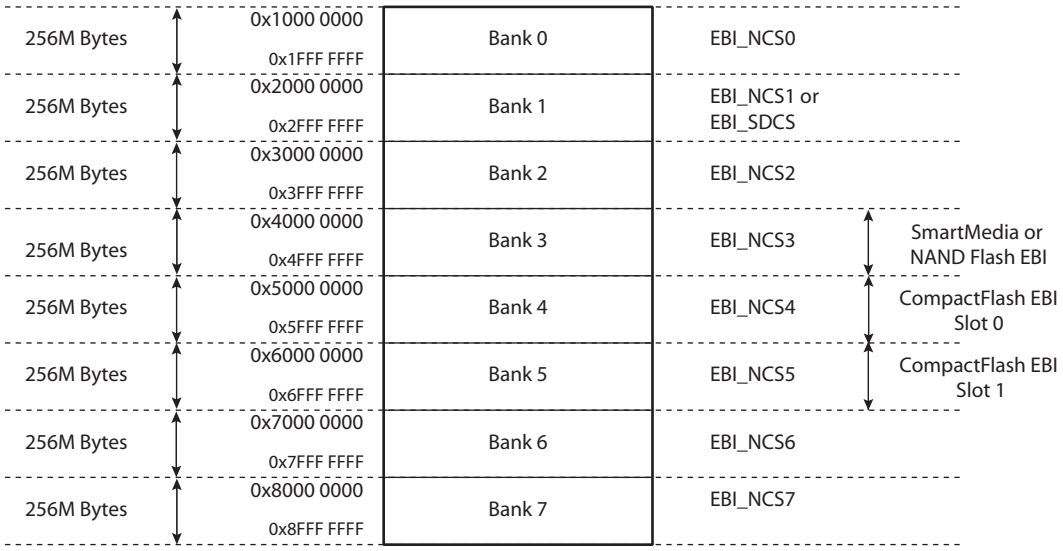
8.4 Boot Program

The internal 256 KB ROM is metal-programmable and each AT91CAP7 customer may develop their own boot program using their own code or a combination of their own code and routines available from Atmel.

8.5 External Memories Mapping

The external memories are accessed through the External Bus Interface. Each Chip Select line has a 256-MByte memory area assigned.

Figure 8-2. AT91CAP7 External Memory Mapping



8.6 External Bus Interface

- Optimized for Application Memory Space support
- Integrates two External Memory Controllers:
  - Static Memory Controller
  - SDRAM Controller
- Additional logic for NANDFlash and CompactFlash™
- Optional Full 32-bit External Data Bus
- Up to 26-bit Address Bus (up to 64MBytes linear per chip select)
- Up to 6 chips selects, Configurable Assignment:
  - Static Memory Controller on NCS0
  - SDRAM Controller or Static Memory Controller on NCS1
  - Static Memory Controller on NCS2
  - Static Memory Controller on NCS3, Optional NAND Flash support
  - Static Memory Controller on NCS4 - NCS5, Optional CompactFlash™ support

8.6.1 Static Memory Controller

- 8-, 16- or 32-bit Data Bus
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
  - Asynchronous read in Page Mode supported (4- up to 32-byte page size)
- Multiple device adaptability
  - Compliant with LCD Module
  - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request

  - Programmable Data Float Time
- Slow Clock mode supported

8.6.2 SDRAM Controller

- Supported devices:
  - Standard SDRAM
- Numerous configurations supported
  - **2K, 4K, 8K Row Address Memory Parts**
  - **SDRAM with two or four Internal Banks**
  - **SDRAM with 16- or 32-bit Data Path**
- Programming facilities
  - **Word, half-word, byte access**
  - **Automatic page break when Memory Boundary has been reached**
  - **Multi-bank Ping-pong Access**
  - **Timing parameters specified by software**
  - **Automatic refresh operation, refresh rate is programmable**
- **Energy-saving capabilities**
  - **Self-refresh, power down and deep power down modes supported**
- Error detection
  - **Refresh Error Interrupt**
- **SDRAM Power-up Initialization by software**
- **CAS Latency of 1, 2 and 3 supported**
- **Auto Precharge Command not used**

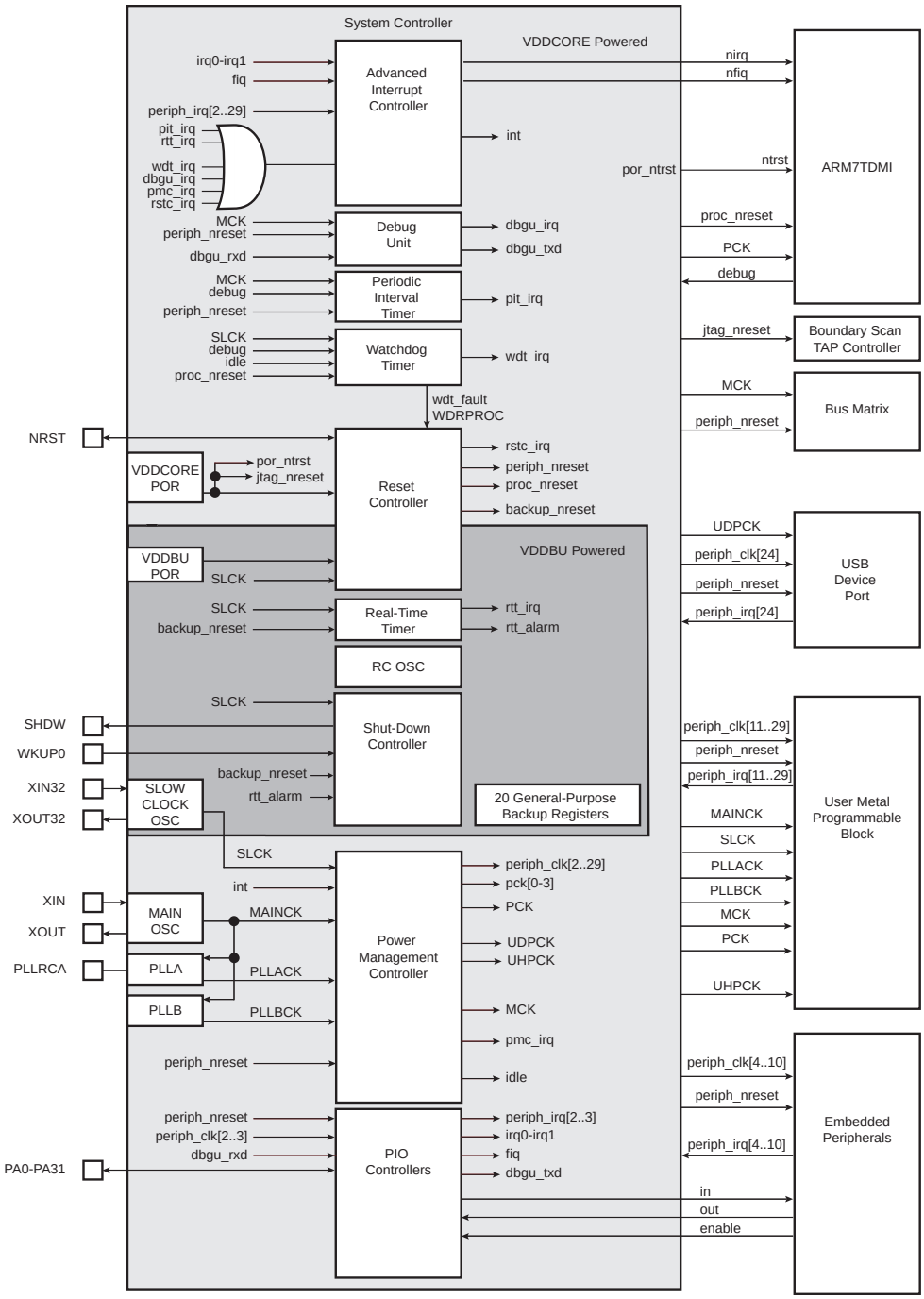
9. System Controller

The System Controller is a set of peripherals, which allow handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc.

The System Controller User Interface also includes control registers for configuring the AHB Matrix and the chip configuration. The chip configuration registers allow setting the EBI chip select assignment for external memories.

9.1 System Controller Block Diagram

Figure 9-1. AT91CAP7 System Controller Block Diagram

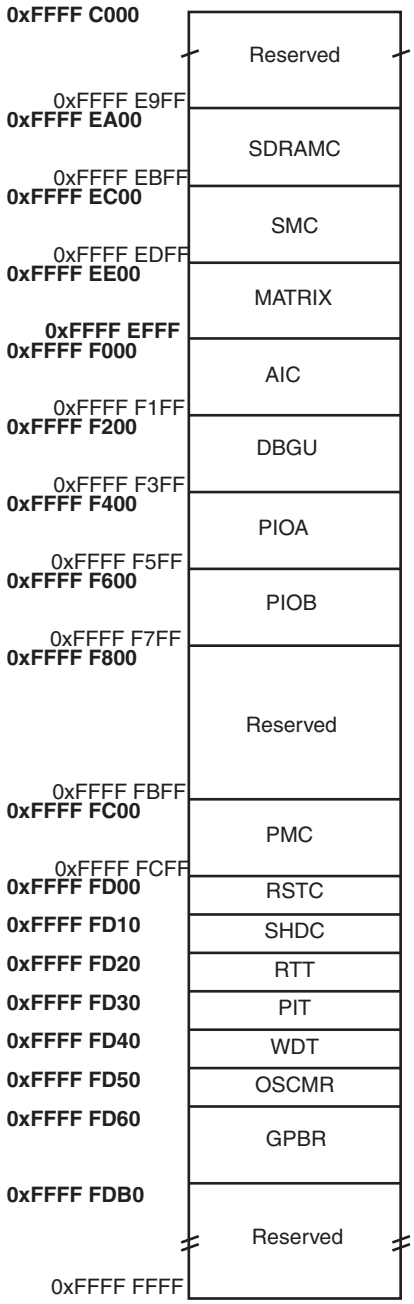


9.2 System Controller Mapping

The System Controller's peripherals are all mapped within the highest 16K bytes of address space, between addresses 0xFFFF C000 and 0xFFFF FFFF.

However, all the registers of System Controller are mapped on the top of the address space. This allows addressing all the registers of the System Controller from a single pointer by using the standard ARM instruction set since the Load/Store instructions have an indexing mode of +/- 4kbytes. Figure 9-2 shows where the User Interfaces for the System Controller peripherals fit into the memory map (relative to bus matrix and EBI (SMC, SDRAMC).

Figure 9-2. System Controller Mapping



Peripheral Name	Size
SDRAM Controller	512 bytes/128 words
Static Memory Controller	512 bytes/128 words
Matrix	512 bytes/128 words
Advanced Interrupt Controller	512 bytes/128 words
Debug Unit	512 bytes/128 words
Parallel I/O Controller A	512 bytes/128 words
Parallel I/O Controller B	512 bytes/128 words
Reserved	
Power Management Controller	512 bytes/128 words
Reset Controller	16 bytes/4 words
Shut-Down Controller	16 bytes/4 words
Real-Time Timer	16 bytes/4 words
Periodic Interval Timer	16 bytes/4 words
Watchdog Timer	16 bytes/4 words
Oscillator Mode Register	2 bytes/1 words (3words reserved)
General-Purpose Backup Registers	80 bytes/20 words
Reserved	

9.3 Reset Controller

- Based on two Power-on-Reset cells
  - one on VDDBU and one on VDDCORE
- Status of the last reset
  - Either general reset (VDDBU rising), wake-up reset (VDDCORE rising), software reset, user reset or watchdog reset
- Controls the internal resets and the NRST pin output
  - Allows shaping a reset signal for the external devices

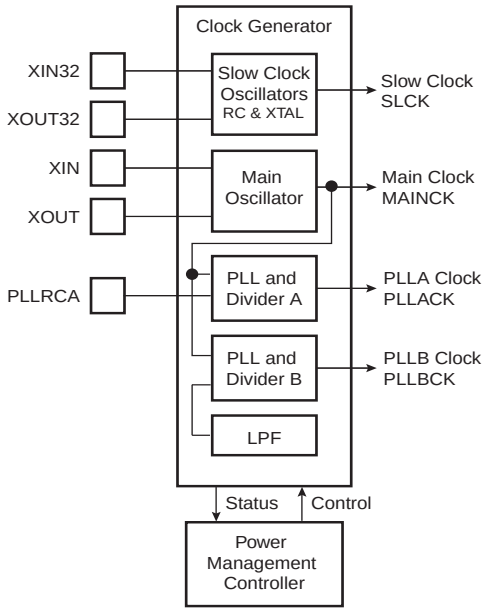
9.4 Shut Down Controller

- Shut-Down and Wake-Up logic
  - Software programmable assertion of the SHDW open-drain pin
  - De-assertion Programmable on a WKUP0 pin level change or on alarm

9.5 Clock Generator

- Embeds the Low Power, fast start-up 32kHz RC Oscillator
  - Provides the default Slow Clock SLCK to the system
  - The SLCK is required for AT91CAP7 to start-up because it is the default clock for the ARM7TDMI at power-up.
- Embeds the Low Power 32768Hz Slow Clock Oscillator
  - Requires an external 32768Hz crystal
  - Optional Slow Clock SLCK source when a real-time timebase is required
- Embeds the Main Oscillator
  - Requires an external crystal. For systems using the USB features, 12MHz is recommended.
  - Oscillator bypass feature
  - Supports 8 to 16MHz crystals. 12 MHz crystal is required if using the USB features of AT91CAP7.
  - Generates input reference clock for the two PLLs.
- Embeds PLLA primarily for generating processor and master clocks. For full-speed operation on the ARM7TDMI processor, this PLL should be programmed to generate a 160 MHz clock that must then be divided in half to generate the 80 MHz PCK and related clocks.
  - PLLA outputs an 80 to 240MHz clock
  - Requires an external RC filter network
  - PLLA has a 1MHz minimum input frequency
  - Integrates an input divider to increase output accuracy
- Embeds PLLB primarily for generating a 96 MHz clock that is divided down to generate the USB related clocks.
  - PLLB and its internal low-pass filter (LPF) are tuned especially for generating a 96 MHz clock with a 12 MHz input frequency
  - 12 MHz minimum input frequency
  - Integrates an input divider to increase output accuracy

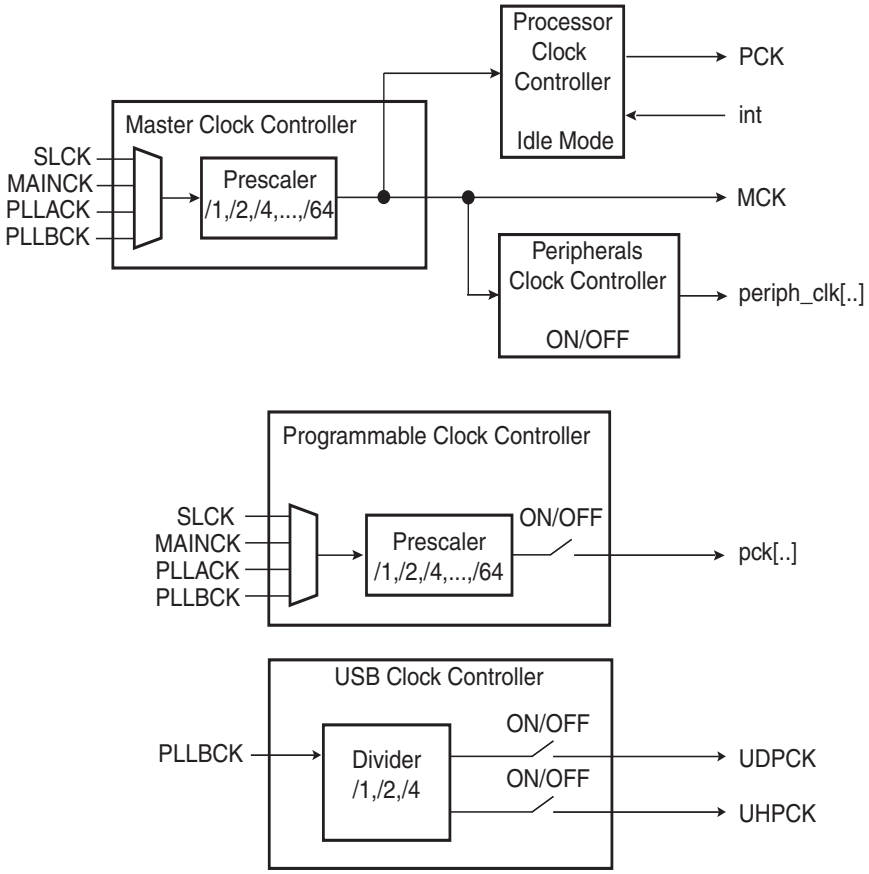
Figure 9-3. Clock Generator Block Diagram



9.6 Power Management Controller

- The Power Management Controller provides the following clocks as shown in Figure 7 below:
  - the Processor Clock PCK
  - the Master Clock MCK, in particular to the Matrix and the memory interfaces
  - the USB Device Clock UDPCK
  - independent peripheral clocks (periph_clk), typically at the frequency of MCK
  - four programmable clock outputs: PCK0 to PCK3
- Five flexible operating modes:
  - Normal Mode, processor and peripherals running at a programmable frequency
  - Idle Mode, processor stopped waiting for an interrupt
  - Slow Clock Mode, processor and peripherals running at low frequency
  - Standby Mode, mix of Idle and Backup Mode, peripheral running at low frequency, processor stopped waiting for an interrupt
  - Backup Mode, Main Power Supplies off, VDDBU and VDDOSC32 on

Figure 9-4. AT91CAP7 Power Management Controller Block Diagram



9.7 Periodic Interval Timer

- Includes a 20-bit Periodic Counter
- Includes a 12-bit Interval Overlay Counter
- Real Time OS or Linux/WinCE compliant tick generator

9.8 Watchdog Timer

- 16-bit key-protected only-once-Programmable Counter
- Windowed, prevents the processor to be in a dead-lock on the watchdog access

9.9 Real-Time Timer

- One Real-Time Timer, allowing backup of time
  - 32-bit Free-running, back-up Counter
  - Integrates a 16-bit programmable prescaler running on the embedded 32.768Hz oscillator
  - Alarm Register capable to generate a wake-up of the system through the Shut Down Controller

9.10 General-Purpose Backed-up Registers

- Twenty 32-bit backup general-purpose registers

9.11 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of the ARM Processor
- Thirty-two individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (PIT, RTT, PMC, DBGU, etc.)
  - Programmable Edge-triggered or Level-sensitive Internal Sources
  - Programmable Positive/Negative Edge-triggered or High/Low Level-sensitive
- Two External Sources plus the Fast Interrupt signal
- 8-level Priority Controller
  - Drives the Normal Interrupt of the processor
  - Handles priority of the interrupt sources 1 to 31
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes Interrupt Service Routine Branch and Execution
  - One 32-bit Vector Register per interrupt source
  - Interrupt Vector Register reads the corresponding current Interrupt Vector
- Protect Mode
  - Easy debugging by preventing automatic operations when protect models are enabled
- Fast Forcing
  - Permits redirecting any normal interrupt source on the Fast Interrupt of the processor

9.12 Debug Unit

- Composed of two functions
  - Two-pin UART
  - Debug Communication Channel (DCC) support
- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Support for two PDC channels with connection to receiver and transmitter
- Debug Communication Channel Support
  - Offers visibility of and interrupt trigger from COMMRX and COMMTX signals from the ARM Processor's ICE Interface

9.13 Chip Identification

- Chip ID: 837709xx (0x1000 0011 0111 0111 0000 1001 010x xxxx). This value is stored in the Chip ID Register (DBGU_CIDR) in the Debug Unit. The last 5 bits of the register are reserved for a chip version number.

This module contains two 32 bit wide hardware registers which are mapped into three fields:

cap7_version - CAP7 platform hardware version (DBGU_EXID[31:30], DBGU_CIDR[4:0])

cap7_id - Defines device to debugger software (DBGU_CIDR[31:5])

mp_chip_id - user defined value for MP customization (DBGU_EXID[29:0])

- Ext Chip ID: Bits 29:0 are MPBlock programmable. Bits 31:30 are resevered.
- JTAG ID: unique for each CAP7 personalization.

9.14 PIO Controllers

- One PIO Controller (PIOA) included.
- Optionally, as many as 3 additional PIO controllers may be added to the MPBlock.
- Each PIO Controller controls up to 32 programmable I/O Lines
  - PIOA controls 32 I/O Lines (PA0 - PA31)
  - PIOB can control up to 32 of the MPIO Lines
- Fully programmable through Set/Clear Registers
- Multiplexing of two peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
  - Input change interrupt
  - Glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

9.15 User Interface

9.15.1 Special System Controller Register Mapping

Table 9-1. Special System Controller Registers

Offset	Register	Name	Access	Reset Value
0x50	Oscillator Mode Register	SYSC_OSCMR	Read/Write	0x1
0x60	General Purpose Backup Register 1	SYSC_GPBR1	Read/Write	0x0
---	---	---	---	---
0xAC	General Purpose Backup Register 20	SYSC_GPBR20	Read/Write	0x0

9.15.2 Oscillator Mode Register

Register Name: SYSC_OSCMR

Access Type: Read/Write

Reset Value: 0x00000001

31	30	29	28	27	26	25	24
–	–	–	–	–	–	–	–

23	22	21	20	19	18	17	16
–	–	–	–	–	–	–	–

15	14	13	12	11	10	9	8
–	–	–	–	–	–	–	–

7	6	5	4	3	2	1	0
–	–	–	–	OSC32K_SEL	–	OSC32K_XT_EN	OSC32K_RC_EN

- **OSC32K_RC_EN: Enable internal RC oscillator**

0: No effect.

1: Enables the internal RC oscillator [enabled out of reset indicating system starts off of RC]

- **OSC32K_XT_EN: Enable external crystal oscillator**

0: No effect.

1: Enables the external crystal oscillator

- **OSC32K_SEL: Slow clock source select**

0: Selects internal RC as source of slow clock

1: Selects external crystal and source of slow

NOTE: After setting the OSC32K_XT_EN bit, wait the 32 kHz Crystal Oscillator Startup Time (see table 34-5) on slow clock timing before setting the OSC32K_SEL bit.

9.15.3 General Purpose Backup Register

Register Name: SYSC_GPBRx

Access Type: Read/Write

Reset Value: 0x0

31	30	29	28	27	26	25	24
GPBRx							
23	22	21	20	19	18	17	16
GPBRx							
15	14	13	12	11	10	9	8
GPBRx							
7	6	5	4	3	2	1	0
GPBRx							

- **GPBRx: General Purpose Backup Register**

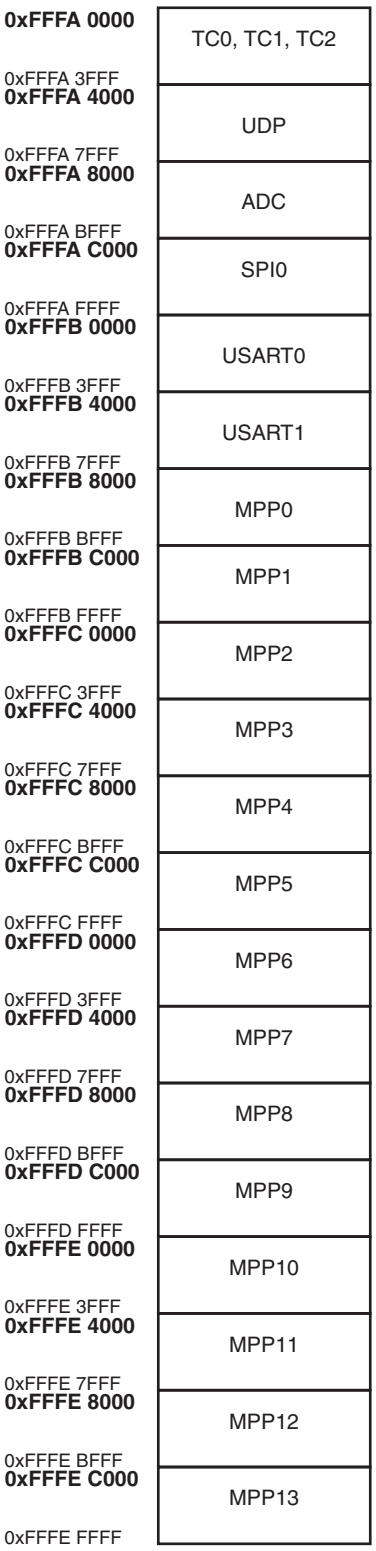
These are user programmable registers that are powered by the backup power supply (VDDBU).

10. Peripherals

10.1 Peripheral Mapping

Both the standard peripherals and any APB peripherals implemented in the MPBlock are mapped in the upper 256M bytes of the address space between the addresses 0xFFFA 0000 and 0xFFFE FFFF. Each User Peripheral is allocated 16K bytes of address space as shown below in Figure 10-1.

Figure 10-1. AT91CAP7 Peripheral Mapping



Peripheral Name	Size
Timer/Counter 0, 1 and 2	16K Bytes
USB Device Port	16K Bytes
Analog to Digital Converter	16K Bytes
Serial Peripheral Interface 0	16K Bytes
Universal Synchronous Asynchronous Receiver Transmitter 0	16K Bytes
Universal Synchronous Asynchronous Receiver Transmitter 1	16K Bytes
MP Block Peripheral 0	16K Bytes
MP Block Peripheral 1	16K Bytes
MP Block Peripheral 2	16K Bytes
MP Block Peripheral 3	16K Bytes
MP Block Peripheral 4	16K Bytes
MP Block Peripheral 5	16K Bytes
MP Block Peripheral 6	16K Bytes
MP Block Peripheral 7	16K Bytes
MP Block Peripheral 8	16K Bytes
MP Block Peripheral 9	16K Bytes
MP Block Peripheral 10	16K Bytes
MP Block Peripheral 11	16K Bytes
MP Block Peripheral 12	16K Bytes
MP Block Peripheral 13	16K Bytes

10.2 Peripheral Identifiers

The AT91CAP7 embeds some of the most common peripherals. Additional peripherals can be implemented in the Metal Programmable Block as required by the customer. The table below defines the Peripheral Identifiers of the AT91CAP7. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 10-1. AT91CAP7 Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSC	System Controller	
2	PIOA	Parallel I/O Controller A	
3	PIOB	Optional Parallel I/O Controller B	
4	US0	USART 0	
5	US1	USART 1	
6	SPI0	Serial Peripheral Interface 0	
7	TC0	Timer/Counter 0	
8	TC1	Timer/Counter 1	
9	TC2	Timer/Counter 2	
10	UDP	USB Device Port	
11	ADC	Analog to Digital Converter	
12	MPP0	Metal Programmable Block Peripheral 0	
13	MPP1	Metal Programmable Block Peripheral 1	
14	MPP2	Metal Programmable Block Peripheral 2	
15	MPP3	Metal Programmable Block Peripheral 3	
16	MPP4	Metal Programmable Block Peripheral 4	
17	MPP5	Metal Programmable Block Peripheral 5	
18	MPP6	Metal Programmable Block Peripheral 6	
19	MPP7	Metal Programmable Block Peripheral 7	
20	MPP8	Metal Programmable Block Peripheral 8	
21	MPP9	Metal Programmable Block Peripheral 9	
22	MPP10	Metal Programmable Block Peripheral 10	
23	MPP11	Metal Programmable Block Peripheral 11	
24	MPP12	Metal Programmable Block Peripheral 12	
25	MPP13	Metal Programmable Block Peripheral 13	
26	MPMA	Metal Programmable Block Master A	
27	MPMB	Metal Programmable Block Master B	
28	MPMC	Metal Programmable Block Master C	

Table 10-1. AT91CAP7 Peripheral Identifiers (Continued)

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
29	**MPMD**	Metal Programmable Block Master D	
30	**AIC**	Advanced Interrupt Controller	IRQ0
31	**AIC**	Advanced Interrupt Controller	IRQ1

10.3 Peripheral Interrupts and Clock Control

10.3.1 System Interrupt

The System Interrupt in Source 1 is the wired-OR of the interrupt signals coming from:

- the SDRAM Controller
- the Debug Unit
- the Periodic Interval Timer
- the Real-Time Timer
- the Watchdog Timer
- the Reset Controller
- the Power Management Controller

The clock of these peripherals cannot be deactivated and Peripheral ID 1 can only be used within the Advanced Interrupt Controller.

10.3.2 External Interrupts

All external interrupt signals, i.e., the Fast Interrupt signal FIQ or the Interrupt signals IRQ0 to IRQ1, use a dedicated Peripheral ID. However, there is no clock control associated with these peripheral IDs.

10.3.3 Timer Counter Interrupts

The three Timer Counter channels interrupt signals are OR-wired together to provide the interrupt source 7 of the Advanced Interrupt Controller. This forces the programmer to read all Timer Counter status registers before branching the right Interrupt Service Routine.

The Timer Counter channels clocks cannot be deactivated independently. Switching off the clock of the Peripheral 7 disables the clock of the 3 channels.

10.4 Peripherals Signals Multiplexing on I/O Lines

The AT91CAP7 features up to two PIO controllers, PIOA which multiplexes the I/O lines of the standard peripheral set and the optional PIOB which can multiplex I/O for any peripherals or user logic included in the MPBlock.

Each PIO Controller controls up to 32 lines. Each line can be assigned to one of two peripheral functions, A or B. The multiplexing tables in the following paragraphs define how the I/O lines of the peripherals A and B are multiplexed on PIOA.

The column “Reset State” indicates whether the PIO Line resets in I/O mode or in peripheral mode. If I/O is listed, the PIO Line resets in input mode with the pull-up enabled, so that the device is maintained in a static state as soon as the reset is released. As a result, the bit corresponding to the PIO Line in the register PIO_PSR (Peripheral Status Register) resets high.

If a signal name is listed in the “Reset State” column, the PIO Line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case of pins controlling memories, in particular the address lines, which require the pin to be driven as soon as the reset is released. Note that the pull-up resistor is also enabled in this case.

10.4.1 PIO Controller A Multiplexing

Table 10-2. Multiplexing on PIO Controller A

PIO Controller A			
I/O Line	**Peripheral A**	**Peripheral B**	**Reset State**
PA0	FIQ	DBG_DRXD	I/O
PA1	NWAIT	DBG_DTXD	I/O
PA2	NCS4/CFCS0	USART0_SCK0	I/O
PA3	CFCE1	USART0_RTS0	I/O
PA4	A25/CFRNW	USART0_CTS0	Periph driven low with pullup enabled
PA5	NANDOE	USART0_TXD0	I/O
PA6	NANDWE	USART0_RXD0	I/O
PA7	NCS6	SPI_MISO	I/O
PA8	NCS7	SPI_MOSI	I/O
PA9	ADTRG	SPI_SPCK	I/O
PA10	IRQ0	SPI_NPCS0	I/O
PA11	IRQ1	SPI_NPCS1	I/O
PA12	NCS5/CFCS1	SPI_NPCS2	I/O
PA13	CFCE2	SPI_NPCS3	I/O
PA14	A23	APMC_PCK0	Periph A, driven low with pullup enabled
PA15	A24	APMC_PCK1	Periph A, driven low with pullup enabled
PA16	D16	APMC_PCK2	I/O
PA17	D17	APMC_PCK3	I/O
PA18	D18	USART1_SCK1	I/O
PA19	D19	USART1_RTS1	I/O
PA20	D20	USART1_CTS1	I/O
PA21	D21	USART1_TXD1	I/O
PA22	D22	USART1_RXD1	I/O
PA23	D23	TIMER0_TCLK0	I/O
PA24	D24	TIMER1_TCLK1	I/O
PA25	D25	TIMER2_TCLK2	I/O
PA26	D26	TIMER0_TIOA0	I/O
PA27	D27	TIMER0_TIOB0	I/O
PA28	D28	TIMER1_TIOA1	I/O

Table 10-2. Multiplexing on PIO Controller A

PIO Controller A			
I/O Line	**Peripheral A**	**Peripheral B**	**Reset State**
PA29	D29	TIMER1_TIOB1	
PA30	D30	TIMER2_TIOA2	
PA31	D31	TIMER2_TIOB2	

10.4.2 PIO Controller B Multiplexing

If implemented, the PIOB Port is dedicated fully to the MPBlock, and its multiplexing is determined by the MPBlock “personality.”

10.4.3 Resource Multiplexing

10.4.3.1 EBI

If not required, the NWAIT function (external wait request) can be deactivated by software allowing this pin to be used as a PIO. Use of the NWAIT function prevents use of the Debug Unit.

10.4.3.2 32-bit Data Bus

Using a 32-bit Data Bus prevents:

- using the three Timer Counter channels’ outputs and trigger inputs
- using the USART1
- using two of the clock outputs (APMC_PCK2 and APMC_PCK3)

10.4.3.3 NAND Flash Interface

Using the NAND Flash interface prevents using the NCS3 and USART0.

10.4.3.4 Compact Flash Interface

Using the CompactFlash interface prevents using the USART0.

10.4.3.5 SPI

Using the SPI prevents use of NCS6, NCS7, and the ADC external trigger.

10.4.3.6 USARTs

Using the USART0 prevents use of CompactFlash or NAND Flash.

Using the USART1 prevents using a full 32-bit bus for the EBI.

10.4.3.7 Clock Outputs

Using the clock outputs prevents use of either higher EBI address bits or a full 32-bit data bus (see table 10-2).

10.4.3.8 Interrupt Lines

Using FIQ prevents using the Debug Unit.

Using IRQ0 prevents the use of SPI_NPCS0.

Using IRQ1 prevents the use of SPI_NPCS1.

10.5 Embedded Peripherals Overview

10.5.1 Serial Peripheral Interface

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

10.5.2 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection
  - MSB-first or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter time-guard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

10.5.3 Timer Counter

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

10.5.4 USB Device Port

- USB V2.0 full-speed compliant, 12 MBits per second
- Embedded USB V2.0 full-speed transceiver
- Embedded 2,432-byte dual-port RAM for endpoints
- Suspend/Resume logic
- Ping-pong mode (two memory banks) for isochronous and bulk endpoints
- Six general-purpose endpoints
  - Endpoint 0 and 3: 64 bytes, no ping-pong mode
  - Endpoint 1 and 2: 64 bytes, ping-pong mode
  - Endpoint 4 and 5: 512 bytes, ping-pong mode

10.5.5 Analog to Digital Converter

- 10-bit Successive Approximation Register (SAR) ADC based on thermometric-resistive
- Up to 440 kSamples/sec.
- Up to 8 independent analog input channels
- Low active power: < 2 mW
- Low power stand-by mode
- External voltage reference of 2.6V to analog supply for better accuracy
- ± 2LSB Integral Non-Linearity (INL), ± 0.9 LSB Differential Non-Linearity (DNL)
- Individual enable and disable of each channel
- Multiple trigger sources:
  - Hardware or software trigger
  - External trigger pin
- Sleep Mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels

11. Metal-Programmable Block

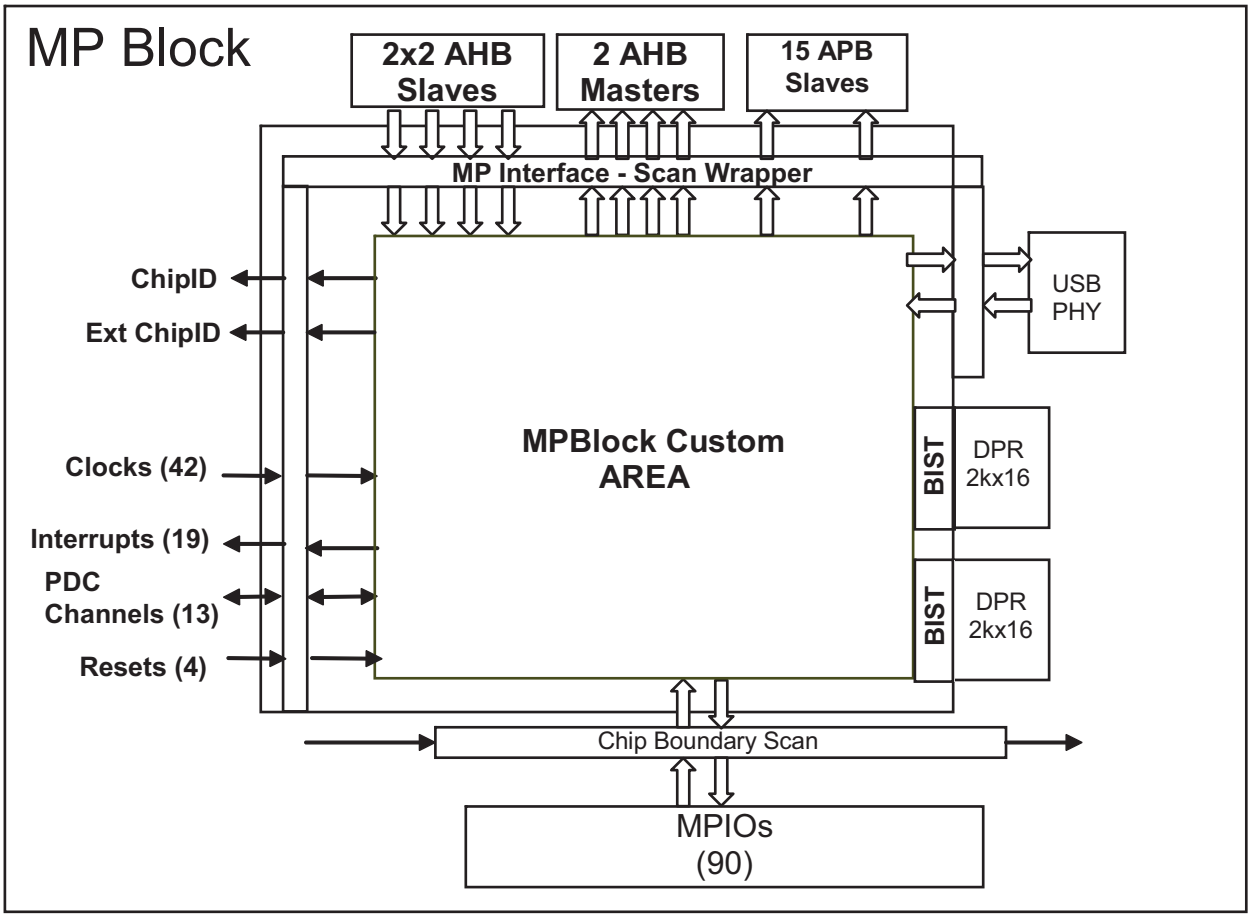
The Metal Programmable Block (MPBlock) is connected to internal resources such as the AHB bus or Advanced Interrupt Controller and external resources such as dedicated I/O pads or a PIO controller.

The MPBlock may be used to implement Advanced High-speed Bus (AHB) or Advanced Peripheral Bus (APB) custom peripherals. The MPBlock provides approximately 200K gates of standard cell custom logic for the addition of user IP to the AT91CAP7 implementation. Each custom metal mask set for the MPBlock can be referred to as a “personality.”

11.1 Internal Connectivity

In order to connect the MPBlock custom peripherals to the AT91CAP7 platform design, various connections to the MPBlock are provided as shown in the figure and described below.

Figure 11-1. MP Block Interface Diagram



11.1.1 AHB Master Buses

The CAP7L MPBlock may implement up to two independent AHB masters each having a dedicated AHB master bus connected to the AHB Matrix.

11.1.2 AHB Slave Buses

The CAP7L MPBlock receives two independent AHB slave buses coming from the AHB Matrix. Each bus has four select signals allowing up to 8 AHB slaves to be implemented in the MPBlock.

11.1.3 Clocks

The MPBlock receives a total of 42 clocks including the following:

32768 Hz Slow Clock

8-16 MHz Main Oscillator Clock

PLLA Clock

PLLB Clock

12 and 48 MHz USB Host Clock (UHPCK) for optional full-speed USB Host Port in MPBlock

MCK System Clock

PCK System Clock

14 gated APB peripheral clocks for use by Peripherals with ID 12 to 25, including 1 dedicated Peripheral and Configuration clock for an additional PIO controller.

4 gated clocks (for AHB masters) associated with ID 26 to 29.

11.1.4 Interrupts

The MPBlock is connected to 19 interrupt lines corresponding to Peripheral ID 11 to 29.

11.1.5 Peripheral DMA Channels

The MPBlock is connected to 13 channels of the Peripheral DMA Controller; 5 read channels, 5 write channels, 3 read/write channel.

11.2 External Connectivity

The MPBlock is connected to the following external resources.

11.2.1 PIO Controller B

The MPBlock may instantiate one 32-bit wide PIO Controller (PIOB) and connect any available signals to the alternate functions A and B of PIOB allowing the addition of up to 32 simultaneous custom I/O and up to 64 custom I/O connections.

11.2.2 Dedicated I/O

The MPBlock is directly connected to up to 90 dedicated I/O Pads with the following features:

Pull-up, Pull-down, bus holder Control Pins

The number of dedicated I/O's for the MPBlock is determined by the package selection.

11.3 Prototyping Solution

Customer's CAP7-based designs can be prototyped using the Atmel AT91CAP7X-DK (Development Kit) using a AT91CAP7S emulation-enabled CAP7 device and a Xilinx Virtex-IV XC4LX80-FFG1148 FPGA. User logic can be added to this large FPGA and debugged using standard software development tools and JTAG-enabled, In-Circuit Emulation (ICE devices).

12. AT91CAP7L Ordering Information

Table 12-1. AT91CAP7L Ordering Information

Ordering Code	Package	Package Type	Temperature Operating Range
AT91CAP7L200A-CJ	BGA225	RoHS Compliant	Industrial -40°C to 85°C

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
CAP@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature

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