ACT–F2M32A High Speed 64 Megabit Sector Erase FLASH Multichip Module

AEROFLEX CIRCUIT TECHNOLOGY
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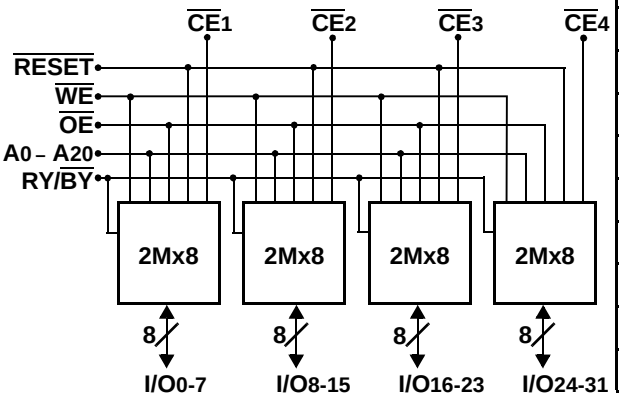
Features

- 4 Low Voltage/Power AMD 2M x 8 FLASH Die in One MCM Package
- Overall Configuration is 2M x 32
- +5V Power Supply / +5V Programing Operation
- Access Times of 90, 120 and 150 ns
- Erase/Program Cycles – 100,000 Minimum
- Sector erase architecture (Each Die)
  - 32 uniform sectors of 64 Kbytes each
  - Any combination of sectors can be erased. Also supports full chip erase
  - Sector group protection is user definable
- Embedded Erase Algorithims – Automatically pre-programs and erases the die or any sector
- Embedded Program Algorithims – Automatically programs and verifies data at specified address
- Ready/$\overline{\text{Busy}}$ output (RY/$\overline{\text{BY}}$) – Hardware method for detection of program or erase cycle completion
- Hardware $\overline{\text{RESET}}$ pin – Resets internal state machine to the read mode
- Erase Suspend/Resume – Supports reading or programming data to a sector not being erased
- Packaging – Hermetic Ceramic
  - 68 Lead, .94" x .94" x .140" Single-Cavity Small Outline Gull Wing, Aeroflex code# "F18" *(Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)*
- Internal Decoupling Capacitors for Low Noise Operation
- Commercial, Industrial and Military Temperature Ranges
- MIL-PRF-38534 Compliant MCMs Available

Block Diagram – CQFP(F18)

Standard Configuration

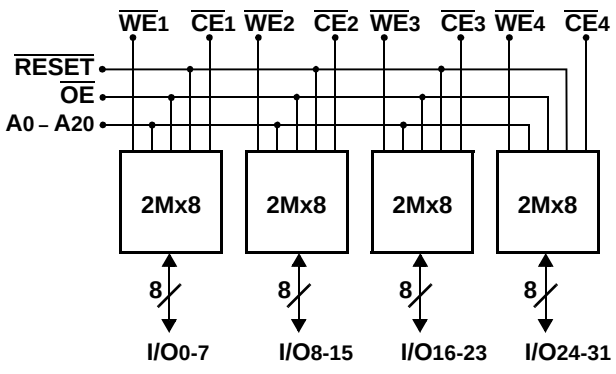


Pin Description

I/O0-31	Data I/O
A0–20	Address Inputs
$\overline{\text{WE}}$	Write Enables
$\overline{\text{CE}}$1-4	Chip Enables
$\overline{\text{OE}}$	Output Enable
RY/$\overline{\text{BY}}$	Ready/$\overline{\text{Busy}}$
$\overline{\text{RESET}}$	Reset
VCC	Power Supply
GND	Ground
NC	Not Connected

Block Diagram – CQFP(F18)

Optional Configuration



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VCC	Power Supply
GND	Ground
NC	Not Connected

General Description

Utilizing AMD's Sector Erase Flash Memory Die, the ACT-F2M32A is a high speed, 64 megabit CMOS flash multichip module (MCM) designed for full temperature range, military, space, or high reliability applications.

The ACT-F2M32A consists of four high-performance AMD Am29F016 16Mbit (16,777,216 bit) memory die. Each die contains 8 separately write or erase sector groups of 256Kbytes (A sector group consists of 4 adjacent sectors of 64Kbytes each).

The command register is written by bringing $\overline{\text{WE}}$ to a logic low level (V_{IL}), while $\overline{\text{CE}}$ is low and $\overline{\text{OE}}$ is high (V_{IH}). Reading is accomplished by chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) being logically active. Access time grades of 90ns, 120ns and 150ns maximum are standard.

General Description, Cont'd,

The ACT-F2M32A is packaged in a hermetically sealed co-fired ceramic 68 lead, .94" SQ Ceramic Gull Wing CQFP package. This allows operation in a military environment temperature range of -55°C to +125°C.

The ACT-F2M32A can be programmed (both read and write functions) in-system using the +5.0V V_{CC} power supply. A 12.0V V_{PP} is not required for programming or erase operations. The end of program or erase is detected by the RY/$\overline{BY}$ pin, Data Polling of DQ7, or by the Toggle bit (DQ6).

The ACT-F2M32A also has a hardware $\overline{RESET}$ pin. When this pin is driven low, execution of any Embedded Program Alggorithm or Embedded Erase Algorithm will be terminated.

Each block can be independently erased and programmed 100,000 times at +25°C.

For Detail Information regarding the operation of the Am29F016 Sector Erase Flash Memory, see the AMD datasheet (Publication 18805).

Absolute Maximum Ratings

Parameter	Range	Units
Case Operating Temperature Range	-55 to +125	°C
Storage Temperature Range	-65 to +150	°C
Voltage with Respect to GND (All pins except A9) (1)	-2.0 to +7.0	V
Voltage on Pins A9, $\overline{OE}$, $\overline{RESET}$ (2)	-2.0 to +13.5	V
Vcc Supply Voltage with Respect to Ground (1)	-2.0 to +7.0	V
Output Short Circuit Current (3)	200	mA

Notes:
1. Minimum DC voltage is -0.5V on input/output pins. During Transitions, inputs may undershoot GND to -2.0V for periods up to 20ns. Maximum DC voltage on input/output pins is V_{CC} + 0.5V, which may overshoot to V_{CC} + 2.0V for periods up to 20ns.
2. Minimum DC input voltage on A9 ,$\overline{OE}$, $\overline{RESET}$ pins is -0.5V. During Voltage transitions, A9, $\overline{OE}$ & $\overline{RESET}$ may overshoot GND to -2.0V for periods up to 20ns. Maximum DC input voltage on A9 is +12.5V which may overshoot to 14V for periods up to 20ns.
3. No more than one output shorted to ground for no more than 1 second.

NOTICE: Stresses above those listed under "Absolute Maximums Rating" may cause permanent damage to the device. These are stress rating only; functional operation beyond the "Operation Conditions" is not recommended and extended exposure beyond the "Operation Conditions" may effect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	5V Power Supply Voltage (10%)	+4.5	+5.5	V
V_{IH}	Input High Voltage (CMOS)	0.7 x V_{CC}	V_{cc} + 0.3	V
V_{IL}	Input Low Voltage	-0.5	+0.8	V
T_C	Operating Temperature (Military)	-55	+125	°C

Capacitance

(f = 1MHz, T_C = 25°C, Standard Configuration)

Symbol	Parameter	Maximum	Units
C_{AD}	A0 – A20 Capacitance	50	pF
C_{OE}	$\overline{OE}$ Capacitance	50	pF
C_{CE}	$\overline{CE}$ Capacitance	20	pF
C_{RESET}	$\overline{RESET}$ Capacitance	50	pF
C_{WE}	$\overline{WE}$ Capacitance	60	pF
$C_{RY/\overline{BY}}$	RY/$\overline{BY}$ Capacitance	50	pF
$C_{I/O}$	I/O0 – I/O31 Capacitance	20	pF

Capacitance Guaranteed by design, but not tested.

DC Characteristics – CMOS Compatible

(T_C = -55°C to +125°C, V_{CC} = +4.5V to + 5.5V, Unless otherwise specified)

Parameter	Sym	Conditions	Min	Max	Units
Input Load Current	I_{IL}	V_{CC} = V_{CC}Max., V_{IN} = V_{CC} or GND		10	µA
A9 Leakage Current	I_{LIT}	V_{CC} = V_{CC}Max., A9 = +12V		50	µA
Output Leakage Current	I_{LO}	V_{CC} = V_{CC}Max., V_{IN} = GND to V_{CC}		10	µA
Vcc Active Read Current	I_{CC1}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		160	mA
Vcc Active Program/Erase Current (1)	I_{CC2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		240	mA
Vcc Standby Current	I_{CC3}	V_{CC} = V_{CC}Max., $\overline{CE}$ = $\overline{RESET}$ = V_{CC} ± 0.3V		4	mA
Vcc Standby Current (Reset)	I_{CC4}	V_{CC} = V_{CC}Max., $\overline{RESET}$ = V_{CC} ± 0.3V		4	mA
Output Low Voltage	V_{OL}	V_{CC} = V_{CC}Min., I_{OL} = 12 mA		0.45	V
Output High Voltage	V_{OH1}	V_{CC} = V_{CC}Min., I_{OH} = -2.5 mA	0.85 x V_{CC}		V
	V_{OH2}	V_{CC} = V_{CC}Min., I_{OH} = -100 µA	V_{CC} - 0.4V		V
Low V_{CC} Lock-Out Voltage	V_{LKO}		3.2	4.2	V

Notes:
1. Not 100% tested.

AC Characteristics – Write/Erase/Program Operations – $\overline{WE}$ Controlled

(T_C = -55°C to +125°C, V_{CC} = +4.5V to + 5.5V, Unless otherwise specified)

Parameter		Parameter Symbol Standard	Parameter Symbol JEDEC	90ns		120ns		150ns		Units
				Min	Max	Min	Max	Min	Max	
Write Cycle Time		t_{WC}	t_{AVAV}	90		120		150		ns
Address Setup to $\overline{WE}$ Going Low		t_{AS}	t_{AVWL}	0		0		0		ns
Address Hold Time from $\overline{CE}$ High		t_{AH}	t_{WLAX}	45		50		50		ns
Data Setup to $\overline{WE}$ Going High		t_{DS}	t_{DVWH}	45		50		50		ns
Data Hold Time from $\overline{WE}$ High		t_{DH}	t_{WHDX}	0		0		0		ns
Output Enable Hold Time	Read	t_{OEH}		0		0		0		ns
	Toggle Bit I and $\overline{Data}$ Polling			10		10		10		ns
Read Recover Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		t_{GHWL}	t_{GHWL}	0		0		0		ns
$\overline{CE}$ Setup Time from $\overline{WE}$ Low		t_{CS}	t_{ELWL}	0		0		0		ns
$\overline{CE}$ Hold Time from $\overline{WE}$ High		t_{CH}	t_{WHEH}	0		0		0		ns
$\overline{WE}$ Pulse Width		t_{WP}	t_{WLWH}	45		50		50		ns
$\overline{WE}$ Pulse Width High		t_{WPH}	t_{WHWL}	20		20		20		ns
Byte Programming Operation		t_{WHWH1}	t_{WHWH1}	8		8		8		µs
Sector Erase Operation		t_{WHWH2}	t_{WHWH2}		15		15		15	Sec
V_{CC} Set-Up Time		t_{VCS}		50		50		50		µs
Rise Time to V_{ID}		t_{VIDR}		500		500		500		ns
$\overline{OE}$ Setup Time to $\overline{WE}$ Active		t_{OESP}		4		4		4		µs
$\overline{Reset}$ Pulse Width		t_{RP}		500		500		500		ns
Program/Erase Valid to RY/$\overline{BY}$ Delay		t_{BUSY}		40		50		60		ns

Notes:
1. Not 100% tested.

AC Characteristics – Read Only Operations

(T_C = -55°C to +125°C, V_{CC} = +4.5V to + 5.5V, Unless otherwise specified)

Parameter	Parameter Symbol Standard	Parameter Symbol JEDEC	90ns		120ns		150ns		Units
			Min	Max	Min	Max	Min	Max	
Read Cycle Time (1)	t_{RC}	t_{AVAV}	90		120		150		ns
Address to Output Delay	t_{ACC}	t_{AVQV}		90		120		150	ns
$\overline{CE}$ to Output Delay	t_{CE}	t_{ELQV}		90		120		150	ns
$\overline{OE}$ to Output Delay	t_{OE}	t_{GLQV}		40		50		55	ns
$\overline{CE}$ to Output in High Z (1)	t_{DF}	t_{EHQZ}		20		30		35	ns
$\overline{OE}$ to Output in High Z (1)	t_{DF}	t_{GHQZ}		20	0	30	0	35	ns
Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change, Whichever Occurs First	t_{OH}	t_{AXQX}	0		0		0		ns
$\overline{RESET}$ Low to Read Mode (1)	t_{READY}			20		20		20	µs

Notes:
1. Not 100% tested.

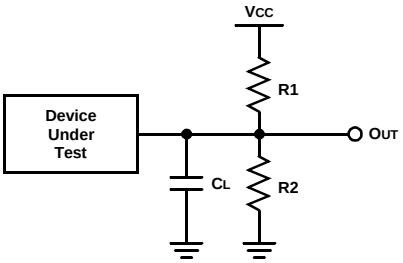
AC Characteristics – Write/Erase/Program Operations – $\overline{CE}$ Controlled

(Tc = -55°C to +125°C, Vcc = +4.5V to + 5.5V, Unless otherwise specified)

Parameter		Parameter Symbol Standard	Parameter Symbol JEDEC	90ns		120ns		150ns		Units
				Min	Max	Min	Max	Min	Max	
Write Cycle Time (1)		t_{WC}	t_{AVAV}	90		120		150		ns
Address Setup to $\overline{CE}$ Going Low		t_{AS}	t_{AVEL}	0		0		0		ns
Address Hold Time from $\overline{CE}$ Low		t_{AH}	t_{ELAX}	45		50		50		ns
Data Setup to $\overline{CE}$ Going High		t_{DS}	t_{DVEH}	45		50		50		ns
Data Hold Time from $\overline{CE}$ High		t_{DH}	t_{EHDX}	0		0		0		ns
Output Enable Setup Time (1)		t_{OES}		0		0		0		ns
Output Enable Hold Time (1)	Read	t_{OEH}		0		0		0		ns
	Toggle Bit I and $\overline{Data}$ Polling			10		10		10		ns
Read Recover Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		t_{GHEL}	t_{GHEL}	0		0		0		ns
$\overline{CE}$ Setup Time from $\overline{WE}$ Low		t_{WS}	t_{WLEL}	0		0		0		ns
$\overline{WE}$ Hold Time from $\overline{CE}$ High		t_{WH}	t_{EHWH}	0		0		0		ns
$\overline{WE}$ Pulse Width		t_{CP}	t_{ELEH}	45		50		50		ns
$\overline{WE}$ Pulse Width High		t_{CPH}	t_{ELEL}	20		20		20		ns
Byte Programming Operation		t_{WHWH1}	t_{WHWH1}	8		8		8		µs
Sector Erase Operation		t_{WHWH2}	t_{WHWH2}		15		15		15	Sec

Notes:
1. Not 100% tested.

AC Test Circuit



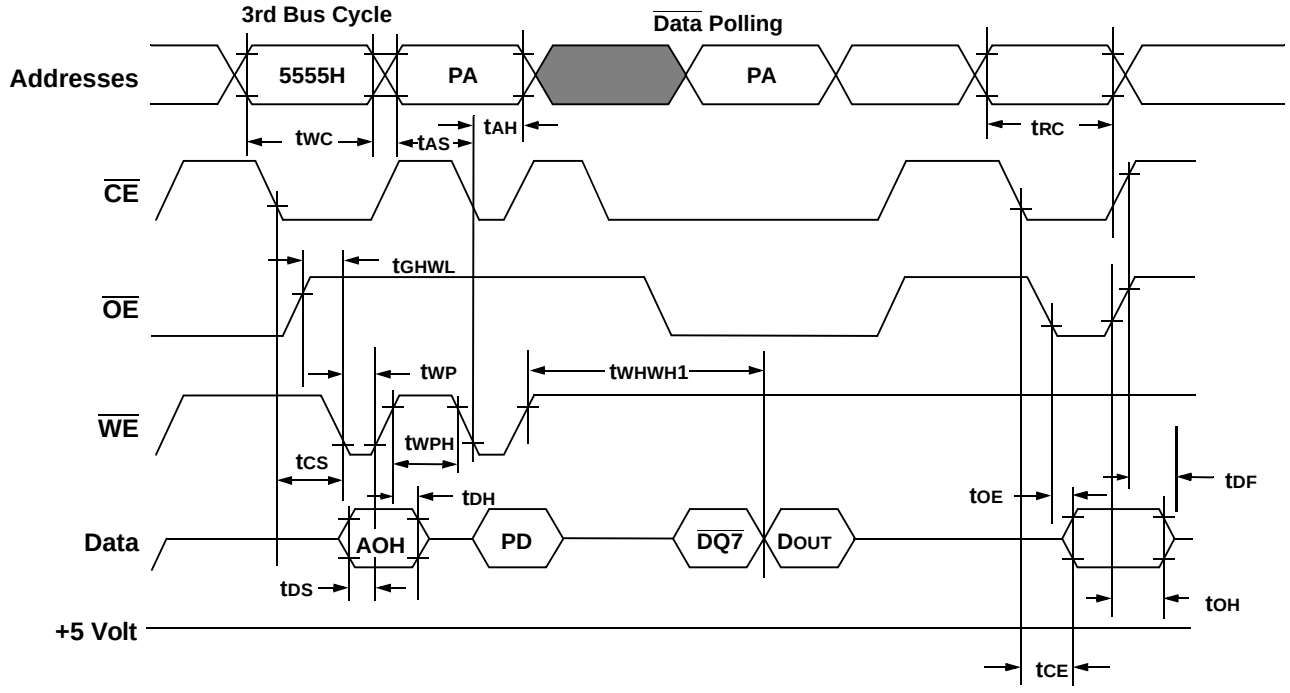
Test Configuration Component Values

Test Configuration	C_L (pF)	R1 (Ω)	R2 (Ω)
3.3V Standard Test	50	990	770
5V Standard Test	50	580	390

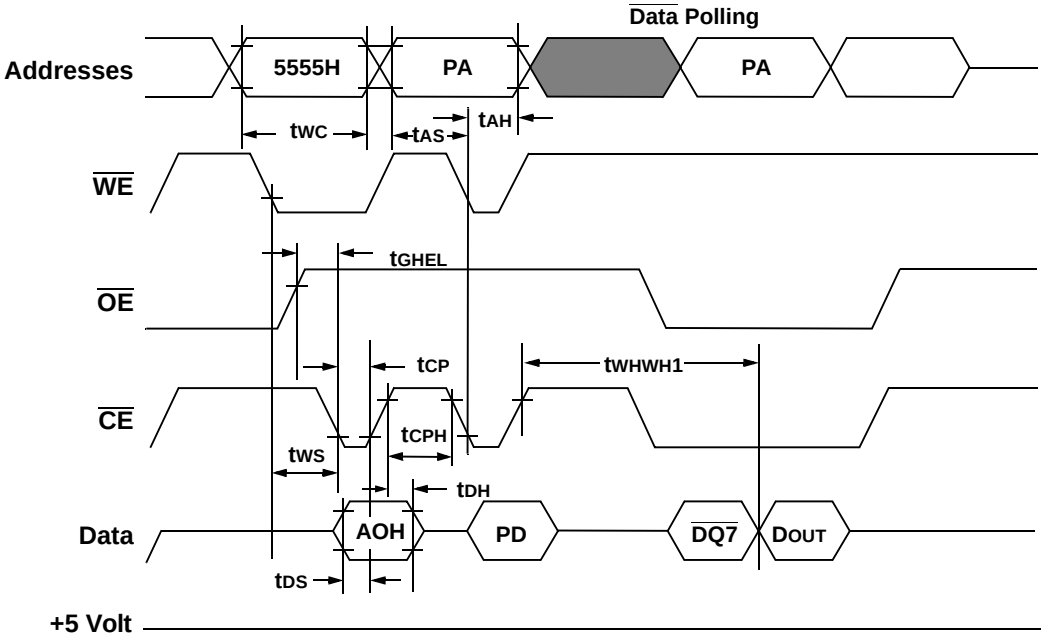
NOTES:
C_L includes jig capacitance.

Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V

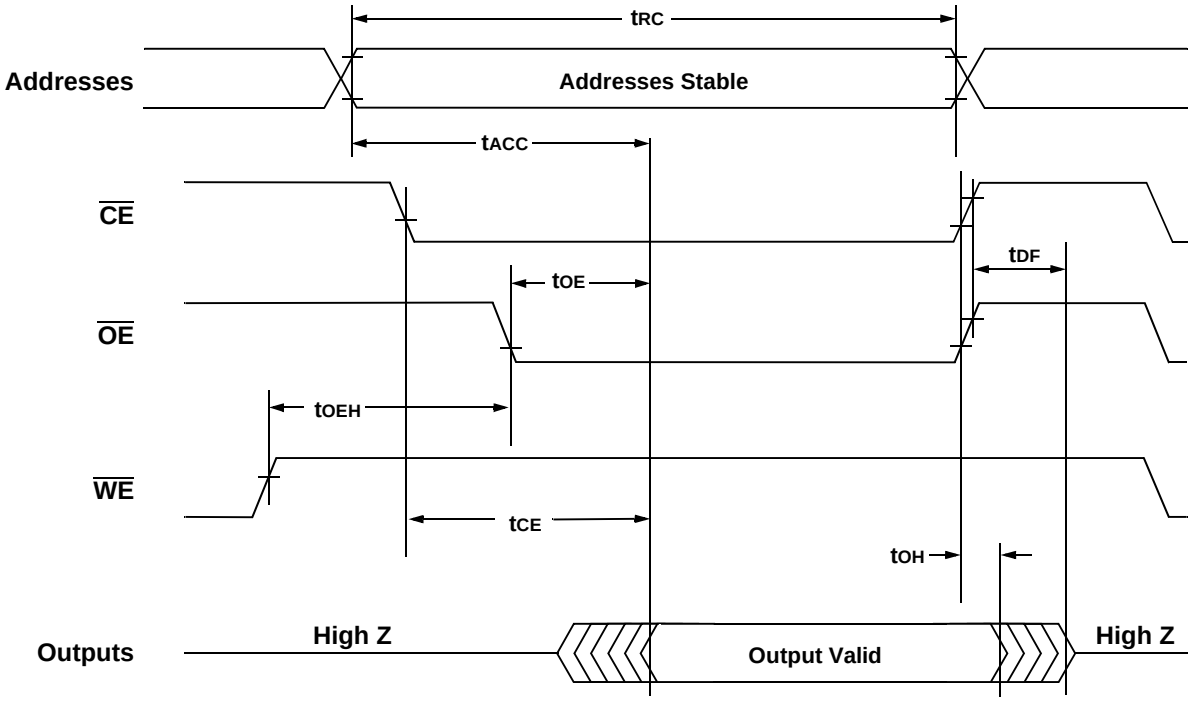
AC Waveforms for Write and Erase Operations, $\overline{WE}$ Controlled



AC Waveforms for Write and Erase Operations, $\overline{CE}$ Controlled



AC Waveform For Read Operations

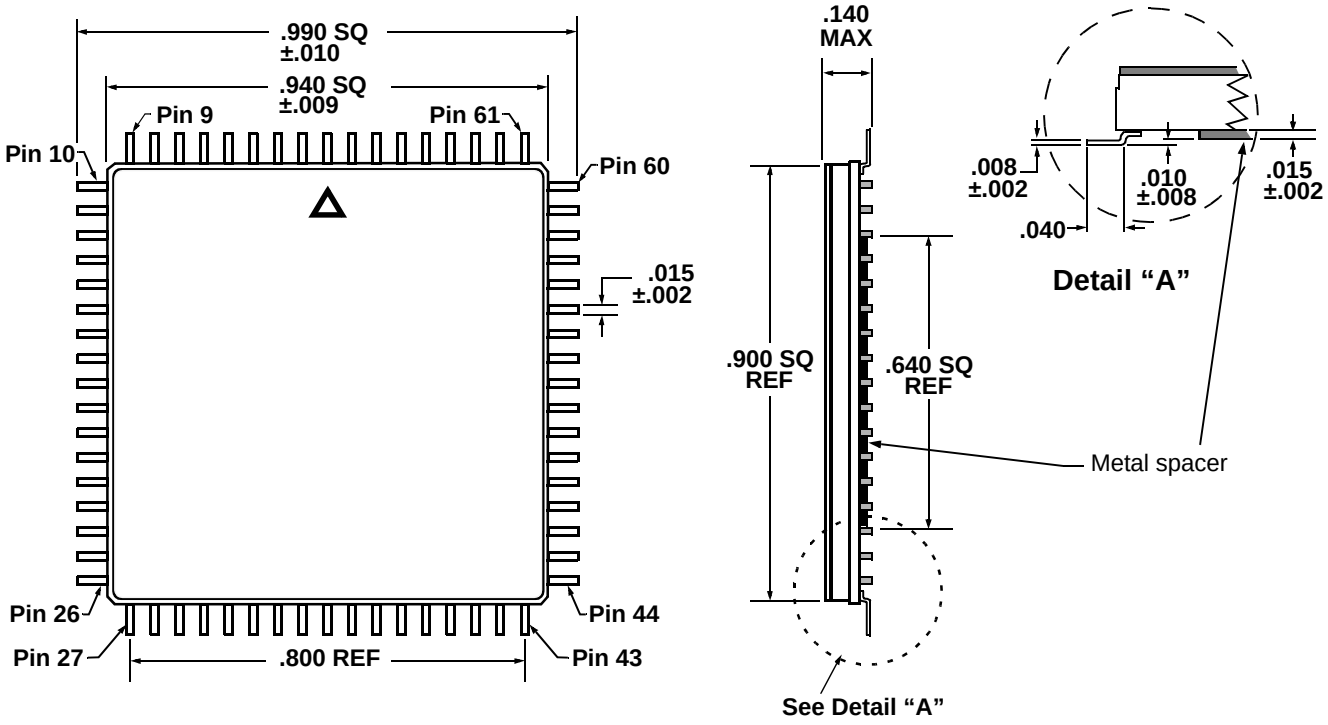


Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP *(Standard Configuration)*							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{CE}_3$	19	I/O_8	36	$\overline{CE}_2$	53	I/O_{23}
3	A_5	20	I/O_9	37	A_{17}	54	I/O_{22}
4	A_4	21	I/O_{10}	38	$RY/\overline{BY}$	55	I/O_{21}
5	A_3	22	I/O_{11}	39	NC	56	I/O_{20}
6	A_2	23	I/O_{12}	40	NC	57	I/O_{19}
7	A_1	24	I/O_{13}	41	A_{18}	58	I/O_{18}
8	A_0	25	I/O_{14}	42	A_{19}	59	I/O_{17}
9	$\overline{RESET}$	26	I/O_{15}	43	A_{20}	60	I/O_{16}
10	I/O_0	27	V_{CC}	44	I/O_{31}	61	V_{CC}
11	I/O_1	28	A_{11}	45	I/O_{30}	62	A_{10}
12	I/O_2	29	A_{12}	46	I/O_{29}	63	A_9
13	I/O_3	30	A_{13}	47	I/O_{28}	64	A_8
14	I/O_4	31	A_{14}	48	I/O_{27}	65	A_7
15	I/O_5	32	A_{15}	49	I/O_{26}	66	A_6
16	I/O_6	33	A_{16}	50	I/O_{25}	67	$\overline{WE}$
17	I/O_7	34	$\overline{CE}_1$	51	I/O_{24}	68	$\overline{CE}_4$

Consult Factory for Special order *(Optional Configuration)*: Pin 38 - $\overline{WE}_2$, Pin 39 - $\overline{WE}_3$, Pin 40 - $\overline{WE}_4$ and Pin 67 - $\overline{WE}_1$

"F18" — CQFP Package



All dimensions in inches

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Ordering Information

Model Number	Screening	Speed	Package
ACT–F2M32A–090F18C	Commercial (0°C to +70°C)	90 ns	CQFP
ACT–F2M32A–120F18C	Commercial (0°C to +70°C)	120 ns	CQFP
ACT–F2M32A–150F18C	Commercial (0°C to +70°C)	150 ns	CQFP
ACT–F2M32A–090F18I	Industrial (-40°C to +85°C)	90 ns	CQFP
ACT–F2M32A–120F18I	Industrial (-40°C to +85°C)	120 ns	CQFP
ACT–F2M32A–150F18I	Industrial (-40°C to +85°C)	150 ns	CQFP
ACT–F2M32A–090F18M	Military (-55°C to +125°C)	90 ns	CQFP
ACT–F2M32A–120F18M	Military (-55°C to +125°C)	120 ns	CQFP
ACT–F2M32A–150F18M	Military (-55°C to +125°C)	150 ns	CQFP
ACT–F2M32A–090F18Q	DESC Drawing Pending MIL-PRF-38534 Compliant	90 ns	CQFP
ACT–F2M32A–120F18Q	DESC Drawing Pending MIL-PRF-38534 Compliant	120 ns	CQFP
ACT–F2M32A–150F18Q	DESC Drawing Pending MIL-PRF-38534 Compliant	150 ns	CQFP

Part Number Breakdown

ACT– F 2M 32 A– 090 F18 M

Aeroflex Circuit Technology

Memory Type

S = SRAM
F = FLASH EEPROM
E = EEPROM
D = Dynamic RAM

Memory Depth, Locations

Memory Width, Bits

Pinout Options

A = One $\overline{WE}$, RY/$\overline{BY}$ access on Pin 38 - Standard pinout
C = Four $\overline{WE}$'s & RY/$\overline{BY}$ internally tied - Optional pinout

Memory Speed, ns (+5V Vcc)

Screening

C = Commercial Temp, 0°C to +70°C
I = Industrial Temp, -40°C to +85°C
T = Military Temp, -55°C to +125°C
M = Military Temp, -55°C to +125°C, Screened *
Q = MIL-PRF-38534 Compliant/SMD if applicable

Package Type & Size

Surface Mount Packages

F18 = .94" SQ 68 Lead\Dual-Cavity CQFP

* **Screened to the individual test methods of MIL-STD-883**

Specifications subject to change without notice

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