

# IP3338CX24

10-channel integrated LC-filter network with ESD input protection to IEC 61000-4-2 level 4

Rev. 01 — 13 November 2008

Product data sheet

## 1. Product profile

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### 1.1 General description

The IP3338CX24 is a 10-channel<sup>1</sup> LC low-pass filter network designed to filter undesired RF signals in the 800 MHz to 3000 MHz frequency band. In addition, the IP3338CX24 incorporates diodes which protect downstream components from ElectroStatic Discharge (ESD) voltages as high as 15 kV.

The IP3338CX24 is fabricated using monolithic silicon technology and integrates 10 inductors and 20 back-to-back diodes in a single Wafer-Level Chip-Scale Package (WLCSP) measuring 2.11 mm by 2.11 mm (typical). These features make the IP3338CX24 ideal for use in applications requiring the utmost in miniaturization such as mobile phone handsets, cordless telephones and personal digital devices.

### 1.2 Features

- Pb-free, RoHS compliant and halogen free package; Dark Green compliant
- Integrated 10-channel  $\pi$ -type LC filter network with 60 nH channel inductance
- 125  $\Omega$  series resistance; 25 pF (typical) capacitance per line
- Integrated ESD protection withstanding  $\pm 15$  kV contact discharge, far exceeding IEC 61000-4-2, level 4
- WLCSP with 0.4 mm pitch

### 1.3 Applications

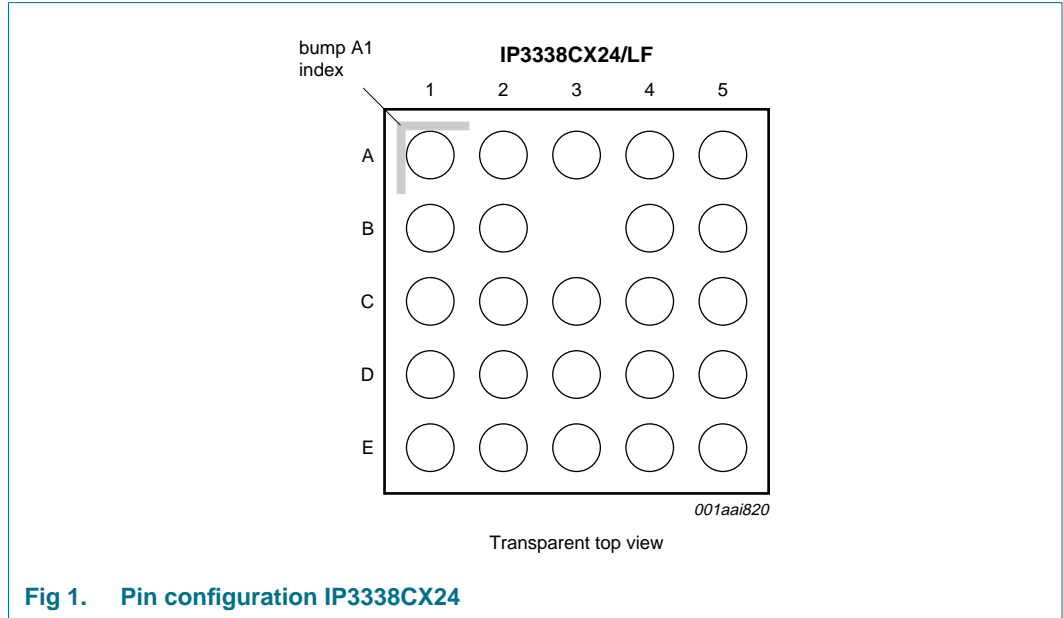
- Cellular and Personal Communication System (PCS) mobile handsets
- Cordless telephones
- Wireless data (WAN/LAN) systems
- PDAs

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1. Also available as a 7-channel device (IP3337CX18).

## 2. Pinning information

### 2.1 Pinning



**Fig 1. Pin configuration IP3338CX24**

**Table 1. Pinning**

Pin	Description
A2 and A5	filter channel 1
A1 and A4	filter channel 2
B2 and B5	filter channel 3
B1 and B4	filter channel 4
C2 and C5	filter channel 5
C1 and C4	filter channel 6
D2 and D5	filter channel 7
D1 and D4	filter channel 8
E2 and E5	filter channel 9
E1 and E4	filter channel 10
A3, C3, D3, E3	ground
B3	no ball

## 3. Ordering information

**Table 2. Ordering information**

Type number	Package		Version
	Name	Description	
IP3338CX24/LF	WLCSP24	wafer level chip-size package; 24 bumps; 2.11 × 2.11 × 0.61 mm	IP3338CX24/LF

### 4. Functional diagram

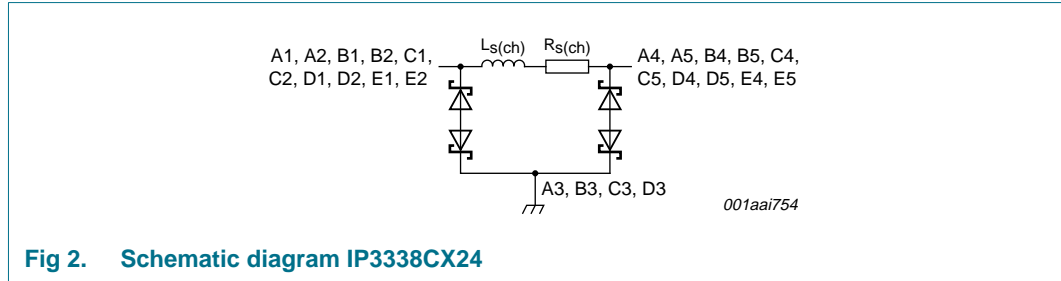


Fig 2. Schematic diagram IP3338CX24

### 5. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_I$	input voltage		-4.0	+4.0	V
$V_{ESD}$	electrostatic discharge voltage	all pins to ground			
		contact discharge	[1] -15	+15	kV
		air discharge	[1] -15	+15	kV
		IEC 61000-4-2, level 4; all pins to ground			
		contact discharge	-8	+8	kV
		air discharge	-15	+15	kV
$I_{ch}$	channel current (DC)	$T_{amb} = 70\text{ °C}$	-	10	mA
$I_{ch(M)}$	peak channel current	$T_{amb} = 70\text{ °C}; 60\text{ s}$	-	50	mA
$P_{ch}$	channel power dissipation	continuous power; $T_{amb} = 70\text{ °C}$	-	10	mW
$P_{tot}$	total power dissipation	$T_{amb} = 70\text{ °C}$	-	100	mW
$T_{stg}$	storage temperature		-55	+150	°C
$T_{reflow(peak)}$	peak reflow temperature	10 s maximum	-	260	°C
$T_{amb}$	ambient temperature		-35	+85	°C

[1] Device tested with 1000 pulses of ±15 kV contact discharges, according to the IEC 61000-4-2 model, which far exceeds IEC 61000-4-2, level 4 (8 kV contact discharge).

## 6. Characteristics

**Table 4. Channel characteristics**

$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{s(ch)}$	channel series resistance	$f = 0\text{ Hz (DC)}$	100	125	150	$\Omega$
$C_{ch}$	channel capacitance	$V_{bias(DC)} = 0\text{ V}; f = 1\text{ MHz}$	-	25	30 <sup>[1]</sup>	pF
$L_{s(ch)}$	channel series inductance		<sup>[1]</sup> -	60	-	nH
$V_{BR}$	breakdown voltage	$I_{test} = 1\text{ mA}$	6	-	10	V
		$I_{test} = -1\text{ mA}$	-10	-	-6	V
$I_{LR}$	reverse leakage current	per channel; $V_I = 3.0\text{ V}$	-	-	100	nA

[1] Guaranteed by design.

**Table 5. Frequency characteristics**

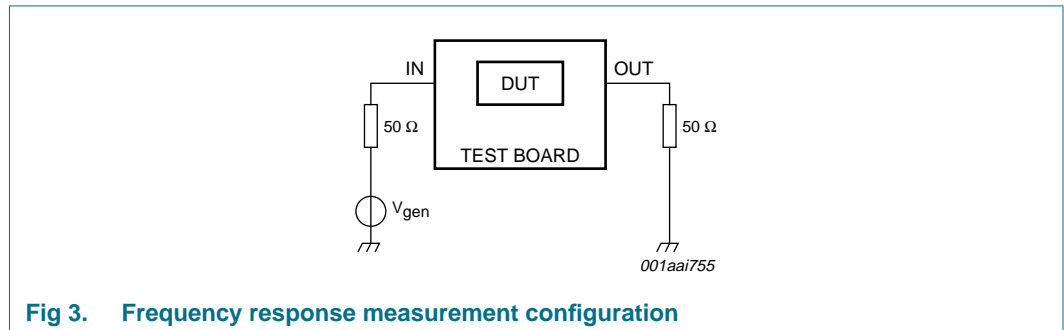
$T_{amb} = 25\text{ }^{\circ}\text{C}$ ; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\alpha_{ij}$	insertion loss	$R_{gen} = 50\text{ }\Omega; R_L = 50\text{ }\Omega$				
		$800\text{ MHz} < f < 1\text{ GHz}$	38	40	-	dB
		$1\text{ GHz} < f < 3\text{ GHz}$	35	40	-	dB
		at $0\text{ Hz}$ ; $R_{gen} = 50\text{ }\Omega$ ; $R_L = 50\text{ }\Omega; V_{bias(DC)} = 0\text{ V}$	6	7	10	dB
$f_{-3dB}$	cut-off frequency	measured relative to insertion loss at DC; $R_{gen} = 50\text{ }\Omega; R_L = 50\text{ }\Omega$	150	180	-	MHz
$\alpha_{ct}$	crosstalk attenuation	$800\text{ MHz} < f < 3\text{ GHz}$ ; $R_{gen} = 50\text{ }\Omega; R_L = 50\text{ }\Omega$	35	40	-	dB

## 7. Application information

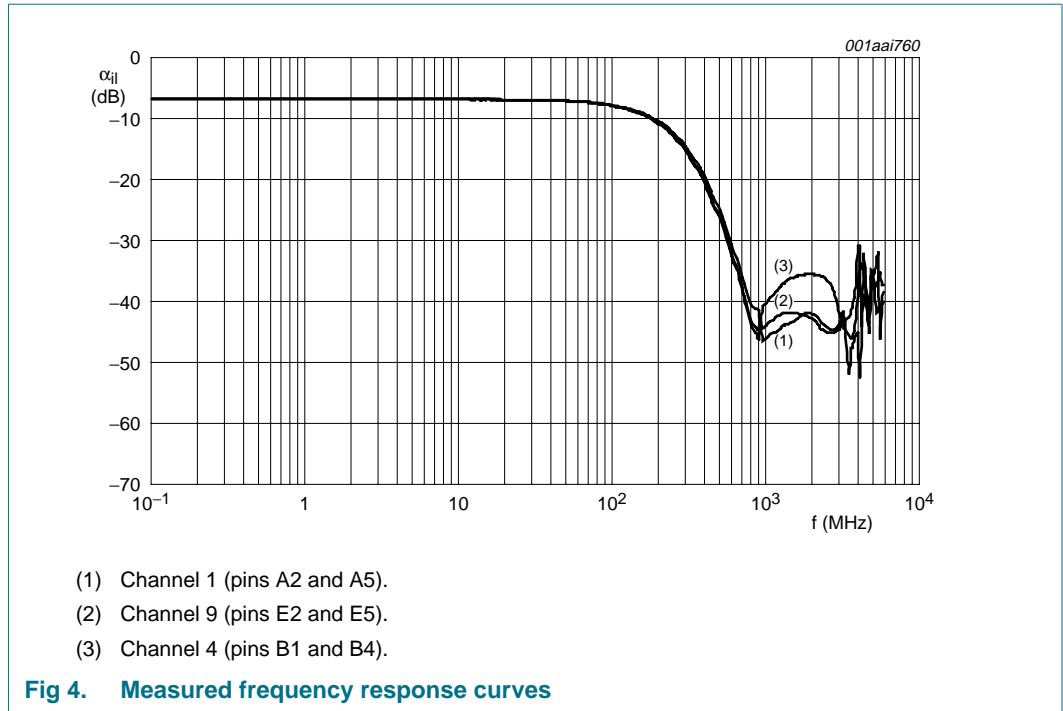
### 7.1 Insertion loss

The setup for measuring insertion loss in a  $50\text{ }\Omega$  system is shown in [Figure 3](#).



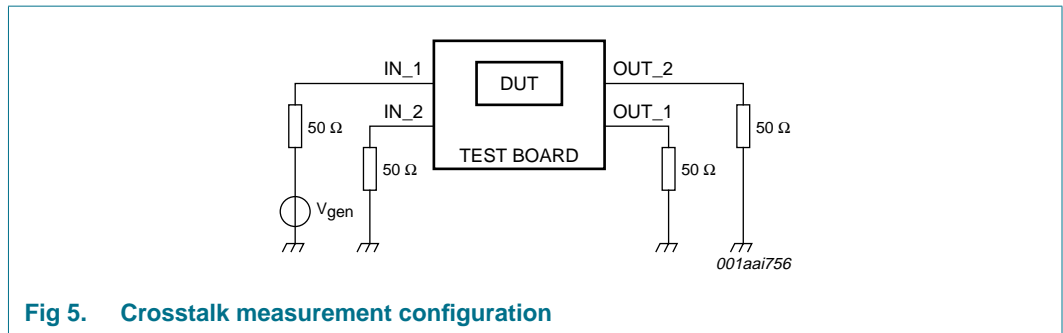
**Fig 3. Frequency response measurement configuration**

The measured frequency response curves for all channels are shown in [Figure 4](#).

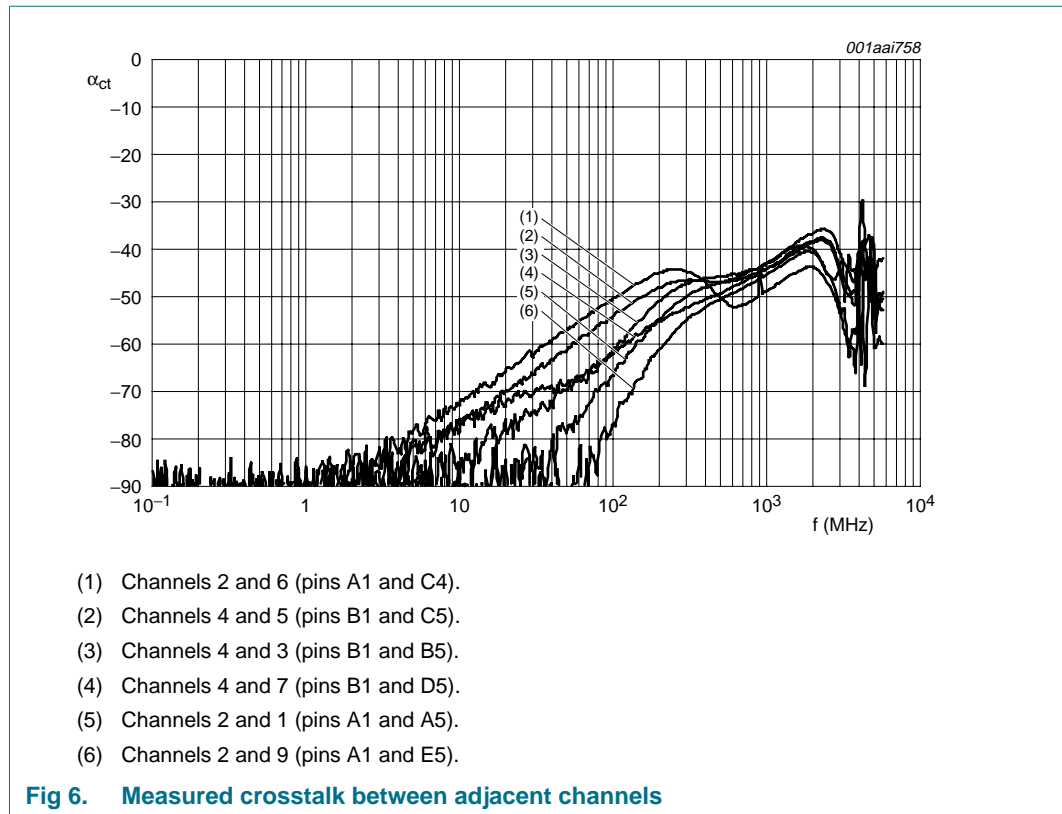


### 7.2 Crosstalk

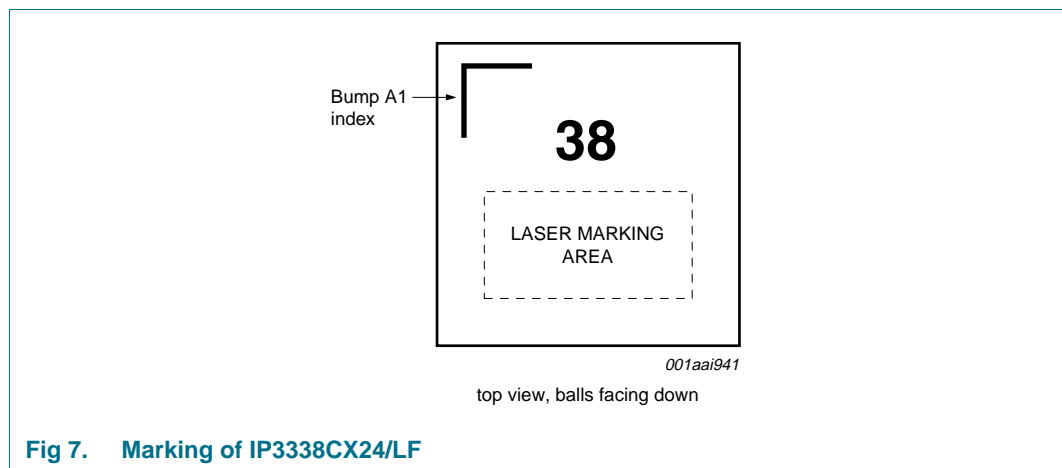
The setup for measuring crosstalk in a 50 Ω system is shown in [Figure 5](#).



The crosstalk between adjacent channels within the IP3338CX24 for different channel pairs measured in a 50 Ω NetWork Analyzer (NWA) system, is shown in [Figure 6](#). In all cases, all unused connections are terminated with 50 Ω to ground.



## 8. Marking



9. Package outline

WLCSP24: wafer level chip-size package; 24 bumps; 2.11 x 2.11 x 0.61 mm

IP3338CX24/LF

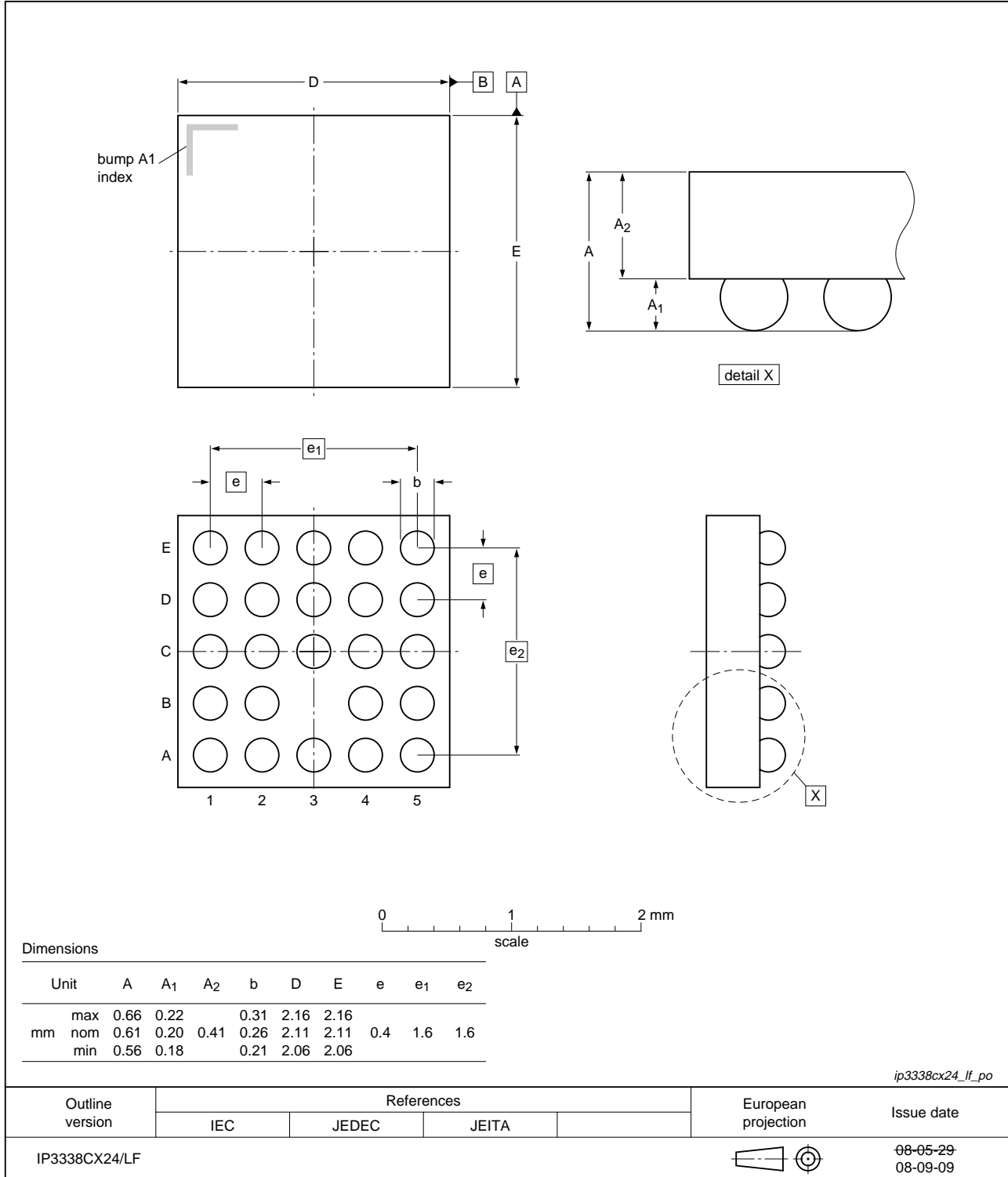


Fig 8. Package outline IP3338CX24/LF (WLCSP24)

10. Packing information

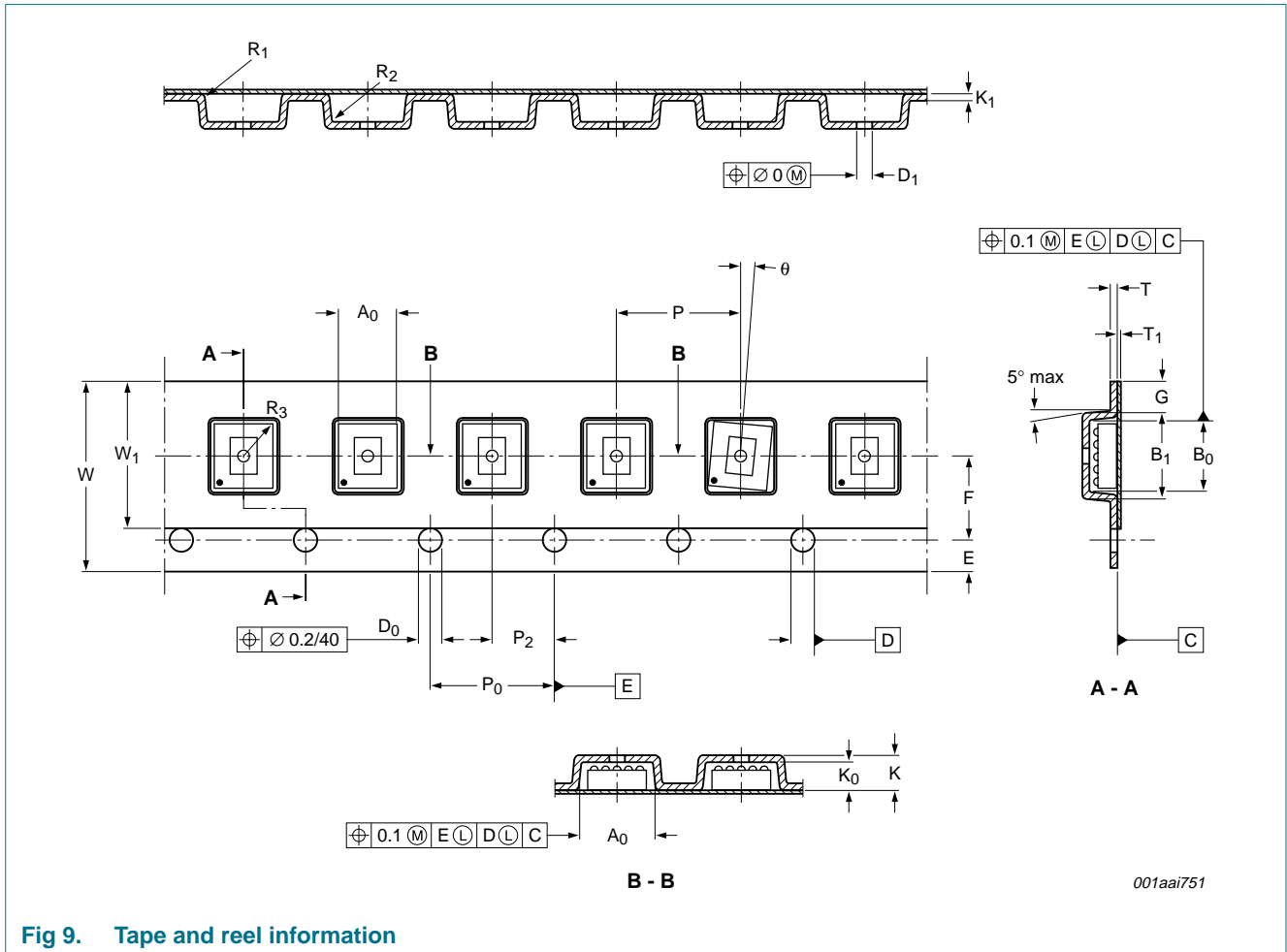


Fig 9. Tape and reel information

Table 6. Tape dimensions

Item	Parameter	Symbol	Specification (mm)	
			Dimension	Tolerance
Overall dimensions	tape width	W	8.00	±0.3
	thickness	K	1.20	maximum
	distance	G	0.75	minimum
	outside width	B1	3.70	maximum
Sprocket holes <sup>[1]</sup>	diameter	D0	1.50	+0.1/-0.0
	distance	E	1.75	±0.1
	pitch	P0	4.00	±0.1
Distance between center lines	length direction	P2	2.00	±0.05
	width direction	F	3.50	±0.05



Table 6. Tape dimensions ...continued

Item	Parameter	Symbol	Specification (mm)	
			Dimension	Tolerance
Compartments	length	A0	1.90	±0.05
	width	B 0	2.35	±0.05
	depth	K0	0.80	±0.05
	hole diameter	D1	0.50	±0.1
	pitch	P	4.00	±0.1
	radius	R1	0.40	maximum
	radius	R2	0.30	maximum
	radius	R3	0.30	typical
	depth	K1	0...0.25	-0.1
Device	rotation	$\theta$	±10°	
Carrier tape anti-static <sup>[2]</sup>	film thickness	T	0.25	±0.07
Cover tape <sup>[3]</sup>	width	W1	5.75	max
	film thickness	T1	0.1	max
Bending pad	in winding direction	R	30	min

[1] Cumulative pitch error: ±0.2 mm per 10 pitches.

[2] Carbon-loaded polystyrene 100 % recyclable.

[3] The cover tape must not overlap the sprocket holes.

## 11. Design and assembly recommendations

### 11.1 PCB design guidelines

For optimum performance it is recommended to use a Non-Solder Mask PCB Design (NSMD), also known as a copper-defined design, incorporating laser-drilled micro-vias connecting the ground pads to a buried ground-plane layer. This results in the lowest possible ground inductance and provides the best high frequency and ESD performance. For this case, refer to [Table 7](#) for the recommended PCB design parameters.

**Table 7. Recommended PCB design parameters**

Parameter	Value or Specification
PCB pad diameter	200 $\mu\text{m}$
Micro-via diameter	100 $\mu\text{m}$ (0.004 inch)
Solder mask aperture diameter	337 $\mu\text{m}$
Copper thickness	20 $\mu\text{m}$ to 40 $\mu\text{m}$
Copper finish	OSP
PCB material	FR4

### 11.2 PCB assembly guidelines for Pb-free soldering

**Table 8. Assembly recommendations**

Parameter	Value or Specification
Solder screen aperture diameter	330 $\mu\text{m}$
Solder screen thickness	100 $\mu\text{m}$ (0.004 inch)
Solder paste: Pb-free	SnAg (3 % to 4 %) Cu (0.5 % to 0.9 %)
Solder/flux ratio	50/50
Solder reflow profile	see <a href="#">Figure 10</a>

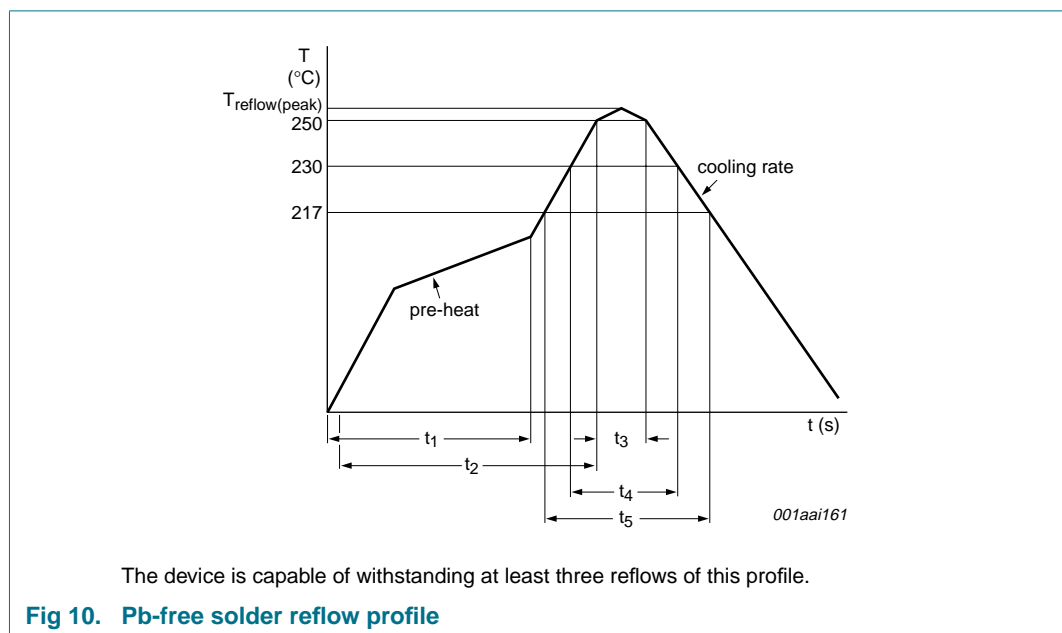


Table 9. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{\text{reflow(peak)}}$	peak reflow temperature		230	-	255	°C
$t_1$	time 1	soak time	60	-	180	s
$t_2$	time 2	time during $T \geq 250$ °C	-	-	30	s
$t_3$	time 3	time during $T \geq 230$ °C	10	-	50	s
$t_4$	time 4	time during $T > 217$ °C	30	-	150	s
$t_5$	time 5		-	-	540	s
dT/dt	rate of change of temperature	cooling rate	-	-	-6	°C/s
		pre-heat	2.5	-	4.0	°C/s

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
DUT	Device Under Test
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
FR4	Flame Retard 4
LAN	Local Area Network
NSMD	Non-Solder Mask Design
OSP	Organic Solderability Preservative
PCB	Printed-Circuit Board
PCS	Personal Communication System
PDA	Personal Digital Assistant
PSU	Power Supply Unit
RoHS	Restriction of Hazardous Substances
WAN	Wide Area Network
WLCSP	Wafer-Level Chip-Scale Package

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP3338CX24_1	20081113	Product data sheet	-	-

## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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