



NOMINAL SIZE = 1 in x 0.62 in (25,4 mm x 15,75 mm)

**Features**

- Up to 10-A Output Current
- 5-V Input Voltage
- Wide-Output Voltage Adjust (0.8 V to 3.6 V)
- Efficiencies up to 96 %
- 150 W/in<sup>3</sup> Power Density
- On/Off Inhibit
- Output Voltage Sense
- Pre-Bias Startup
- Margin Up/Down Controls
- Under-Voltage Lockout
- Auto-Track™ Sequencing
- Output Over-Current Protection (Non-Latching, Auto-Reset)
- Operating Temp: -40 to +85 °C
- DSP Compatible Output Voltages
- IPC Lead Free 2
- Safety Agency Approvals (Pending) UL 1950, CSA 22.2 950, & EN60950
- Point-of-Load Alliance (POLA) Compatible

**Description**

The ATH10T05 series non-isolated power module is small in size but big on performance and flexibility. Its high output current, compact footprint, and industry-leading features offers system designers a versatile module for powering complex multi-processor digital systems.

This product employs double-sided surface mount construction and provides high-performance step-down power conversion for up to 10 A of output current from a 5-V input bus voltage. The output voltage is adjustable and can be set to any value over the range, 0.8 V to 3.6 V, using a single resistor.

This series includes Auto-Track™

Sequencing. Auto-Track simplifies the task of supply voltage sequencing in a power system by enabling modules to track each other, or any external voltage, during power up and power down.

Other operating features include an on/off inhibit, margin up/down controls, and the ability to start up into an existing output voltage or prebias. To ensure tight load regulation, an output voltage sense is also provided. A non-latching over-current trip serves as load fault protection.

Target applications include complex multi-voltage, multi-processor systems that incorporate the industry's high-speed DSPs, micro-processors and bus drivers.

**Pin Configuration**

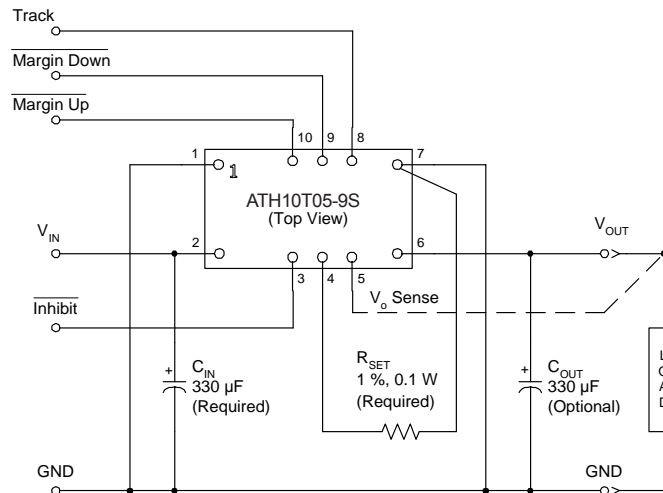
Pin	Function
1	GND
2	V <sub>in</sub>
3	Inhibit *
4	V <sub>o</sub> Adjust
5	V <sub>o</sub> Sense
6	V <sub>out</sub>
7	GND
8	Track
9	Margin Down *
10	Margin Up *

\* Denotes negative logic:  
Open = Normal operation  
Ground = Function active



ADVANCE INFORMATION

**Standard Application**



R<sub>set</sub> = Resistor to set the desired output voltage (see spec. table for values)  
C<sub>in</sub> = Required 330 µF capacitor  
C<sub>out</sub> = Optional 330 µF capacitor

## Ordering Information

Input Voltage	Output Voltage	Output Current	Model Number
4.5V to 5.5V	0.8V <sup>1</sup> to 3.6V	10A	ATH10T05-9(S)(J)

Options:

- “-J” - Through-hole Termination, Tray Packaging
- “-SJ” - SMT Termination, Tray Packaging
- “-S” - SMT Termination, T&R Packaging

Notes:

<sup>1</sup>Preset output voltage is 0.8V; externally adjustable to 3.6V through the Vo,Adjust pin

## Pin Descriptions

**Vin:** The positive input voltage power node to the module, which is referenced to common *GND*.

**Vout:** The regulated positive power output with respect to the *GND* node.

**GND:** This is the common ground connection for the *Vin* and *Vout* power connections. It is also the 0 VDC reference for the control inputs.

**Inhibit:** The Inhibit pin is an open-collector/drain negative logic input that is referenced to *GND*. Applying a low-level ground signal to this input disables the module's output and turns off the output voltage. When the *Inhibit* control is active, the input current drawn by the regulator is significantly reduced. If the *Inhibit* pin is left open-circuit, the module will produce an output whenever a valid input source is applied.

**Vo Adjust:** A 0.1 W 1 % resistor must be directly connected between this pin and pin 7 (*GND*) to set the output voltage to a value higher than 0.8 V. The temperature stability of the resistor should be 100 ppm/°C (or better). The set point range for the output voltage is from 0.8 V to 3.6 V. The resistor value required for a given output voltage may be calculated from the following formula. If left open circuit, the output voltage will default to its lowest value. For further information on output voltage adjustment consult the related application note.

$$R_{\text{set}} = 10 \text{ k}\Omega \frac{0.8 \text{ V}}{V_{\text{out}} - 0.8 \text{ V}} - 2.49 \text{ k}\Omega$$

The specification table gives the preferred resistor values for a number of standard output voltages.

**Vo Sense:** The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy *Vo Sense* should be connected to *Vout*. It can also be left disconnected.

**Track:** This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range the output will follow the voltage at the *Track* pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, the input may be left unconnected. *Note: Due to the under-voltage lockout, this feature does not allow the output from the module to follow its own input voltage during power up. For more information, consult the related application note.*

**Margin Down:** When this input is asserted to *GND*, the output voltage is decreased by 5% from the nominal. The input requires an open-collector (open-drain) interface. It is not TTL compatible. A lower percent change can be accommodated with a series resistor. If unused, the input may be left unconnected. For further information, consult the related application note.

**Margin Up:** When this input is asserted to *GND*, the output voltage is increased by 5%. The input requires an open-collector (open-drain) interface. It is not TTL compatible. The percent change can be reduced with a series resistor. If unused, the input may be left unconnected. For further information, consult the related application note.

# ATH10T05 Series —5-V Input

## 10-A, 5-V Input Non-Isolated Wide-Output Adjust Power Module

### Environmental & Absolute Maximum Ratings (Voltages are with respect to GND)

Characteristics	Symbols	Conditions	Min	Typ	Max	Units
Track Input Voltage	$V_{\text{track}}$		-0.3	—	$V_{\text{in}} + 0.3$	V
Operating Temperature Range	$T_a$	Over $V_{\text{in}}$ Range	-40 (i)	—	85	°C
Solder Reflow Temperature	$T_{\text{reflow}}$	Surface temperature of module body or pins			215 (ii)	°C
Storage Temperature	$T_s$		-40	—	125	°C
Mechanical Shock		Per Mil-STD-883D, Method 2002.3 1 msec, ½ Sine, mounted	—	TBD	—	G's
Mechanical Vibration		Mil-STD-883D, Method 2007.2 20-2000 Hz	Suffix H Suffix S	TBD TBD	—	G's
Weight	—		—	3.7	—	grams
Flammability	—	Meets UL 94V-O				

**Notes:** (i) For operation below 0 °C the external capacitors must have stable characteristics. Use either a low ESR tantalum, Os-Con, or ceramic capacitor.  
(ii) During reflow of SMD package version do not elevate peak temperature of the module, pins or internal components above the stated maximum. For further guidance refer to the application note, "Reflow Soldering Requirements for Plug-in Power Surface Mount Products."

### Specifications (Unless otherwise stated, $T_a = 25$ °C, $V_{\text{in}} = 5$ V, $V_o = 3.3$ V, $C_{\text{in}} = 330$ µF, $C_{\text{out}} = 0$ µF, and $I_o = I_{o\text{max}}$ )

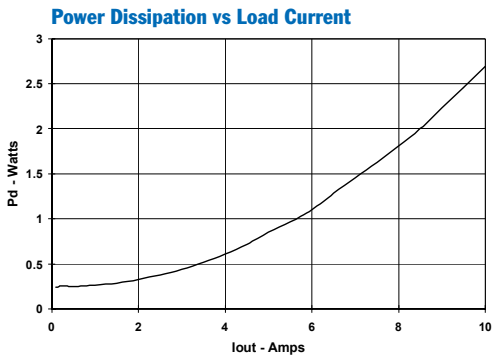
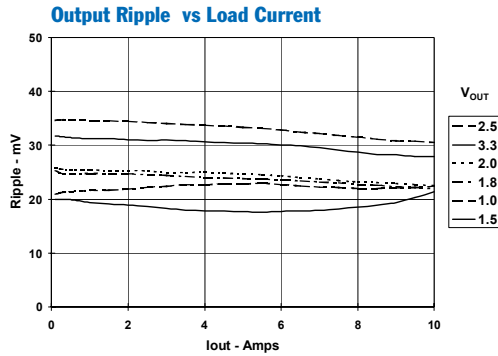
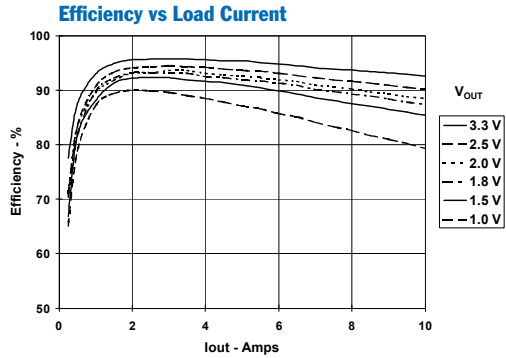
Characteristics	Symbols	Conditions	ATH10T05			Units
			Min	Typ	Max	
Output Current	$I_o$	$0.8 \text{ V} \leq V_o \leq 3.6 \text{ V}$ , 60 °C, 200 LFM airflow 25 °C, natural convection	0 0	— —	10 (1) 10 (1)	A
Input Voltage Range	$V_{\text{in}}$	Over $I_o$ range	4.5	—	5.5	V
Set-Point Voltage Tolerance	$V_o \text{ tol}$		—	—	±2 (2)	% $V_o$
Temperature Variation	$\Delta \text{Reg}_{\text{temp}}$	-40 °C < $T_a$ < +85 °C	—	±0.5	—	% $V_o$
Line Regulation	$\Delta \text{Reg}_{\text{line}}$	Over $V_{\text{in}}$ range	—	±10	—	mV
Load Regulation	$\Delta \text{Reg}_{\text{load}}$	Over $I_o$ range	—	±12	—	mV
Total Output Variation	$\Delta \text{Reg}_{\text{tot}}$	Includes set-point, line, load, -40 °C ≤ $T_a$ ≤ +85 °C	—	—	±3 (2)	% $V_o$
Efficiency	$\eta$	$I_o = 7 \text{ A}$ RSET = 698 Ω $V_o = 3.3 \text{ V}$ RSET = 2.21 kΩ $V_o = 2.5 \text{ V}$ RSET = 4.12 kΩ $V_o = 2.0 \text{ V}$ RSET = 5.49 kΩ $V_o = 1.8 \text{ V}$ RSET = 8.87 kΩ $V_o = 1.5 \text{ V}$ RSET = 17.4 kΩ $V_o = 1.2 \text{ V}$ RSET = 36.5 kΩ $V_o = 1.0 \text{ V}$	— — — — — — —	94 92 91 90 89 86 85	— — — — — — —	%
$V_o$ Ripple (pk-pk)	$V_r$	20 MHz bandwidth	—	25	—	mVpp
Over-Current Threshold	$I_o \text{ trip}$	Reset, followed by auto-recovery	—	20	—	A
Transient Response	$t_{\text{tr}}$ $\Delta V_{\text{tr}}$	1 A/µs load step, 50 to 100 % $I_{o\text{max}}$ , $C_{\text{out}} = 330 \text{ µF}$ Recovery Time $V_o$ over/undershoot	— —	70 100	— —	µSec mV
Margin Up/Down Adjust	$\Delta V_o \text{ margin}$		—	±5	—	%
Margin Input Current (pins 9/10)	$I_{\text{IL}} \text{ margin}$	Pin to GND	—	-8 (3)	—	µA
Track Input Current (pin 8)	$I_{\text{IL}} \text{ track}$	Pin to GND	—	—	-130 (4)	µA
Track Slew Rate Capability	$dV_{\text{track}}/dt$	$ V_{\text{track}} - V_o  \leq 50 \text{ mV}$ and $V_{\text{track}} < V_o(\text{nom})$	5	—	—	V/ms
Under-Voltage Lockout	UVLO	$V_{\text{in}}$ increasing $V_{\text{in}}$ decreasing	— 3.4	4.3 3.7	4.45 —	V
Inhibit Control (pin3) Input High Voltage Input Low Voltage	$V_{\text{IH}}$ $V_{\text{IL}}$	Referenced to GND	$V_{\text{in}} - 0.5$ -0.2	—	Open (4) 0.6	V
Input Low Current	$I_{\text{IL}} \text{ inhibit}$	Pin to GND	—	-130	—	µA
Input Standby Current	$I_{\text{in}} \text{ inh}$	Inhibit (pin 3) to GND, Track (pin 8) open	—	10	—	mA
Switching Frequency	$f_s$	Over $V_{\text{in}}$ and $I_o$ ranges	275	300	325	kHz
External Input Capacitance	$C_{\text{in}}$		330 (5)	—	—	µF
External Output Capacitance	$C_{\text{out}}$		0	330 (6)	15,000	µF
Reliability	MTBF	Per Bellcore TR-332 50 % stress, $T_a = 40$ °C, ground benign	TBD	—	—	10 <sup>6</sup> Hrs

**Notes:** (1) See SOA curves or consult factory for appropriate derating.  
(2) The set-point voltage tolerance is affected by the tolerance and stability of RSET. The stated limit is unconditionally met if RSET has a tolerance of 1 % with 100 ppm/°C or better temperature stability.  
(3) A small low-leakage (<100 nA) MOSFET is recommended to control this pin. The open-circuit voltage is less than 1 Vdc.  
(4) This control pin has an internal pull-up to the input voltage  $V_{\text{in}}$ . If it is left open-circuit the module will operate when input power is applied. A small low-leakage (<100 nA) MOSFET is recommended for control. For further information, consult the related application note.  
(5) A 330 µF input capacitor is required for proper operation. The capacitor must be rated for a minimum of 500 mA rms of ripple current.  
(6) An external output capacitor is not required for basic operation. Adding 330 µF of distributed capacitance at the load will improve the transient response.

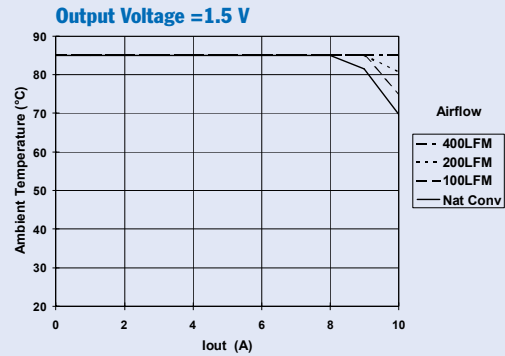
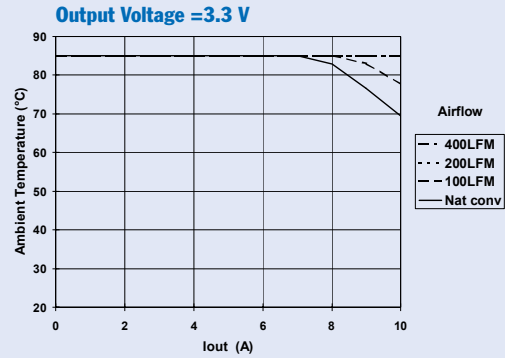
ADVANCE INFORMATION

10-A, 5-V Input Non-Isolated Wide-Output Adjust Power Module

Characteristic Data;  $V_{in} = 5\text{ V}$  (See Note A)



Safe Operating Area;  $V_{in} = 5\text{ V}$  (See Note B)



ADVANCE INFORMATION

The products listed hereunder are prototype or pre-production devices which have not been fully qualified to Astec's specifications. Product specifications are subject to change without notice. Astec makes no warranty, either expressed, implied, or statutory, including implied warranty of merchantability or fitness for a specific purpose, of these products.

**Note A:** Characteristic data has been developed from actual products tested at 25°C. This data is considered typical data for the Converter.

**Note B:** SOA curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 4-layer PCB with 1 oz. copper.



### Adjusting the Output Voltage of the ATH10T033 & ATH10T05 Wide-Output Adjust Power Modules

The  $V_o$  Adjust control (pin 4) sets the output voltage of the ATH10T033 and ATH10T05 products to a value higher than 0.8 V. The adjustment range of the ATH10T033 (3.3-V input) is from 0.8 V to 2.5 V1, and the ATH10T05 (5-V input) from 0.8 V to 3.6 V. For an output voltage other than 0.8 V a single external resistor,  $R_{set}$ , must be connected directly between the  $V_o$  Adjust and GND pins 2. Table 1-1 gives the preferred value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

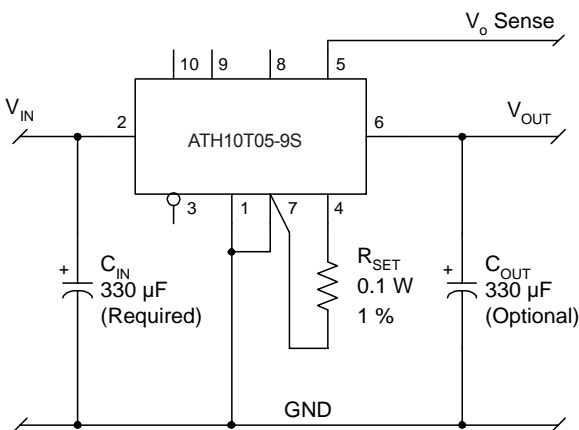
For other output voltages the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 1-2. Figure 1-1 shows the placement of the required resistor.

$$R_{set} = 10 \text{ k}\Omega \cdot \frac{0.8 \text{ V}}{V_{out} - 0.8 \text{ V}} = 2.49 \text{ k}\Omega$$

**Table 1-1; Preferred Values of  $R_{set}$  for Standard Output Voltages**

$V_{out}$ (Standard)	$R_{set}$ (Pref'd Value)	$V_{out}$ (Actual)
3.3 V1	698 $\Omega$	3.309V
2.5 V	2.21 k $\Omega$	2.502 V
2 V	4.12 k $\Omega$	2.010 V
1.8 V	5.49 k $\Omega$	1.803 V
1.5 V	8.87 k $\Omega$	1.504 V
1.2 V	17.4 k $\Omega$	1.202 V
1 V	36.5 k $\Omega$	1.005 V
0.8 V	Open	0.8 V

**Figure 1-1;  $V_o$  Adjust Resistor Placement**



**Table 1-2; Output Voltage Set-Point Resistor Values**

$V_a$ Req'd	$R_{set}$	$V_a$ Req'd	$R_{set}$
0.800	Open	2.00	4.18 k $\Omega$
0.825	318 k $\Omega$	2.05	3.91 k $\Omega$
0.850	158 k $\Omega$	2.10	3.66 k $\Omega$
0.875	104 k $\Omega$	2.15	3.44 k $\Omega$
0.900	77.5 k $\Omega$	2.20	3.22 k $\Omega$
0.925	61.5 k $\Omega$	2.25	3.03 k $\Omega$
0.950	50.8 k $\Omega$	2.30	2.84 k $\Omega$
0.975	43.2 k $\Omega$	2.35	2.67 k $\Omega$
1.000	37.5 k $\Omega$	2.40	2.51 k $\Omega$
1.025	33.1 k $\Omega$	2.45	2.36 k $\Omega$
1.050	29.5 k $\Omega$	2.50	2.22 k $\Omega$
1.075	26.6 k $\Omega$	2.55	2.08 k $\Omega$
1.100	24.2 k $\Omega$	2.60	1.95 k $\Omega$
1.125	22.1 k $\Omega$	2.65	1.83 k $\Omega$
1.150	20.4 k $\Omega$	2.70	1.72 k $\Omega$
1.175	18.8 k $\Omega$	2.75	1.61 k $\Omega$
1.200	17.5 k $\Omega$	2.80	1.51 k $\Omega$
1.225	16.3 k $\Omega$	2.85	1.41 k $\Omega$
1.250	15.3 k $\Omega$	2.90	1.32 k $\Omega$
1.275	14.4 k $\Omega$	2.95	1.23 k $\Omega$
1.300	13.5 k $\Omega$	3.00	1.15 k $\Omega$
1.325	12.7 k $\Omega$	3.05	1.07 k $\Omega$
1.350	12.1 k $\Omega$	3.10	988 $\Omega$
1.375	11.4 k $\Omega$	3.15	914 $\Omega$
1.400	10.8 k $\Omega$	3.20	843 $\Omega$
1.425	10.3 k $\Omega$	3.25	775 $\Omega$
1.450	9.82 k $\Omega$	3.30	710 $\Omega$
1.475	9.36 k $\Omega$	3.35	647 $\Omega$
1.50	8.94 k $\Omega$	3.40	587 $\Omega$
1.55	8.18 k $\Omega$	3.45	529 $\Omega$
1.60	7.51 k $\Omega$	3.50	473 $\Omega$
1.65	6.92 k $\Omega$	3.55	419 $\Omega$
1.70	6.4 k $\Omega$	3.60	367 $\Omega$
1.75	5.93 k $\Omega$		
1.80	5.51 k $\Omega$		
1.85	5.13 k $\Omega$		
1.90	4.78 k $\Omega$		
1.95	4.47 k $\Omega$		

#### Notes:

1. Modules that operate from a 3.3-V input bus should not be adjusted higher than 2.5 V.
2. Use a 0.1 W resistor. The tolerance should be 1 %, with temperature stability of 100 ppm/°C (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 4 and 7 using dedicated PCB traces.
3. Never connect capacitors from  $V_o$  Adjust to either GND or  $V_{out}$ . Any capacitance added to the  $V_o$  Adjust pin will affect the stability of the regulator.

### ATH10T033/T05: Capacitor Recommendations

#### Input Capacitor

The recommended input capacitor(s) is determined by 330  $\mu$ F minimum capacitance, and 500 mA rms minimum ripple current rating.

Ripple current and <150 m $\Omega$  equivalent series resistance (ESR) values are the major considerations, along with temperature, when designing with different types of capacitors. Tantalum capacitors have a recommended minimum voltage rating of twice 2 $\times$  (the maximum DC voltage + AC ripple). This is standard practice for tantalum capacitors to insure reliability.

#### Output Capacitors (Optional)

The ESR of the bulk (non-ceramic) capacitors must be equal to, or less than 150 m $\Omega$ . Electrolytic capacitors have marginal ripple performance at frequencies greater than 400 kHz but excellent low frequency transient response. Above the ripple frequency, ceramic capacitors are necessary to improve the transient response and reduce any high frequency noise components apparent during higher current excursions.

#### Tantalum Capacitors

Tantalum type capacitors can be used for the output but only the AVX TPS, Sprague 593D/594/595 or Kemet T495/T510 series. These capacitors are recommended

over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution the TAJ series by AVX is not recommended. This series has considerably higher ESR, reduced power dissipation, and lower ripple current capability. The TAJ series is less reliable than the AVX TPS series when determining power dissipation capability. Tantalum or Oscon® types are recommended for applications where ambient temperatures fall below 0 °C.

#### Ceramic Capacitors

Ceramic capacitors will compliment electrolytic types. Adding 10  $\mu$ F to 47  $\mu$ F of ceramic capacitance will reduce ripple on the input and output bus. Output ripple and transient measurement accuracy is improved by measuring directly across a 10  $\mu$ F ceramic capacitor.

#### Capacitor Table

Table 2-1 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The number of capacitors required at both the input and output buses is identified for each capacitor type.

*This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100 kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.*

**Table 1: Input/Output Capacitors**

Capacitor Vendor/ Series	Capacitor Characteristics					Quantity		Vendor Part Number
	Working Voltage	Value ( $\mu$ F)	(ESR) Equivalent Series Resistance	Max. Ripple Current @105 °C (I <sub>rms</sub> )	Physical Size (mm)	Input Bus	Output Bus	
Panasonic (FC Radial)	10 V	330	0.117 $\Omega$	555 mA	8 $\times$ 10	1	1	EEUFC1A331
WA (SMT.)	10 V	330	0.022 $\Omega$	4500 mA	10 $\times$ 10.2	1	1	EEFWA1A331P
FK (SMT.)	25 V	470	0.080 $\Omega$	850 mA	10 $\times$ 10.2	1	1	EEVFK1E471P
FC (SMT)	16 V	330	0.150 $\Omega$	670 mA	10 $\times$ 10.2	1	1	EEVFC1C331P
United Chemi-con								
PXA (SMT)	10 V	330	0.024 $\Omega$	3770 mA	10 $\times$ 7.7	1	1	PXA10VC331MJ80TP
PS	16 V	330	0.014 $\Omega$	5050 mA	10 $\times$ 12.5	1	1	16PS330MJ12
FX	10 V	390	0.018 $\Omega$	3710 mA	8 $\times$ 10.5	1	1	10FX390M
LXZ Series	16 V	330	0.120 $\Omega$	555 mA	8 $\times$ 12.5	1	1	LXZ16VB331M8X12LL
Nichicon (WG)	25 V	330	0.150 $\Omega$	670 mA	10 $\times$ 10	1	1	UWG1E331MNR1GS
HD Series	16 V	330	0.072 $\Omega$	760 mA	8 $\times$ 11.5	1	1	UHD1A331MPR
PM Series	16 V	330	0.120 $\Omega$	625 mA	10 $\times$ 12.5	1	1	UPM1C331MPH6
Sanyo-Os-con (SP)	10 V	470	0.015 $\Omega$	>4500 mA	10 $\times$ 10.5	1	1	10SP470M
SVP (SMT)	10 V	330	0.017 $\Omega$	>3950mA	8 $\times$ 12	1	1	10SVP330M
AVX Tantalum	10 V	330	0.045 $\Omega$	1723 mA	7.3L	1	1	TPSE337M010R0045
TPS (SMT.)	10 V	330	0.060 $\Omega$	1826 mA	$\times$ 5.7W $\times$ 4.1H	1	1	TPSV337M010R0060
Kemet Polymer	10 V	330	0.040 $\Omega$	1800 mA	4.3W	1	1	T520X337M010AS
Tantalum T520/T530 (SMT)	10 V	330	0.015 $\Omega$	>3800 mA	$\times$ 7.3L $\times$ 4.0H	1	1	T530X337M010AS
Sprague Tantalum	10 V	330	0.100 $\Omega$	1040 mA	7.2L	1	1	595D337X0010D2T
595D Series (SMT)	10 V	330	0.045 $\Omega$	2360 mA	$\times$ 6W $\times$ 4.1H			594D337X0016R2T



### Features of the ATH Family of Non-Isolated Wide Output Adjust Power Modules

#### Point-of-Load Alliance

The ATH family of non-isolated, wide-output adjust power modules are optimized for applications that require a flexible, high performance module that is small in size. These products are part of the “Point-of-Load Alliance” (POLA), which ensures compatible footprint, interoperability and true second sourcing for customer design flexibility. The POLA is a collaboration between Texas Instruments, Artesyn Technologies, and Astec Power to offer customers advanced non-isolated modules that provide the same functionality and form factor. Product series covered by the alliance includes the ATH06 (6 A), ATH10 (10 A), ATH12/15 (12/15 A), ATH18/22 (18/22 A), and the ATH26/30 (26/30 A).

From the basic, “Just Plug it In” functionality of the 6-A modules, to the 30-A rated feature-rich ATH30 Series, these products were designed to be very flexible, yet simple to use. The features vary with each product. Table 3-1 provides a quick reference to the available features by product and input bus voltage.

**Table 3-1; Operating Features by Series and Input Bus Voltage**

Series	Input Bus	I <sub>OUT</sub>	Adjust (Trim)	On/Off Inhibit	Over-Current	Pre-Bias Startup	Auto-Track™	Margin Up/Down	Output Sense	Thermal Shutdown
ATH06	3.3 V	6 A	•	•	•	•	•			
	5 V	6 A	•	•	•	•	•			
	12 V	6 A	•	•	•	•	•			
ATH10	3.3 V / 5 V	10 A	•	•	•	•	•	•	•	
	12 V	10 A	•	•	•	•	•	•	•	
ATH12/15	3.3 V / 5 V	15 A	•	•	•	•	•	•	•	
	12 V	12 A	•	•	•	•	•	•	•	
ATH18/22	3.3 V / 5 V	22 A	•	•	•	•	•	•	•	•
	12 V	18 A	•	•	•	•	•	•	•	•
ATH26/30	3.3 V / 5 V	30 A	•	•	•	•	•	•	•	•
	12 V	26 A	•	•	•	•	•	•	•	•

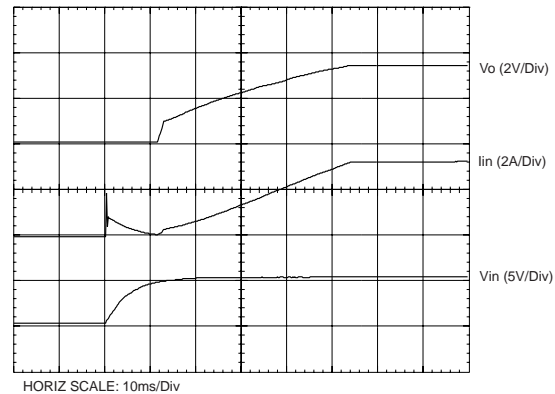
For simple point-of-use applications, the ATH06 (6A) provides operating features such as an on/off inhibit, output voltage trim, pre-bias startup (3.3/5-V input only), and over-current protection. The ATH10 (10 A), and ATH12/15 (12/15 A) include an output voltage sense, and margin up/down controls. Then the higher output current, ATH18/22 (18/22A) and ATH26/30 (26/30A) products incorporate over-temperature shutdown protection. All of the products referenced in Table 3-1 include Auto-Track™.

This is a feature unique to the ATH family, and was specifically designed to simplify the task of sequencing the supply voltage in a power system. These and other features are described in the following sections.

#### Power-Up Characteristics

When configured per their standard application all the ATH products will produce a regulated output voltage following the application of a valid input source voltage. All the modules include soft-start circuitry. This slows the initial rate in which the output voltage can rise, thereby limiting the amount of in-rush current that can be drawn from the input source. The soft-start circuitry also introduces a short time delay (typically 5 ms-10 ms) into the power-up characteristic. This delay is from the point that a valid input source is recognized, to the initial rise of the output voltage. Figure 3-1 shows the power-up characteristic of the 22-A output product (ATH22T05-9xx), operating from a 5-V input bus and configured for a 3.3-V output. The waveforms were measured with a 5-A resistive load. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors.

**Figure 3-1**



#### Over-Current Protection

For protection against load faults, all modules incorporate output over-current protection. Applying a load that exceeds the regulator’s over-current threshold will cause the regulated output to shut down. Following shutdown a module will periodically attempt to recover by initiating a soft-start power-up. This is described as a “hiccup” mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

### Output On/Off Inhibit

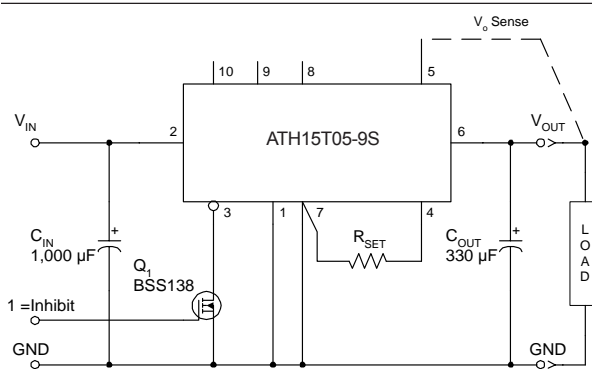
For applications requiring output voltage on/off control, each series of the ATH family incorporates an output *Inhibit* control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the *Inhibit* pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to  $V_{in}$  with respect to *GND*.

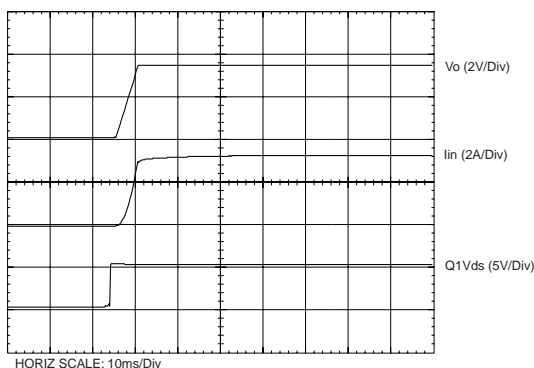
Figure 3-2 shows the typical application of the inhibit function. Note the discrete transistor ( $Q_1$ ). The *Inhibit* control has its own internal pull-up to  $V_{in}$  potential. The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

Turning  $Q_1$  on applies a low voltage to the *Inhibit* control pin and disables the output of the module. If  $Q_1$  is then turned off, the module will execute a soft-start power-up sequence. A regulated output voltage is produced within 20 msec. Figure 3-3 shows the typical rise in both the output voltage and input current, following the turn-off of  $Q_1$ . The turn off of  $Q_1$  corresponds to the rise in the waveform,  $Q_1 V_{ds}$ . The waveforms were measured with a 5-A load.

**Figure 3-2**



**Figure 3-3**



### Remote Sense

The ATH10, ATH12/15, ATH18/22, and ATH26/30 products incorporate an output voltage sense pin,  $V_o Sense$ . The  $V_o Sense$  pin should be connected to  $V_{out}$  at the load circuit (see data sheet standard application). A remote sense improves the load regulation performance of the module by allowing it to compensate for any ‘IR’ voltage drop between itself and the load. An IR drop is caused by the high output current flowing through the small amount of pin and trace resistance. Use of the remote sense is optional. If not used, the  $V_o Sense$  pin can be left open-circuit. An internal low-value resistor (15- $\Omega$  or less) is connected between the  $V_o Sense$  and  $V_{out}$ . This ensures the output voltage remains in regulation.

With the sense pin connected, the difference between the voltage measured directly between the  $V_{out}$  and *GND* pins, and that measured from  $V_o Sense$  to *GND*, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

*Note: The remote sense feature is not designed to compensate for the forward drop of non-linear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.*

### Over-Temperature Protection

The ATH18/22 and ATH26/30 series of products have over-temperature protection. These products have an on-board temperature sensor that protects the module’s internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module’s *Inhibit* control is automatically pulled low. This turns the output off. The output voltage will drop as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the the sensed temperature decreases by about 10 °C below the trip point.

*Note: The over-temperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and will reduce the long-term reliability of the module. Always operate the regulator within the specified Safe Operating Area (SOA) limits for the worst-case conditions of ambient temperature and airflow.*



#### Auto-Track™ Function

The Auto-Track™ function is unique to the ATH family, and is available with the all “Point-of-Load Alliance” (POLA) products. Auto-Track™ was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications, that use dual-voltage VLSI ICs such as DSPs, micro-processors, and ASICs.

#### How Auto-Track™ Works

Auto-Track™ works by forcing the module’s output voltage to follow a voltage presented at the *Track* control pin. This control range is limited to between 0 V and the module’s set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module’s output remains at its set-point <sup>1</sup>. As an example, if the *Track* pin of a 2.5-V regulator is at 1 V, the regulated output will be 1 V. But if the voltage at the *Track* pin rises to 3 V, the regulated output will not go higher than 2.5 V.

When under track control, the regulated output from the module follows the voltage at its *Track* pin on a volt-for-volt basis. By connecting the *Track* pin of a number of these modules together, the output voltages will follow a common signal during power-up and power-down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit <sup>3</sup>. The *Track* control also incorporates an internal RC charge circuit. This operates off the module’s input voltage to produce a suitable rising waveform at power up.

#### Typical Application

The basic implementation of Auto-Track™ allows for simultaneous voltage sequencing of a number of Auto-Track™ compliant modules. Connecting the *Track* control pins of two or more modules forces the *Track* control of all modules to follow the same collective RC ramp waveform, and allows them to be controlled through a single transistor or switch; Q<sub>1</sub> in Figure 3-4.

To initiate a power-up sequence, it is recommended that the *Track* control be first pulled to ground potential. This should be done at or before input power is applied to the modules, and then held for at least 10 ms thereafter. This brief period gives the modules time to complete their internal soft-start initialization. Applying a logic-level high signal to the circuit’s On/Off Control turns Q<sub>1</sub> on and applies a ground signal to the *Track* pins. After completing their internal soft-start initialization, the output of all modules will remain at zero volts while Q<sub>1</sub> is on.

10 ms after a valid input voltage has been applied to the modules, Q<sub>1</sub> may be turned off. This allows the track control voltage to automatically rise toward to the modules’ input voltage. During this period the output voltage of

each module will rise in unison with other modules, to its respective set-point voltage.

Figure 3-5 shows the output voltage waveforms from the circuit of Figure 3-4 after the On/Off Control is set from a high to a low-level voltage. The waveforms, V<sub>O1</sub> and V<sub>O2</sub> represent the output voltages from the two power modules, U<sub>1</sub> (3.3 V) and U<sub>2</sub> (2.0 V) respectively. V<sub>O1</sub> and V<sub>O2</sub> are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. Power down is the reverse of power up, and is accomplished by lowering the track control voltage back to zero volts. The important constraint is that a valid input voltage must be maintained until the power down is complete. It also requires that Q<sub>1</sub> be turned off relatively slowly. This is so that the *Track* control voltage does not fall faster than Auto-Track’s slew rate capability, which is 5 V/ms. The components R<sub>1</sub> and C<sub>1</sub> in Figure 3-4 limit the rate at which Q<sub>1</sub> can pull down the *Track* control voltage. The values of 100 k-ohm and 0.047 μF correlate to a decay rate of about 0.6 V/ms.

The power-down sequence is initiated with a low-to-high transition at the On/Off Control input to the circuit. Figure 3-6 shows the power-down waveforms. As the *Track* control voltage falls below the nominal set-point voltage of each power module, then its output voltage decays with all the other modules under Auto-Track™ control.

#### Notes on Use of Auto-Track™

1. The *Track* pin voltage must be allowed to rise above the module’s set-point voltage before the module can regulate at its adjusted set-point voltage.
2. The Auto-Track™ function will track almost any voltage ramp during power up, and is compatible with ramp speeds of up to 5 V/ms.
3. The absolute maximum voltage that may be applied to the *Track* pin is V<sub>in</sub>.
4. The module will not follow a voltage at its *Track* control input until it has completed its soft-start initialization. This takes about 10 ms from the time that the module has sensed that a valid voltage has been applied its input. During this period, it is recommended that the *Track* pin be held at ground potential.
5. Once its soft-start initialization is complete, the module is capable of both sinking and sourcing current when following the voltage at the *Track* pin.
6. The Auto-Track™ function can be disabled by connecting the *Track* pin to the input voltage (V<sub>in</sub>) through a 1-kΩ resistor. When Auto-Track™ is disabled, the output voltage will rise faster following the application of input power.

\*\*Auto-Track is a trademark of Texas Instruments, Inc.

# Application Notes

## ATH Series of Wide-Output Adjust Power Modules (3.3/5-V Input)

Figure 3-4; Sequenced Power Up & Power Down Using Auto-Track

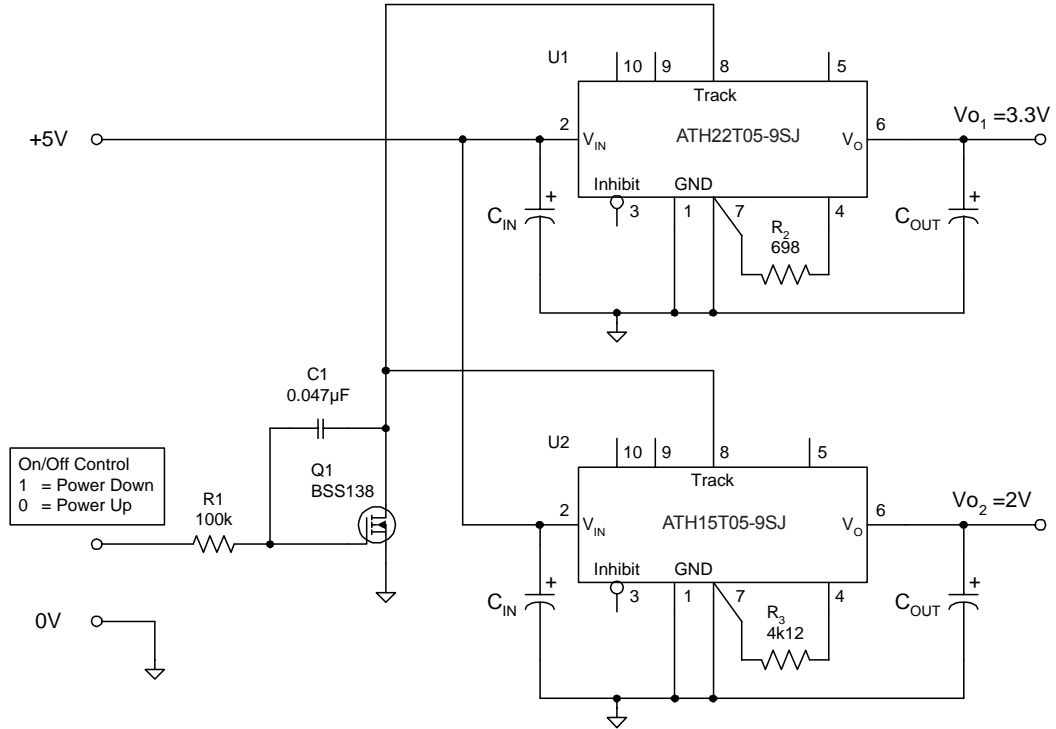


Figure 3-5; Simultaneous Power Up with Auto-Track Control

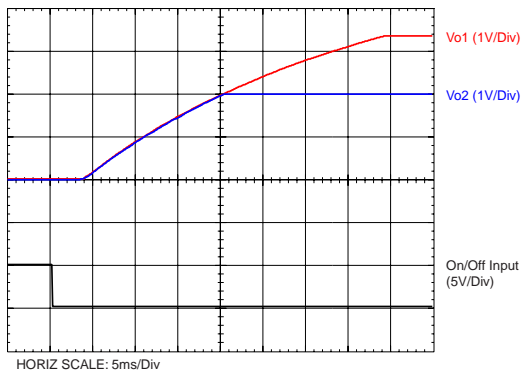
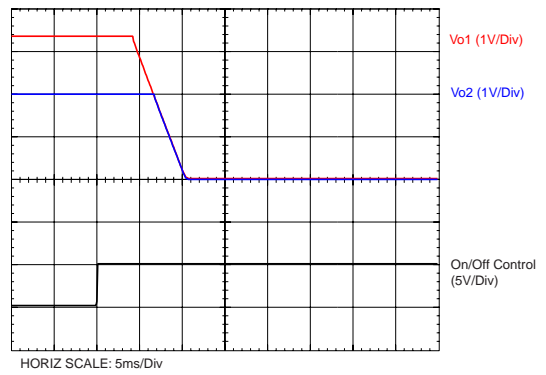


Figure 3-6; Simultaneous Power Down with Auto-Track Control



### Margin Up/Down Controls

The ATH10 (10A), ATH12/15 (12/15A), ATH18/22 (18/22A) and ATH26/30 (26/30A) products incorporate *Margin Up* and *Margin Down* control inputs. These controls allow the output voltage to be momentarily adjusted <sup>1</sup>, either up or down, by a nominal 5 %. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. The  $\pm 5\%$  change is applied to the adjusted output voltage, as set by the external resistor,  $R_{SET}$  at the  $V_o$  Adjust pin.

The 5 % adjustment is made by pulling the appropriate margin control input directly to the *GND* terminal <sup>2</sup>. A low-leakage open-drain device, such as an n-channel MOSFET or p-channel JFET is recommended for this purpose <sup>3</sup>. Adjustments of less than 5 % can also be accommodated by adding series resistors to the control inputs (See Figure 3-4). The value of the resistor can be selected from Table 3-2, or calculated using the following formula.

### Up/Down Adjust Resistance Calculation

To reduce the margin adjustment to something less than 5 %, series resistors are required (See  $R_D$  and  $R_U$  in Figure 3-7). For the same amount of adjustment, the resistor value calculated for  $R_U$  and  $R_D$  will be the same. The formulas is as follows.

$$R_U \text{ or } R_D = \frac{499}{\Delta\%} - 99.8 \quad \text{k}\Omega$$

Where  $\Delta\%$  = The desired amount of margin adjust in percent.

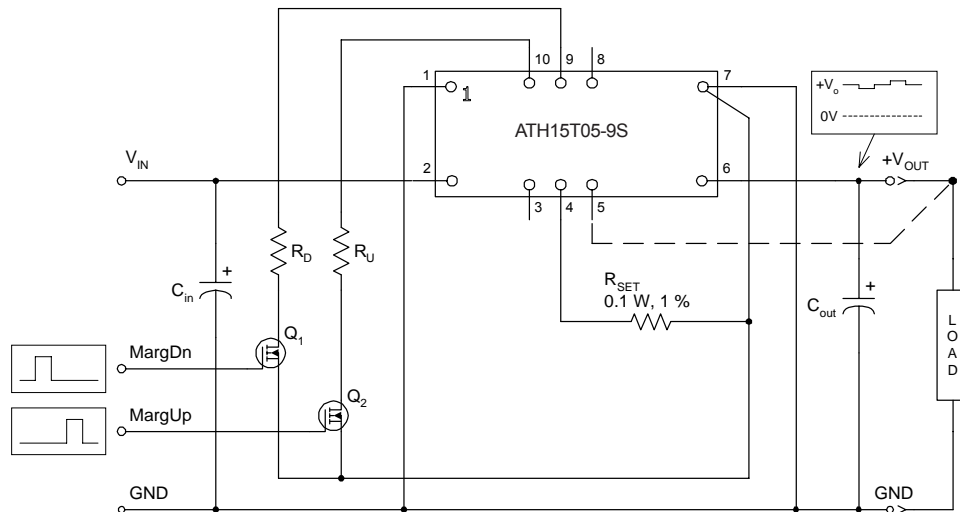
### Notes:

1. The *Margin Up*\* and *Margin Dn*\* controls were not intended to be activated simultaneously. If they are their affects on the output voltage may not completely cancel, resulting in the possibility of a slightly higher error in the output voltage set point.
2. The ground reference should be a direct connection to the module *GND* at pin 7 (pin 1 for the ATH06). This will produce a more accurate adjustment at the load circuit terminals. The transistors  $Q_1$  and  $Q_2$  should be located close to the regulator.
3. The Margin Up and Margin Dn control inputs are not compatible with devices that source voltage. This includes TTL logic. These are analog inputs and should only be controlled with a true open-drain device (preferably a discrete MOSFET transistor). The device selected should have low off-state leakage current. Each input sources 8  $\mu$ A when grounded, and has an open-circuit voltage of 0.8 V.

**Table 3-2; Margin Up/Down Resistor Values**

% Adjust	$R_U / R_D$
5	0.0 k $\Omega$
4	24.9 k $\Omega$
3	66.5 k $\Omega$
2	150.0 k $\Omega$
1	397.0 k $\Omega$

**Figure 3-7; Margin Up/Down Application Schematic**



### Pre-Bias Startup Capability

Only selected products in the ATH family incorporate this capability. Consult Table 3-1 to identify which products are compliant.

A pre-bias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, these types of modules can sink as well as source output current.

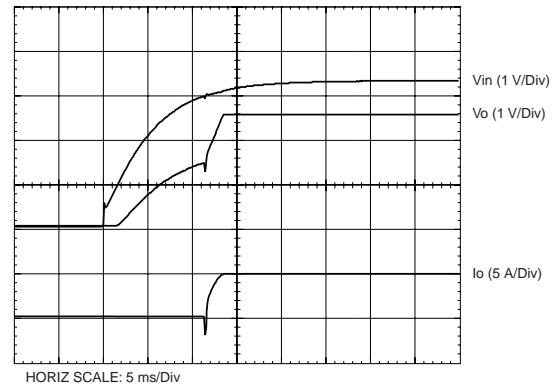
The ATH family of power modules incorporate synchronous rectifiers, but will not sink current during startup<sup>1</sup>, or whenever the *Inhibit* pin is held low. However, to ensure satisfactory operation of this function, certain conditions must be maintained.<sup>2</sup> Figure 3-7 shows an application demonstrating the pre-bias startup capability. The startup waveforms are shown in Figure 3-9. Note that the output current from the ATH15T033-9xx ( $I_o$ ) shows negligible current until its output voltage rises above that backed through diodes  $D_1$  and  $D_2$ .

*Note: The pre-bias start-up feature is not compatible with Auto-Track. When the module is under Auto-Track control, it is fully active and will sink current if the output voltage is below that of a back-feeding source. Therefore to ensure a pre-bias hold-off, one of two approaches must be followed when input power is applied to the module. The Auto-Track function must either be disabled<sup>3</sup>, or the module's output held off using the *Inhibit* pin. The latter allows Auto-Track's internal (RC) voltage ramp to rise above the set-point voltage.*

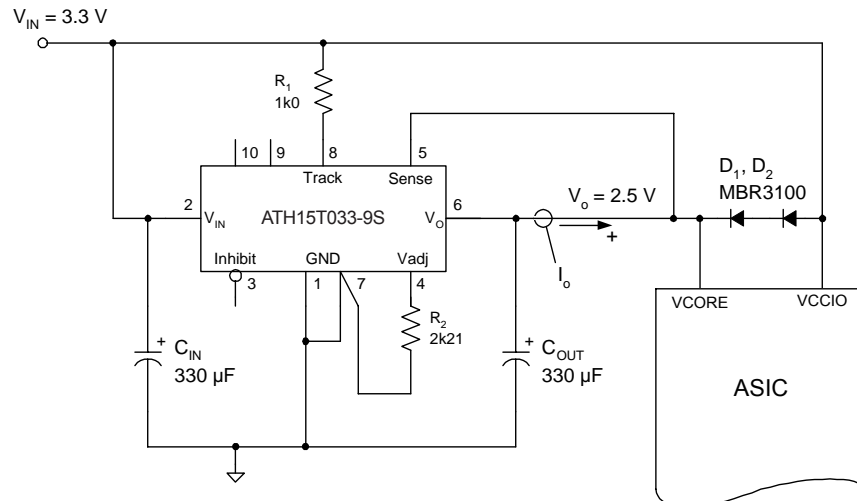
### Notes

1. Startup is the relatively short period (approx. 10 ms) prior to the output voltage rising. The startup period immediately follows either the application of a valid input source voltage, or the release of a ground signal at the *Inhibit* pin.
2. To ensure that the regulator does not sink current when power is first applied (even with a ground signal applied to the *Inhibit* control pin), the input voltage must always be greater than the output voltage throughout the power-up and power-down sequence.
3. The Auto-Track function can be disabled at power up by immediately applying a voltage to the module's *Track* pin that is greater than its set-point voltage. This can be easily accomplished by connecting the *Track* pin to  $V_{in}$  through a 1-k $\Omega$  resistor.

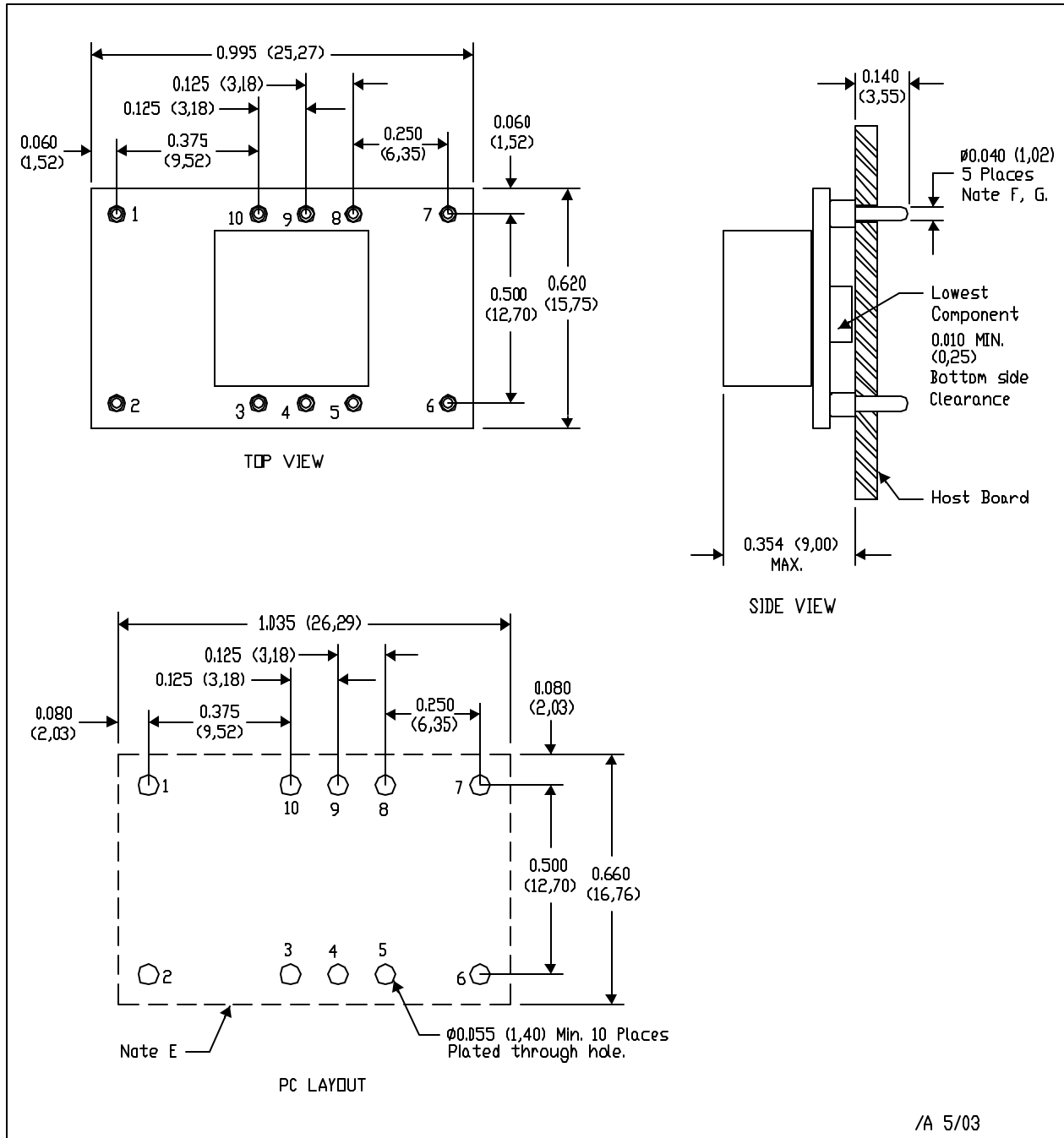
**Figure 3.9; Pre-Bias Startup Waveforms**



**Figure 3.8; Application Circuit Demonstrating Pre-Bias Startup**



# Through Hole Termination

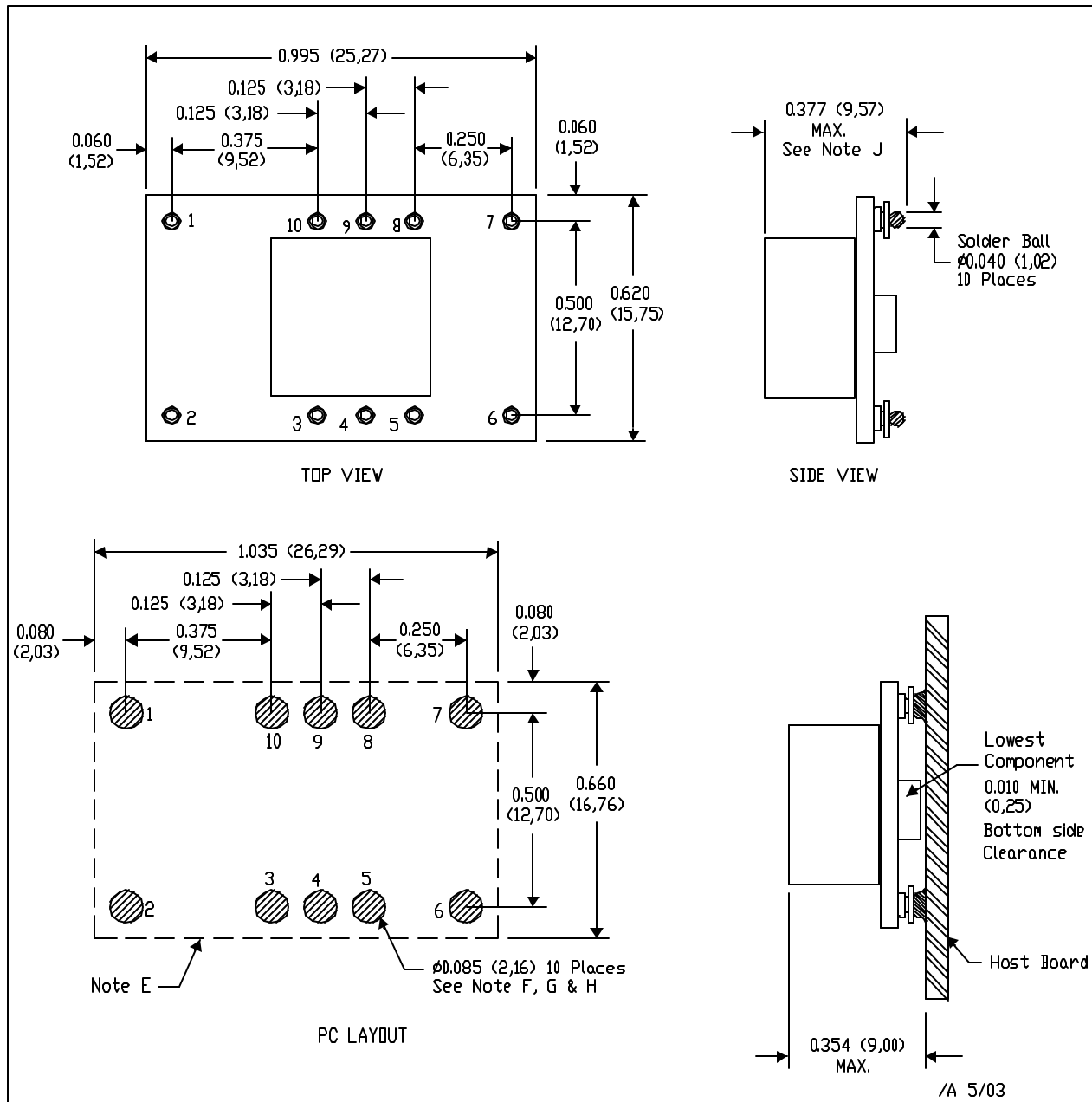


/A 5/03

- NOTES:
- A. All linear dimensions are in inches (mm).
  - B. This drawing is subject to change without notice.
  - C. 2 place decimals are  $\pm 0.030$  ( $\pm 0,76$ mm).
  - D. 3 place decimals are  $\pm 0.010$  ( $\pm 0,25$ mm).
  - E. Recommended keep out area for user components

- E. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
- F. All pins: Material - Copper Alloy  
Finish - Tin (100%) over Nickel plate

## Surface Mount Termination



- NOTES:
- All linear dimensions are in inches (mm).
  - This drawing is subject to change without notice.
  - 2 place decimals are  $\pm 0.030$  ( $\pm 0,76$ mm).
  - 3 place decimals are  $\pm 0.010$  ( $\pm 0,25$ mm).
  - Recommended keep out area for user components.
  - Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).

- Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
- Pad type: Solder mask defined.
- All pins: Material - Copper Alloy  
Finish - Tin (100%) over Nickel plate  
Solder Ball - See product data sheet.
- Dimension prior to reflow solder.