

## 1. Product profile

### 1.1 General description

Ultra low level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Higher operating power due to low thermal resistance
- Low conduction losses due to low on-state resistance
- Interfaces directly with low voltage gate drivers

### 1.3 Applications

- DC-to-DC convertors
- Portable equipment
- Notebook computers
- Switched-mode power supplies

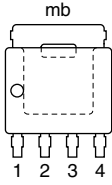
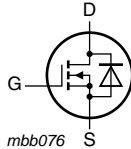
### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	25	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 4.5\text{ V}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	100	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	62.5	W
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 4.5\text{ V}$ ; $I_D = 50\text{ A}$ ; $V_{DS} = 10\text{ V}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	-	20.2	-	nC
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 8</a> ; see <a href="#">Figure 9</a>	-	2.3	3	m $\Omega$

## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>SOT669 (LFPAK)</b></p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 3. Ordering information

**Table 3. Ordering information**

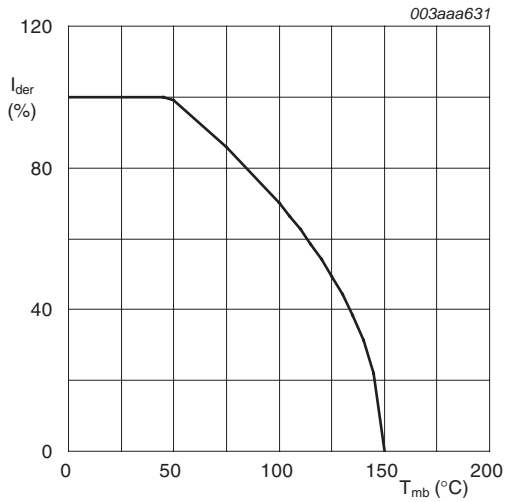
Type number	Package		Version
	Name	Description	
PH2925U	LFPAK	plastic single-ended surface-mounted package (LFPAK); 4 leads	SOT669

## 4. Limiting values

**Table 4. Limiting values**

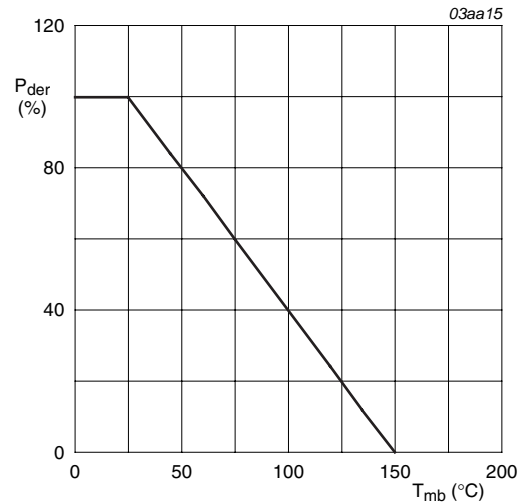
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	25	V
$V_{DGR}$	drain-gate voltage	$T_j \leq 150\text{ °C}$ ; $T_j \geq 25\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	25	V
$V_{GS}$	gate-source voltage		-10	10	V
$I_D$	drain current	$V_{GS} = 4.5\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	-	70	A
		$V_{GS} = 4.5\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	100	A
$I_{DM}$	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	300	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	62.5	W
$T_{stg}$	storage temperature		-55	150	°C
$T_j$	junction temperature		-55	150	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	52	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	150	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 70.7\text{ A}$ ; $V_{sup} \leq 25\text{ V}$ ; unclamped; $t_p = 0.22\text{ ms}$ ; $R_{GS} = 50\text{ }\Omega$	-	250	mJ



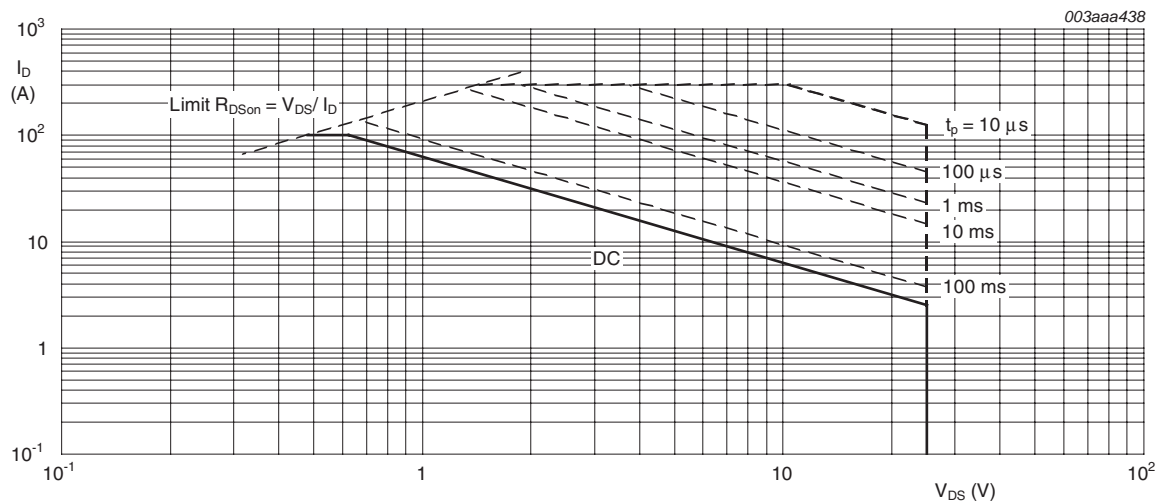
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



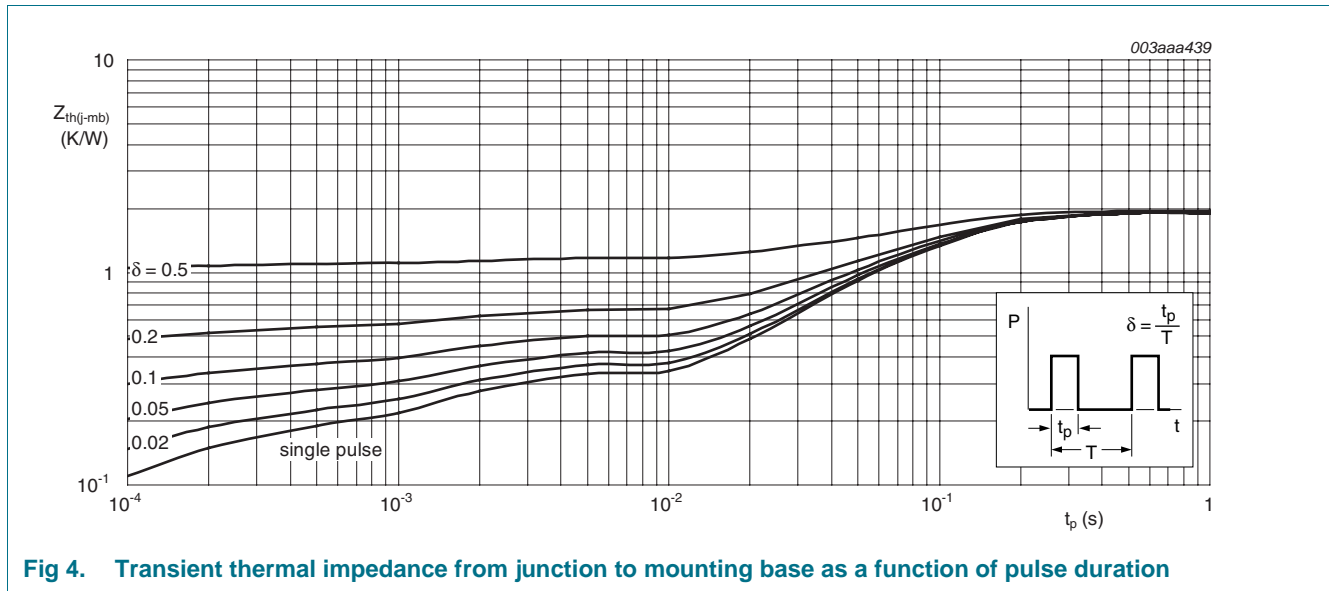
$T_{mb} = 25^\circ\text{C}; I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

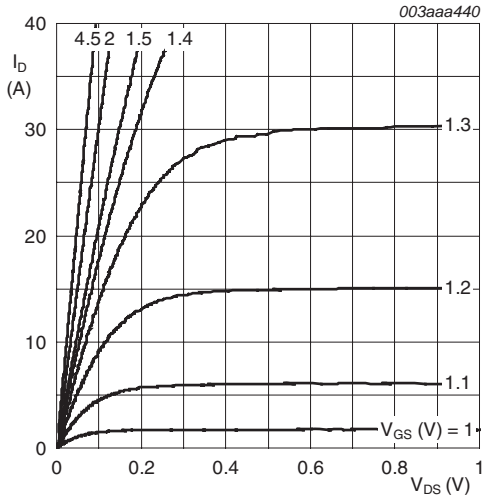
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	2	K/W



## 6. Characteristics

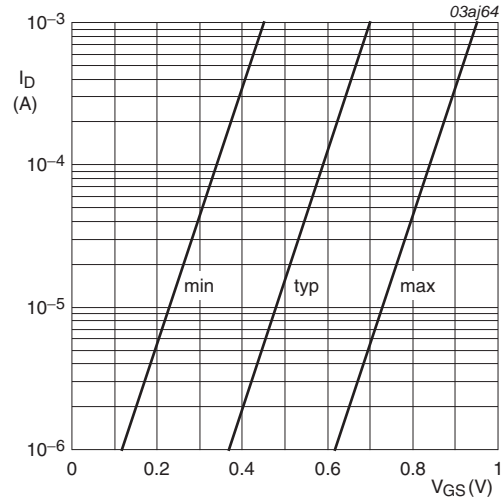
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	22.5	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	25	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; see <a href="#">Figure 6</a> ; see <a href="#">Figure 7</a>	-	-	1.2	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 6</a> ; see <a href="#">Figure 7</a>	0.25	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 7</a> ; see <a href="#">Figure 6</a>	0.45	0.7	0.95	V
$I_{DSS}$	drain leakage current	$V_{DS} = 25 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	500	$\mu A$
		$V_{DS} = 25 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.06	1	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	20	100	nA
		$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	20	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5 V; I_D = 25 A; T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 8</a> ; see <a href="#">Figure 9</a>	-	3.6	4.8	m $\Omega$
		$V_{GS} = 2.5 V; I_D = 25 A; T_j = 25 \text{ }^\circ C$	-	3.2	4.2	m $\Omega$
		$V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 8</a> ; see <a href="#">Figure 9</a>	-	2.3	3	m $\Omega$
$R_G$	internal gate resistance (AC)	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	-	1.55	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 50 A; V_{DS} = 10 V; V_{GS} = 4.5 V; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	-	92	-	nC
$Q_{GS}$	gate-source charge		-	12	-	nC
$Q_{GD}$	gate-drain charge		-	20.2	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 50 A; V_{DS} = 10 V; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 10</a> ; see <a href="#">Figure 11</a>	-	1.6	-	V
$C_{iss}$	input capacitance	$V_{DS} = 10 V; V_{GS} = 0 V; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>	-	6150	-	pF
$C_{oss}$	output capacitance		-	1170	-	pF
$C_{riss}$	reverse transfer capacitance		-	814	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10 V; R_L = 1 \Omega; V_{GS} = 4.5 V; R_{G(ext)} = 4.7 \Omega; T_j = 25 \text{ }^\circ C$	-	30	-	ns
$t_r$	rise time		-	80	-	ns
$t_{d(off)}$	turn-off delay time		-	258	-	ns
$t_f$	fall time		-	114	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25 A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 13</a>	-	0.72	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20 A; di_S/dt = -100 A/\mu s; V_{GS} = 0 V; V_{DS} = 25 V$	-	60	-	ns



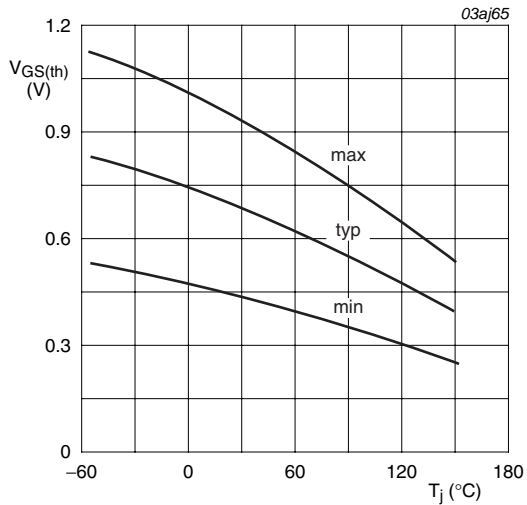
$T_j = 25^\circ C$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



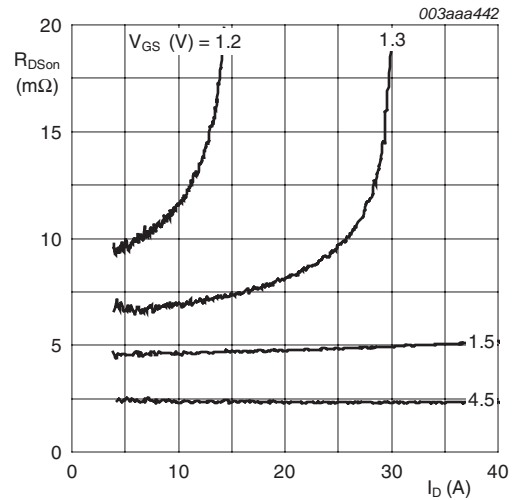
$T_j = 25^\circ C; V_{DS} = 5V$

Fig 6. Sub-threshold drain current as a function of gate-source voltage



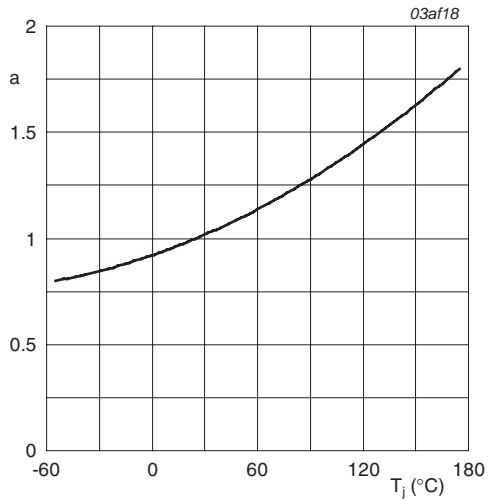
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 7. Gate-source threshold voltage as a function of junction temperature



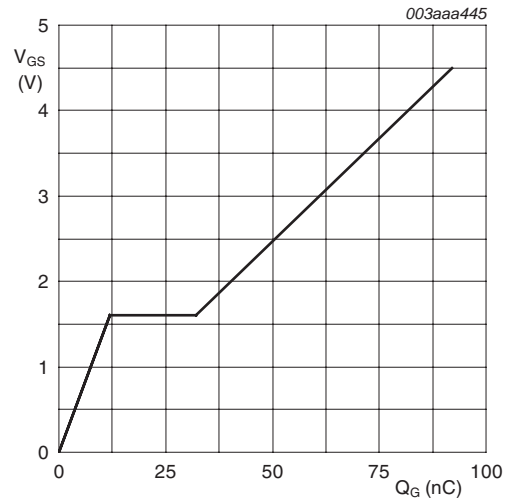
$T_j = 25^\circ C$

Fig 8. Drain-source on-state resistance as a function of drain current; typical values



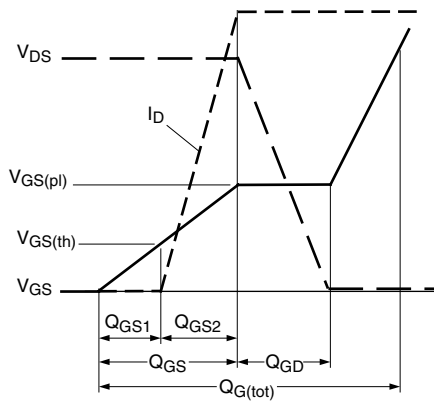
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

**Fig 9. Normalized drain-source on-state resistance factor as a function of junction temperature**



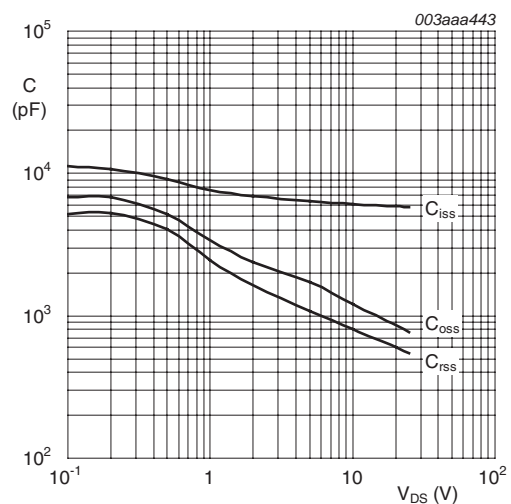
$$I_D = 50A; V_{DS} = 10V$$

**Fig 10. Gate-source voltage as a function of gate charge; typical values**



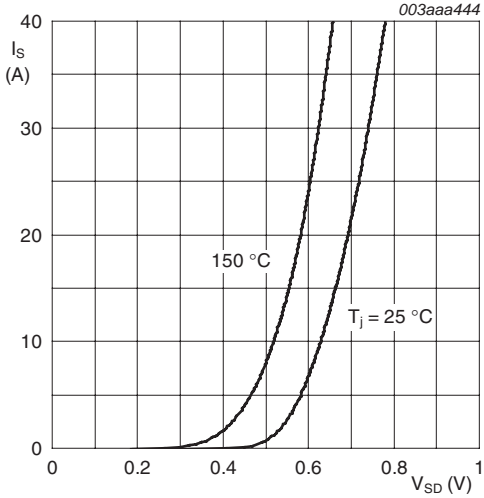
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**Fig 11. Gate charge waveform definitions**



$$V_{GS} = 0V; f = 1MHz$$

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$T_j = 25^\circ\text{C}$  and  $150^\circ\text{C}; V_{GS} = 0\text{V}$

Fig 13. Source current as a function of source-drain voltage; typical values



## 7. Package outline

Plastic single-ended surface-mounted package (LFAK); 4 leads

SOT669

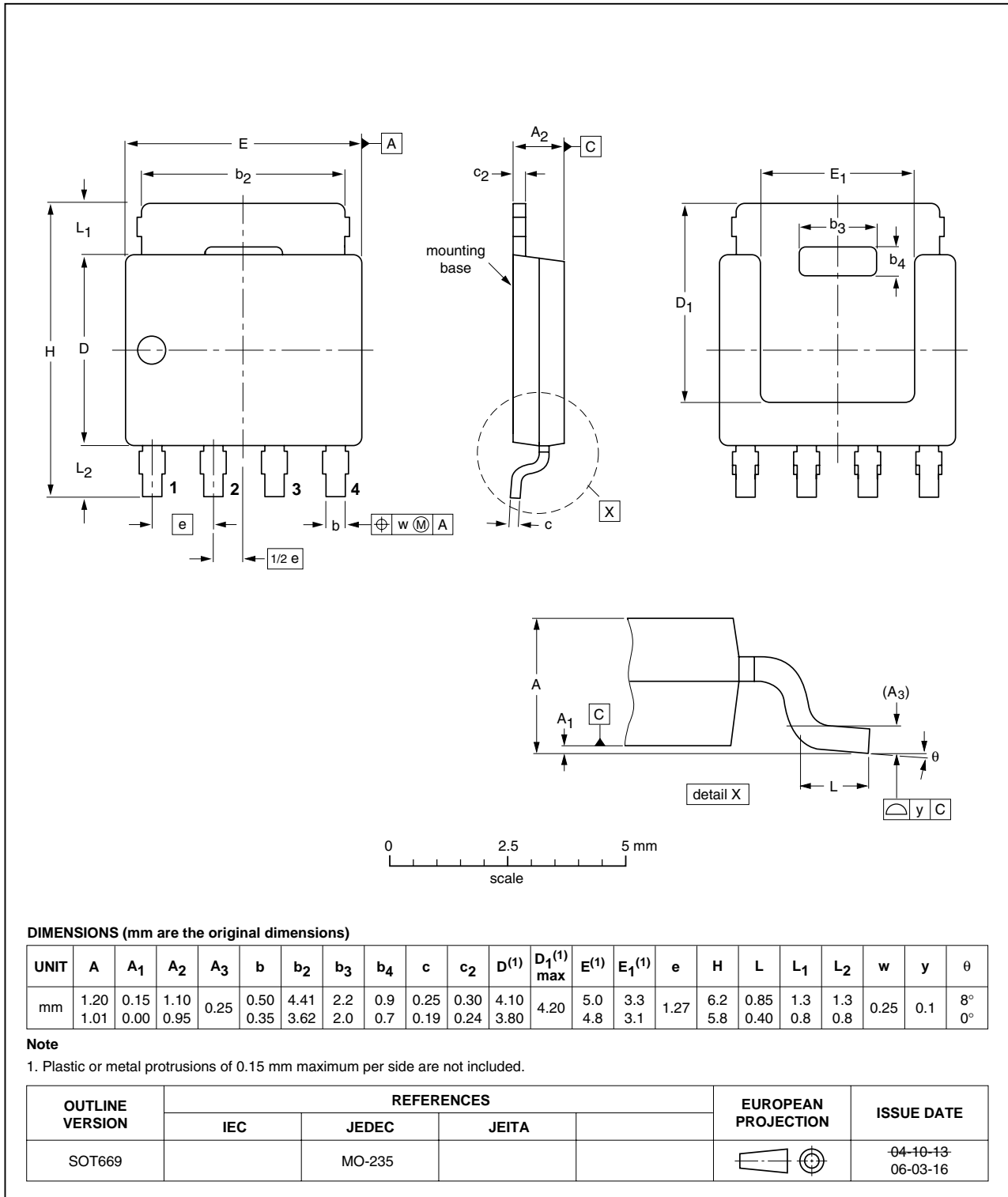


Fig 14. Package outline SOT669 (LFAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH2925U_4	20090224	Product data sheet	-	PH2925U_3
Modifications:		<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li></ul>		
PH2925U_3	20051129	Product data sheet	-	PH2925U-02
PH2925U-02 (9397 750 13064)	20040408	Product data	-	PH2925U-01
PH2925U-01 (9397 750 11407)	20030502	Product data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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