DDR3 SDRAM
Unbuffered SODIMM
Based on 2Gb M version

HMT451S6MMP(R)8C

** Contents are subject to change without prior notice.

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Release	Oct. 2008	
0.2	IDD Update	Apr. 2009	

Table of Contents

1. Description

This Hynix unbuffered Small Outline Dual In-Line Memory Module (SODIMM) series consists of 2Gb M version. DDR3 SDRAMs in Fine Ball Grid Array (FBGA) packages on a 204 pin glass-epoxy substrate. This DDR3 Unbuffered SODIMM series based on 2Gb M ver. provide a high performance 8 byte interface in 67.60mm width form factor of industry standard. It is suitable for easy interchange and addition.

1.1 Device Features & Ordering Information

1.1.1 Features

- VDD=VDDQ=1.5V
- VDDSPD=3.0V to 3.6V
- Fully differential clock inputs (CK, /CK) operation
- Differential Data Strobe (DQS, /DQS)
- On chip DLL align DQ, DQS and /DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5, 6, 7, 8, 9, 10, and (11) supported
- Programmable additive latency 0, CL-1 and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8 banks
- 8K refresh cycles /64ms
- DDR3 SDRAM Package: JEDEC standard 82ball FBGA(x4/x8) with support balls
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- Auto Self Refresh supported
- 8 bit pre-fetch

1.1.2 Ordering Information

Part Name	Density	Organization	# of DRAMs	# of ranks	Materials
HMT451S6MMP8C-S6/G7*	4GB	512Mx64	16	2	Lead free
HMT451S6MMR8C-S6/G7*	4GB	512Mx64	16	2	Halogen free

*Information on temperature sensor can be found on the label:
T0 indicates that the DIMM has temperature sensor.
N0 indicates that the DIMM does not have temperature sensor.

1.2 Speed Grade & Key Parameters

MT/S	DDR3-800	DDR3-1066	Unit
Grade	-S6	-G7	
tCK (min)	2.5	1.875	ns
CAS Latency	6	7	tCK
tRCD (min)	15	13.125	ns
tRP (min)	15	13.125	ns
tRAS (min)	37.5	37.5	ns
tRC (min)	52.5	50.625	ns
CL-tRCD-tRP	6-6-6	7-7-7	tCK

1.3 Address Table

	4GB
Organization	512M x 64
Refresh Method	8K/64ms
Row Address	A0-A14
Column Address	A0-A9
Bank Address	BA0-BA2
Page Size	1KB
# of Rank	2
# of Device	16

2. Pin Architecture

2.1 Pin Definition

Pin Name	Description		Pin Name	Description	
CK[1:0]	Clock Inputs, positive line	2	DQ[63:0]	Data Input/Output	64
$\overline{CK}$[1:0]	Clock Inputs, negative line	2	DM[7:0]	Data Masks	8
CKE[1:0]	Clock Enables	2	DQS[7:0]	Data strobes	8
$\overline{RAS}$	Row Address Strobe	1	$\overline{DQS}$[7:0]	Data strobes complement	8
$\overline{CAS}$	Column Address Strobe	1	$\overline{RESET}$	Reset pin	1
$\overline{WE}$	Write Enable	1	TEST	Logic Analyzer specific test pin (No connect on SODIMM)	1
$\overline{S}$[1:0]	Chip Selects	2	$\overline{EVENT}$	Temperature event pin	1
A[9:0], A11, A[15:13]	Address Inputs	14	V_{DD}	Core and I/O power	18
A10/AP	Address Input/Autoprecharge	1	V_{SS}	Ground	52
A12/$\overline{BC}$	Address Input/Burst Stop	1	V_{REF}DQ	Input/Output Reference	2
BA[2:0]	SDRAM Bank Address	3	V_{REF}CA		
$\overline{ODT}$[1:0]	On-die termination control	2	V_{DD}SPD	SPD and Temp sensor power	1
SCL	Serial Presence Detect (SPD) Clock input	1	Vtt	Termination voltage	2
SDA	SPD Data Input/Output	1	NC	Reserved for future use	2
$\overline{SA}$[1:0]	SPD address	2		Total	204

2.2 Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0/$\overline{CK}$0 CK1/$\overline{CK}$1	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{CK}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE[1:0]	Input	Active High	Activates the DDR3 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{S}$[1:0]	Input	Active Low	Enables the associated DDR3 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by $\overline{S}$0; Rank 1 is selected by $\overline{S}$1.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Active Low	When sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$, signals $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA[2:0]	Input	-	Selects which DDR3 SDRAM internal bank of eight is activated.
ODT[1:0]	Input	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{DQS}$ signals if enabled via the DDR3 SDRAM mode register.
A[9:0], A10/$\overline{AP}$, A11, A12/$\overline{BC}$, A[15:13]	Input	-	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{CK}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge. A12($\overline{BC}$) is sampled during READ and WRITE commands to determine if burst chop (on-thefly) will be performed (HIGH, no burst chop; LOW, burst chopped)
DQ[63:0]	In/Out	-	Data Input/Output pins.
DM[7:0]	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS[7:0], $\overline{DQS}$[7:0]	In/Out	Cross Point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR3 SDRAMs and is sent at the leading edge of the data window. $\overline{DQS}$ signals are complements, and timing is relative to the crosspoint of respective DQS and $\overline{DQS}$.

Symbol	Type	Polarity	Function
V_{DD},V_{DD}SPD, V_{SS},	Supply		Power supplies for core, I/O, Serial Presence Detect, Temp sensor, and ground for the module.
V_{REF}DQ, V_{REF}CA	Supply		Reference voltage for SSTL15 inputs.
SDA	In/Out		This is a bidirectional pin used to transfer data into or out of the SPD EEPROM and Temp sensor. A resistor must be connected from the SDA bus line to V_{DD}SPD on the system planar to act as a pull up.
SCL	Input		This signal is used to clock data into and out of the SPD EEPROM and Temp sensor.
SA[1:0]	Input		Address pins used to select the Serial Presence Detect and Temp sensor base address.
TEST	In/Out		The TEST pin is reserved for bus analysis tools and is not connected on normal memory modules (SO-DIMMs).
$\overline{\text{EVENT}}$	Wire OR Out	Active Low	The EVENT pin is reserved for use to flag critical module temperature. A resistor may be connected from EVENT bus line to VDDSPD on the system planar to act as a pullup.
$\overline{\text{RESET}}$	In	Active Low	This signal resets the DDR3 SDRAM

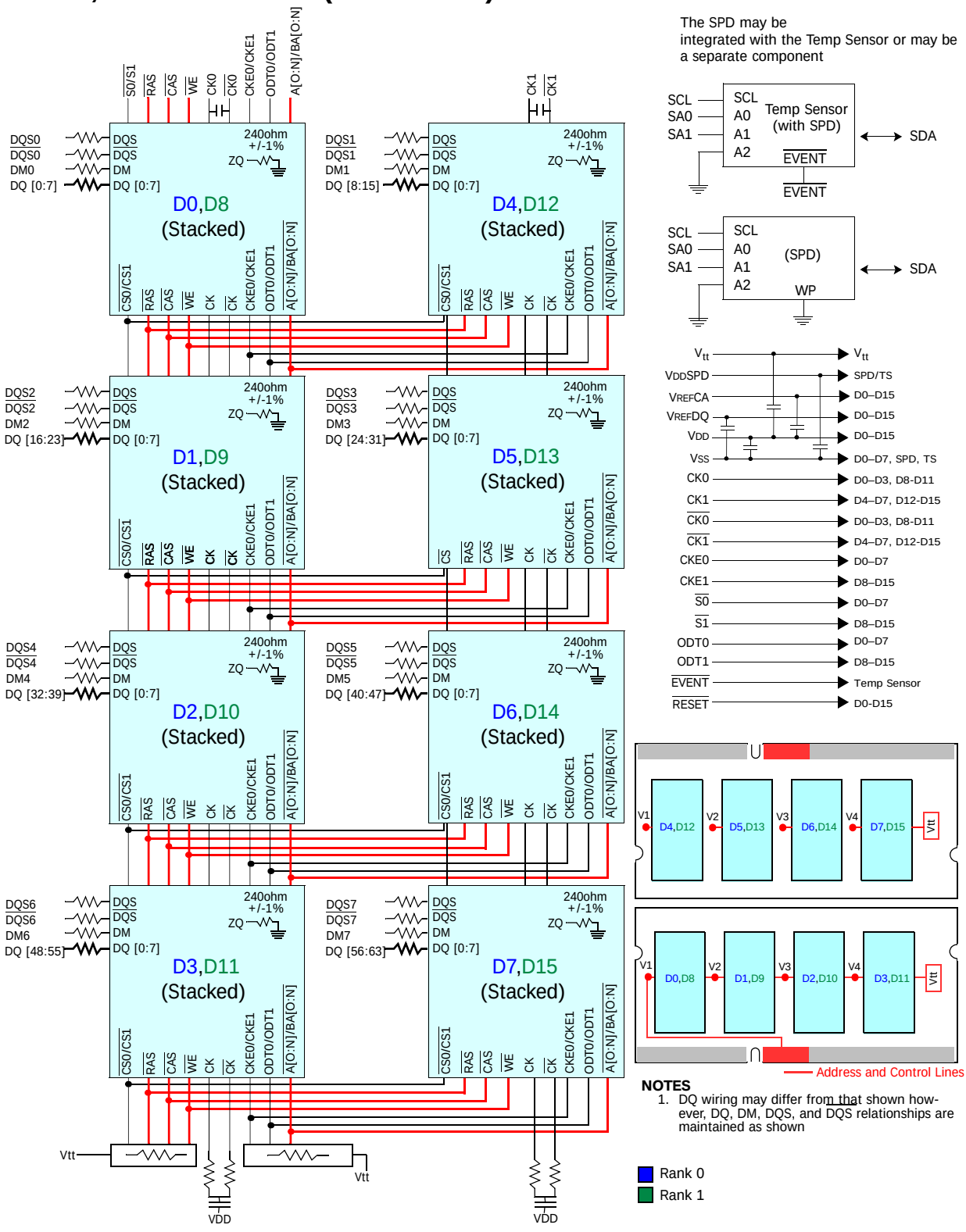
2.3 Pin Assignment

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Sid	Pin #	Back Side
1	$V_{REF}DQ$	2	V_{SS}	53	DQ19	54	V_{SS}	105	V_{DD}	106	V_{DD}	157	DQ42	158	DQ46
3	V_{SS}	4	DQ4	55	V_{SS}	56	DQ28	107	A10/AP	108	BA1	159	DQ43	160	DQ47
5	DQ0	6	DQ5	57	DQ24	58	DQ29	109	BA0	110	$\overline{RAS}$	161	V_{SS}	162	V_{SS}
7	DQ1	8	V_{SS}	59	DQ25	60	V_{SS}	111	V_{DD}	112	V_{DD}	163	DQ48	164	DQ52
9	V_{SS}	10	$\overline{DQS0}$	61	V_{SS}	62	$\overline{DQS3}$	113	$\overline{WE}$	114	$\overline{S0}$	165	DQ49	166	DQ53
11	DM0	12	DQS0	63	DM3	64	DQS3	115	$\overline{CAS}$	116	ODT0	167	V_{SS}	168	V_{SS}
13	V_{SS}	14	V_{SS}	65	V_{SS}	66	V_{SS}	117	V_{DD}	118	V_{DD}	169	$\overline{DQS6}$	170	DM6
15	DQ2	16	DQ6	67	DQ26	68	DQ30	119	A13[2]	120	ODT1	171	DQS6	172	V_{SS}
17	DQ3	18	DQ7	69	DQ27	70	DQ31	121	$\overline{S1}$	122	NC	173	V_{SS}	174	DQ54
19	V_{SS}	20	V_{SS}	71	V_{SS}	72	V_{SS}	123	V_{DD}	124	V_{DD}	175	DQ50	176	DQ55
21	DQ8	22	DQ12	73	CKE0	74	CKE1	125	TEST	126	$V_{REF}CA$	177	DQ51	178	V_{SS}
23	DQ9	24	DQ13	75	V_{DD}	76	V_{DD}	127	V_{SS}	128	V_{SS}	179	V_{SS}	180	DQ60
25	V_{SS}	26	V_{SS}	77	NC	78	A15[2]	129	DQ32	130	DQ36	181	DQ56	182	DQ61
27	$\overline{DQS1}$	28	DM1	79	BA2	80	A14[2]	131	DQ33	132	DQ37	183	DQ57	184	V_{SS}
29	DQS1	30	$\overline{RESET}$	81	V_{DD}	82	V_{DD}	133	V_{SS}	134	V_{SS}	185	V_{SS}	186	$\overline{DQS7}$
31	V_{SS}	32	V_{SS}	83	A12/$\overline{BC}$	84	A11	135	$\overline{DQS4}$	136	DM4	187	DM7	188	DQS7
33	DQ10	34	DQ14	85	A9	86	A7	137	DQS4	138	V_{SS}	189	V_{SS}	190	V_{SS}
35	DQ11	36	DQ15	87	V_{DD}	88	V_{DD}	139	V_{SS}	140	DQ38	191	DQ58	192	DQ62
37	V_{SS}	38	V_{SS}	89	A8	90	A6	141	DQ34	142	DQ39	193	DQ59	194	DQ63
39	DQ16	40	DQ20	91	A5	92	A4	143	DQ35	144	V_{SS}	195	V_{SS}	196	V_{SS}
41	DQ17	42	DQ21	93	V_{DD}	94	V_{DD}	145	V_{SS}	146	DQ44	197	SA0	198	$\overline{EVENT}$
43	V_{SS}	44	V_{SS}	95	A3	96	A2	147	DQ40	148	DQ45	199	VDD_{SPD}	200	SDA
45	$\overline{DQS2}$	46	DM2	97	A1	98	A0	149	DQ41	150	V_{SS}	201	SA1	202	SCL
47	DQS2	48	V_{SS}	99	V_{DD}	100	V_{DD}	151	V_{SS}	152	$\overline{DQS5}$	203	V_{TT}	204	V_{TT}
49	V_{SS}	50	DQ22	101	CK0	102	CK1	153	DM5	154	DQS5				
51	DQ18	52	DQ23	103	$\overline{CK0}$	104	$\overline{CK1}$	155	V_{SS}	156	V_{SS}				

NC = No Connect; RFU = Reserved Future Use

1. TEST (pin 125) is reserved for bus analysis probes and is NC on normal memory modules.
2. This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

3.1 4GB, 512Mx64 Module(2Rank of x8)



NOTES

1. DQ wiring may differ from that shown however, DQ, DM, DQS, and DQS relationships are maintained as shown

4. ABSOLUTE MAXIMUM RATINGS

4.1 Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.975 V	V	,3
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.975 V	V	,3
VIN, VOUT	Voltage on any pin relative to Vss	- 0.4 V ~ 1.975 V	V	
TSTG	Storage Temperature	-55 to +100 ℃	℃	, 2

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be not greater than 0.6XVDDQ,When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

4.2 DRAM Component Operating Temperature Range

Symbol	Parameter	Rating	Units	Notes
TOPER	Normal Temperature Range	0 to 85	℃	,2
	Extended Temperature Range	85 to 95	℃	1,3

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85oC under all operating conditions
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°... and 95°... case temperature.
   Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. (This double refresh requirement may not apply for some devices.) It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/ or the DIMM SPD for option avail ability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, than it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0band MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

5. AC & DC Operating Conditions

5.1 Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

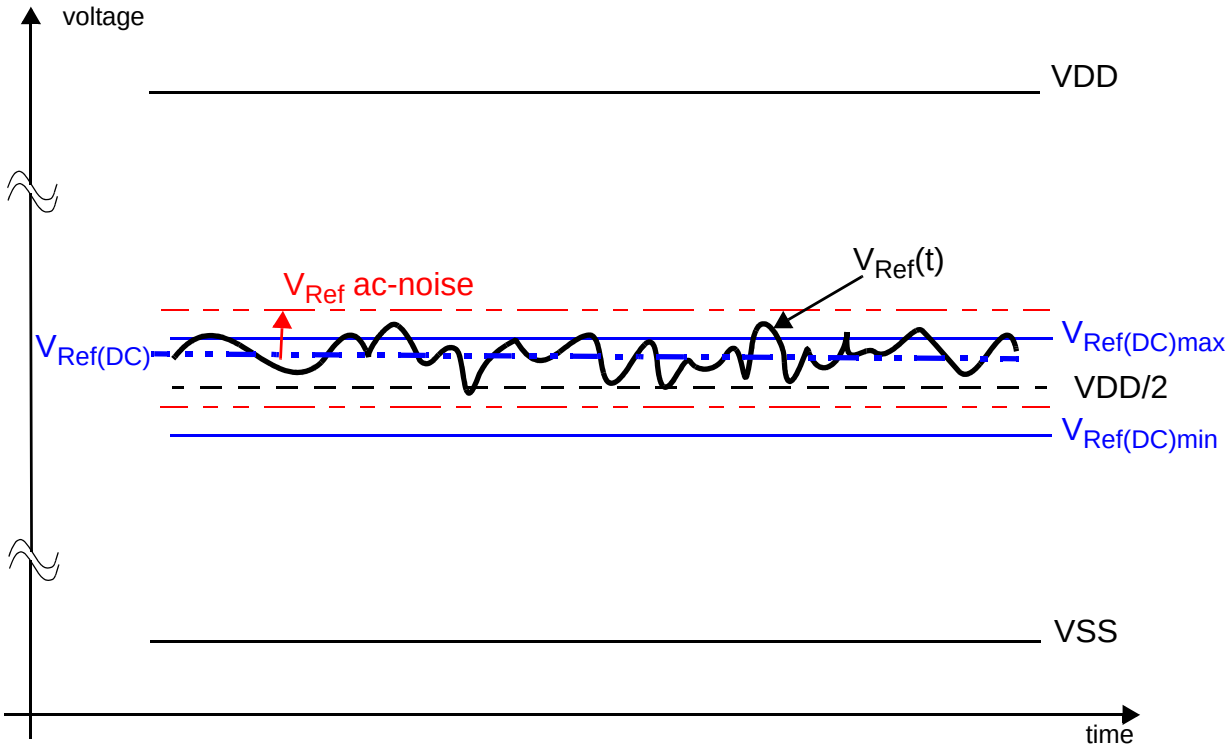
5.2 DC & AC Logic Input Levels

5.2.1 DC & AC Logic Input Levels for Single-Ended Signals

Symbol	Parameter	DDR3-800, DDR3-1066		Unit	Notes
		Min	Max		
VIH(DC)	DC input logic high	Vref + 0.100	-	V	1, 2
VIL(DC)	DC input logic low		Vref - 0.100	V	1, 2
VIH(AC)	AC input logic high	Vref + 0.175	-	V	1, 2
VIL(AC)	AC input logic low		Vref - 0.175	V	1, 2
VRefDQ (DC)	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	3, 4
VRefCA (DC)	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4
VTT	Termination voltage for DQ, DQS outputs	VDDQ/2 - TBD	VDDQ/2 + TBD	V	

1. For DQ and DM, Vref = VrefDQ. For input only pins except RESET#, Vref = VrefCA.
2. The “t.b.d.” entries might change based on overshoot and undershoot specification.
3. The ac peak noise on VRef may not allow VRef to deviate from VRef (DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
   For reference: approx. VDD/2 +/- 15 mV.

The dc-tolerance limits and ac-noise limits for the reference voltages VRefCA and VRefDQ are illustrated in figure 5.2.1. It shows a valid reference voltage VRef (t) as a function of time. (VRef stands for VRefCA and VRefDQ like-wise).VRef(DC) is the linear average of VRef (t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table 1. Furthermore VRef (t) may temporarily deviate from VRef (DC) by no more than +/- 1% VDD.



< Figure 5.2.1: Illustration of Vref (DC) tolerance and Vref AC-noise limits >

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VRef. "VRef " shall be understood as VRef (DC), as defined in Figure.
This clarifies, that dc-variations of VRef affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for VRef (DC) deviations from the optimum position within the data-eye of the input signals.
This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VRef ac-noise. Timing and voltage effects due to ac-noise on VRef up to the specified limit (+/-1% of VDD) are included in DRAM timings and their associated deratings.

5.2.2 DC & AC Logic Input Levels for Differential Signals

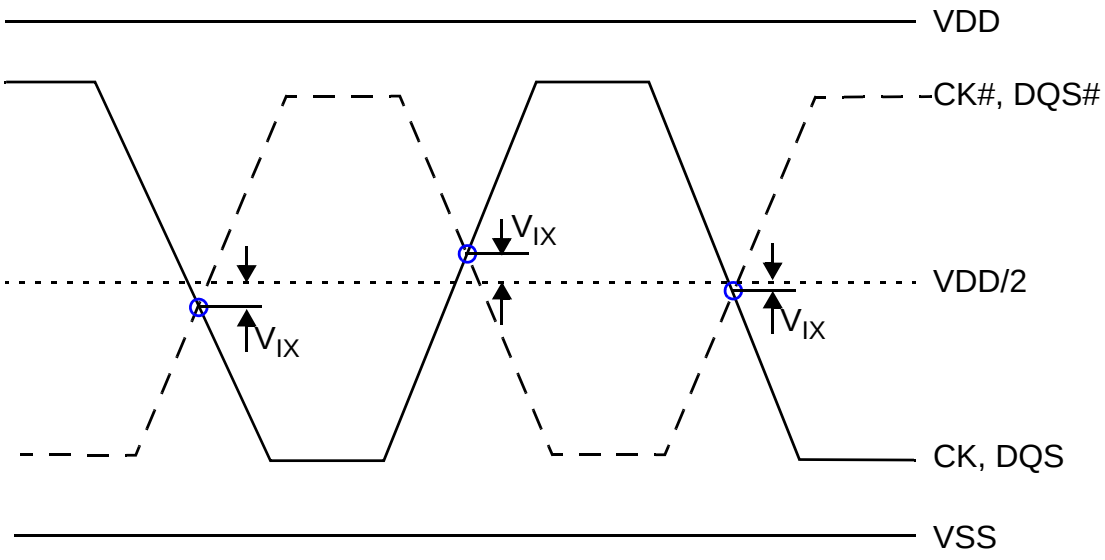
Symbol	Parameter	DDR3-800, DDR3-1066		Unit	Notes
		Min	Max		
VIHdiff	Differential input logic high	+ 0.200	-	V	1
VILdiff	Differential input logic low		- 0.200	V	1

Note1:

Refer to “Overshoot and Undershoot Specification section 6.5 on 26 page

5.2.3 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK# and DQS, DQS#) must meet the requirements in Table The differential input cross point voltage VIX is measured from the actual cross point of true and complement signal to the midlevel between of VDD and VSS.



< Figure 5.2.3: Vix Definition >

Symbol	Parameter	DDR3-800, DDR3-1066		Unit	Notes
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2	- 150	+ 150	mV	

< Table 5.2.3: Cross point voltage for differential input signals (CK, DQS) >

5.3 Slew Rate Definitions

5.3.1 For Single Ended Input Signals

- Input Slew Rate for Input Setup Time (tIS) and Data Setup Time (tDS)

Setup (tIS and tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIH (AC) min. Setup (tIS and tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIL (AC) max.

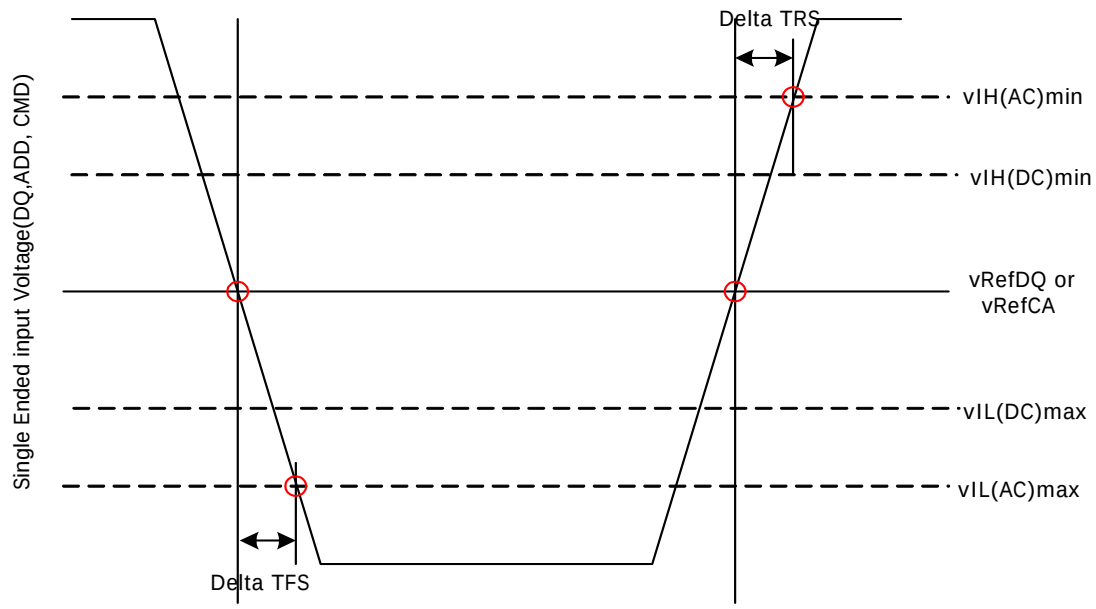
- Input Slew Rate for Input Hold Time (tIH) and Data Hold Time (tDH)

Hold nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL (DC) max and the first crossing of VRef. Hold (tIH and tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH (DC) min and the first crossing of VRef.

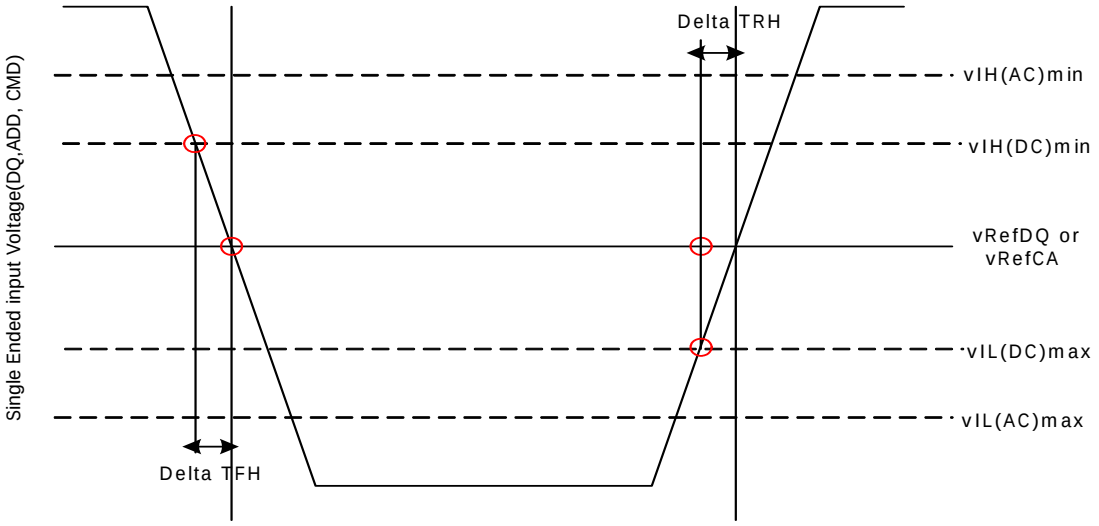
Description	Measured		Defined by	Applicable for
	Min	Max		
Input slew rate for rising edge	Vref	VIH (AC) min	$\frac{\text{VIH (AC) min-Vref}}{\text{Delta TRS}}$	Setup (tIS, tDS)
Input slew rate for falling edge	Vref	VIL (AC) max	$\frac{\text{Vref-VIL (AC) max}}{\text{Delta TFS}}$	
Input slew rate for rising edge	VIL (DC) max	Vref	$\frac{\text{Vref-VIL (DC) max}}{\text{Delta TFH}}$	Hold (tIH, tDH)
Input slew rate for falling edge	VIH (DC) min	Vref	$\frac{\text{VIH (DC) min-Vref}}{\text{Delta TRH}}$	

< Table 5.3.1: Single-Ended Input Slew Rate Definition >

Part A: Set up



Part B: Hold



< Figure 5.3.1: Input Nominal Slew Rate Definition for Single-Ended Signals >

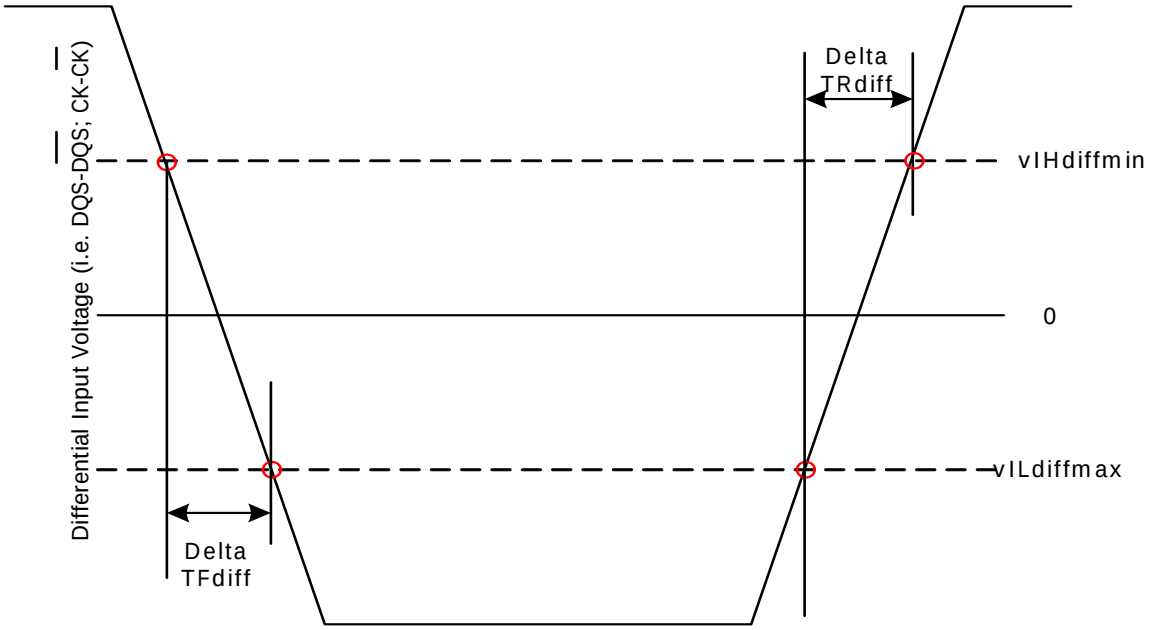
5.3.2 Differential Input Signals

Input slew rate for differential signals (CK, CK# and DQS, DQS#) are defined and measured as shown in below Table and Figure .

Description	Measured		Defined by
	Min	Max	
Differential input slew rate for rising edge (CK-CK and DQS-DQS)	VILdiffmax	VIHdiffmin	$\frac{\text{VIHdiffmin-VILdiffmax}}{\text{DeltaTRdiff}}$
Differential input slew rate for falling edge (CK-CK and DQS-DQS)	VIHdiffmin	VILdiffmax	$\frac{\text{VIHdiffmin-VILdiffmax}}{\text{DeltaTFdiff}}$

Note:

The differential signal (i.e. CK-CK and DQS-DQS) must be linear between these thresholds.



< Figure 5.3.2: Differential Input Slew Rate Definition for DQS,DQS# and CK,CK# >

5.4 DC & AC Output Buffer Levels

5.4.1 Single Ended DC & AC Output Levels

Below table shows the output levels used for measurements of single ended signals.

Symbol	Parameter	DDR3-800, 1066	Unit	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.2 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT + 0.1 x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	VTT - 0.1 x VDDQ	V	1

1. The swing of ± 0.1 x VDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT = VDDQ / 2.

5.4.2 Differential DC & AC Output Levels

Below table shows the output levels used for measurements of differential signals.

Symbol	Parameter	DDR3-800, 1066	Unit	Notes
VOHdiff (AC)	AC differential output high measurement level (for output SR)	+ 0.2 x VDDQ	V	1
VOLdiff (AC)	AC differential output low measurement level (for output SR)	- 0.2 x VDDQ	V	1
1. The swing of °æ 0.2 x VDDQ is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40ßŸ and an effective test load of 25ßŸ to VTT = VDDQ/2 at each of the differential output				

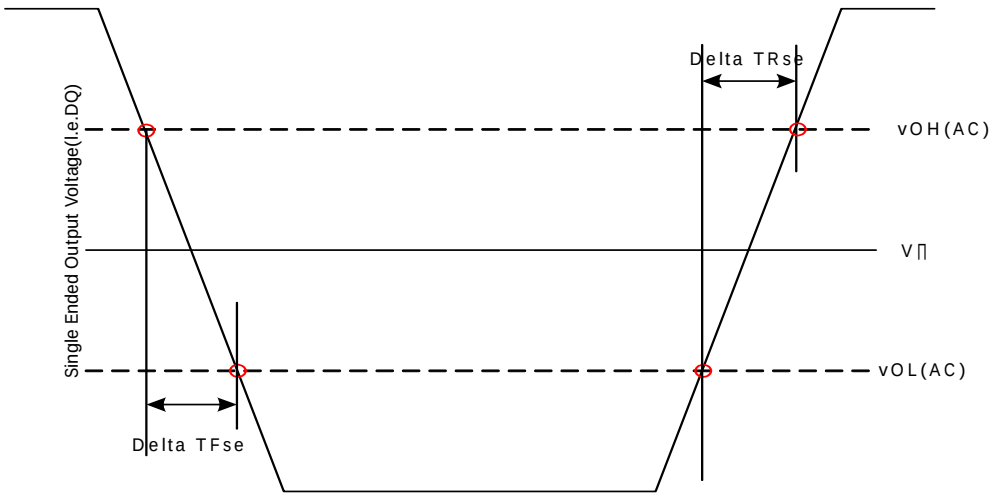
5.4.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in below Table and Figure 5.4.3.

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	$\frac{VOH(AC)-VOL(AC)}{\overline{DeltaTRse}}$
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	$\frac{VOH(AC)-VOL(AC)}{\overline{DeltaTFse}}$

Note:

Output slew rate is verified by design and characterisation, and may not be subject to production test.



< Figure 5.4.3: Single Ended Output Slew Rate Definition >

Parameter	Symbol	DDR3-800		DDR3-1066		Units
		Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5	V/ns

***** Description:**
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
For Ron = RZQ/7 setting

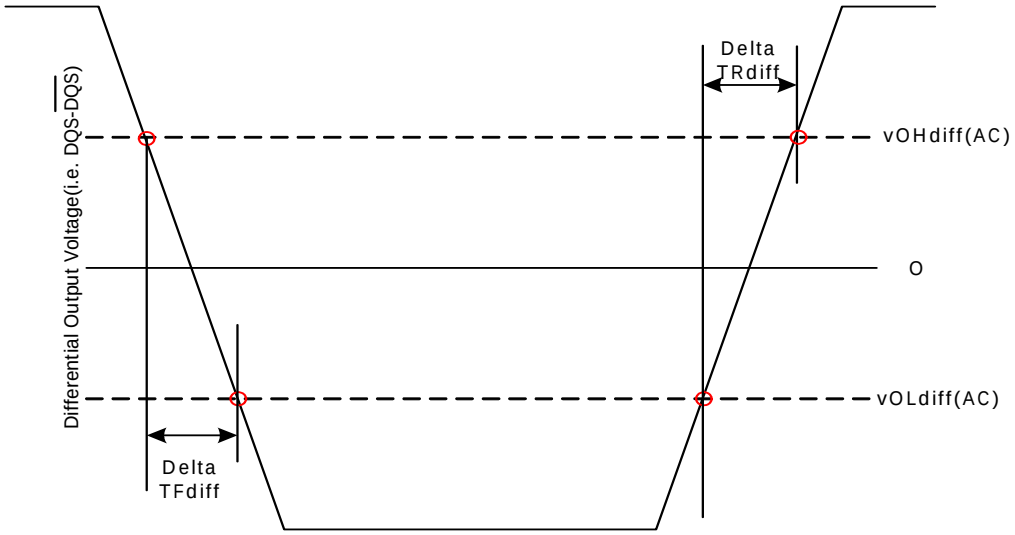
< Table 5.4.3: Output Slew Rate (single-ended) >

5.4.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff (AC) and VOHdiff (AC) for differential signals as shown in below Table and Figure 5.4.4

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff (AC)	VOHdiff (AC)	$\frac{\text{VOHdiff (AC)-VOLdiff (AC)}}{\overline{\text{DeltaTRdiff}}}$
Differential output slew rate for falling edge	VOHdiff (AC)	VOLdiff (AC)	$\frac{\text{VOHdiff (AC)-VOLdiff (AC)}}{\overline{\text{DeltaTFdiff}}}$

Note: Output slew rate is verified by design and characterization, and may not be subject to production test..



< Figure 5.4.4: Differential Output Slew Rate Definition >

Parameter	Symbol	DDR3-800		DDR3-1066		Units
		Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	5	10	5	10	V/ns

*****Description:**
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

< Table 5.4.4: Differential Output Slew Rate >

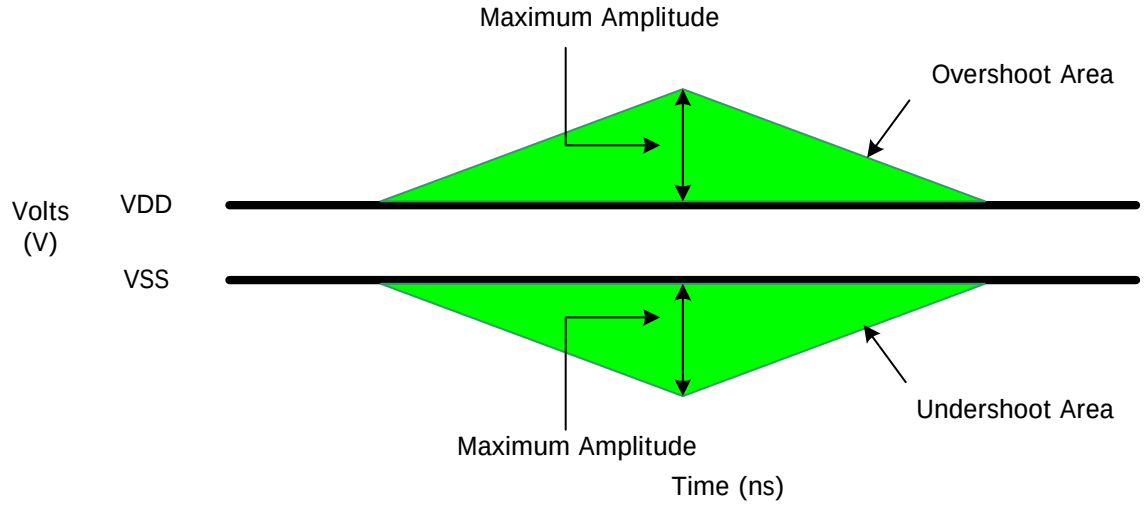
5.5 Overshoot and Undershoot Specifications

5.5.1 Address and Control Overshoot and Undershoot Specifications

Description	Specification	
	DDR3-800	DDR3-1066
Maximum peak amplitude allowed for overshoot area (see Figure)	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure)	0.4V	0.4V
Maximum overshoot area above VDD (See Figure)	0.67 V-ns	0.5 V-ns
Maximum undershoot area below VSS (See Figure)	0.67 V-ns	0.5 V-ns

< Table 5.5.1: AC Overshoot/Undershoot Specification for Address and Control Pins >

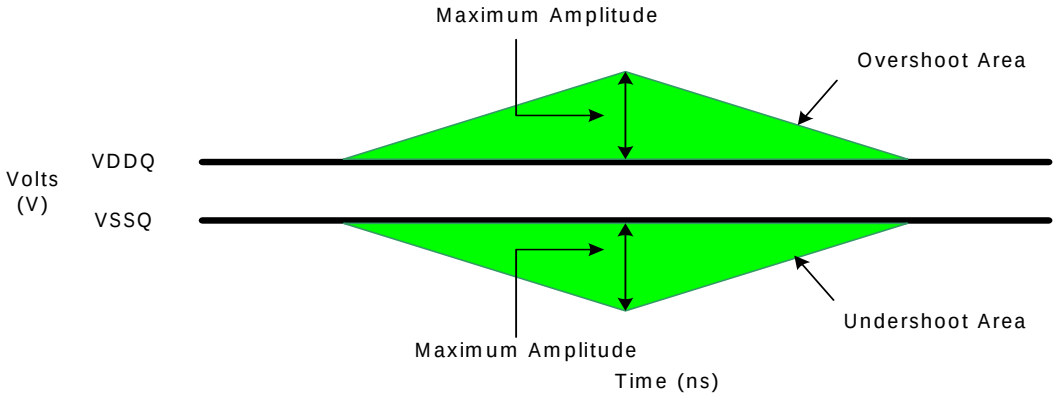
< Figure 5.5.1: Address and Control Overshoot and Undershoot Definition >



5.5.2 Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

Description	Specification	
	DDR3-800	DDR3-1066
Maximum peak amplitude allowed for overshoot area (see Figure)	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure)	0.4V	0.4V
Maximum overshoot area above VDDQ (See Figure)	0.25 V-ns	0.19 V-ns
Maximum undershoot area below VSSQ (See Figure)	0.25 V-ns	0.19 V-ns

< Table 5.5.2: AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask >



Clock, Data Strobe and Mask Overshoot and Undershoot Definition

< Figure 5.5.2: Clock, Data, Strobe and Mask Overshoot and Undershoot Definition >

5.6 Pin Capacitance

Parameter	Symbol	DDR3-800		DDR3-1066		Units	Notes
		Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, DQS#, TDQS, TDQS#)	C_{IO}	TBD	TBD	TBD	TBD	pF	1,2,3
Input capacitance, CK and CK#	C_{CK}	TBD	TBD	TBD	TBD	pF	2,3,5
Input capacitance delta CK and CK#	C_{DCK}	TBD	TBD	TBD	TBD	pF	2,3,4
Input capacitance (All other input-only pins)	C_{I}	TBD	TBD	TBD	TBD	pF	2,3,6
Input capacitance delta, DQS and DQS#	C_{DDQS}	TBD	TBD	TBD	TBD	pF	2,3,12
Input capacitance delta (All CTRL input-only pins)	C_{DI_CTRL}	TBD	TBD	TBD	TBD	pF	2,3,7,8
Input capacitance delta (All ADD/CMD input-only pins)	$C_{DI\_ADD\_CMD}$	TBD	TBD	TBD	TBD	pF	2,3,9, 10
Input/output capacitance delta (DQ, DM, DQS, DQS#)	C_{DIO}	TBD	TBD	TBD	TBD	pF	2,3,11

Notes:

1. TDQS/TDQS# are not necessarily input function but since TDQS is sharing DM pin and the parasitic characterization of TDQS/TDQS# should be close as much as possible, Cio & Cdio requirement is applied (recommend deleting note or changing to “Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS.”)
2. This parameter is not subject to production test. It is verified by design and characterization. Input capacitance is measured according to JEP147(“PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)”) with VDD, VDDQ, VSS,VSSQ applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of C_{CK}-C_{CK}#.
5. The minimum C_{CK} will be equal to the minimum C_{I}.
6. Input only pins include: ODT, CS, CKE, A0-A15, BA0-BA2, RAS#, CAS#, WE#.
7. CTRL pins defined as ODT, CS and CKE.
8. C_{DI_CTRL}=C_{I}(CNTL) - 0.5 * C_{I}(CLK) + C_{I}(CLK#))
9. ADD pins defined as A0-A15, BA0-BA2 and CMD pins are defined as RAS#, CAS# and WE#.
10. $C_{DI\_ADD\_CMD}$=C_{I}(ADD_CMD) - 0.5*(C_{I}(CLK)+C_{I}(CLK#))
11. C_{DIO}=C_{IO}(DQ) - 0.5*(C_{IO}(DQS)+C_{IO}(DQS#))
12. Absolute value of C_{IO}(DQS) - C_{IO}(DQS#)

5.7 IDD Specifications (T_{CASE}: 0 to 95°C)

4GB, 512M x 64 SO-DIMM: HMT451S6MMP8C

Symbol	DDR3 800	DDR3 1066	Unit	note
I_{DD0}	1152	1376	mA	x8
I_{DD1}	1320	1536	mA	x8
I_{DD2N}	848	1072	mA	x8
I_{DD2NT}	864	1104	mA	x8
I_{DD2QNT}	1232	1264	mA	x8
I_{DD2P0}	208	208	mA	x8
I_{DD2P1}	400	528	mA	x8
I_{DD2Q}	832	1056	mA	x8
I_{DD3N}	912	1152	mA	x8
I_{DD3P}	512	672	mA	x8
I_{DD4R}	1680	2096	mA	x8
I_{DDQ4R}	920	1048	mA	x8
I_{DD4W}	1456	1856	mA	x8
I_{DD5B}	2488	2704	mA	x8
I_{DD6}	192	192	mA	x8
I_{DD6ET}	192	192	mA	x8
I_{DD6TC}	192	192	mA	x8
I_{DD7}	2560	2888	mA	x8

5.7 IDD Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 1. shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- ”0” and “LOW” is defined as VIN <= $V_{ILAC(max)}$.
- ”1” and “HIGH” is defined as VIN >= $V_{IHAC(max)}$.
- “FLOATING” is defined as inputs are VREF - VDD/2.
- Timing used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 1 on Page 26.
- Basic IDD and IDDQ Measurement Conditions are described in Table 2 on page 26.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 3 on page 30 through Table 10 on page 36.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  Qoff = 0_B (Output Buffer enabled in MR1);
  RTT_Nom = RZQ/6 (40 Ohm in MR1);
  RTT_Wr = RZQ/2 (120 Ohm in MR2);
  TDQS Feature disabled in MR1
- Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, LOW, LOW, LOW}
- Define $\overline{D}$ = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, HIGH, HIGH, HIGH}

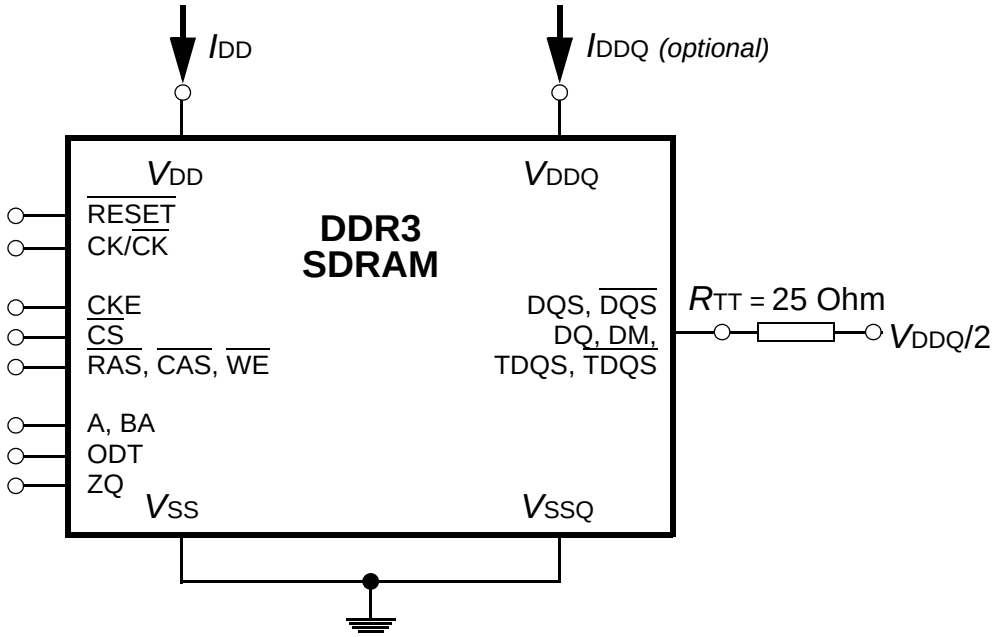


Figure 1 - Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements [Note: DIMM level Output test load condition may be different from above]

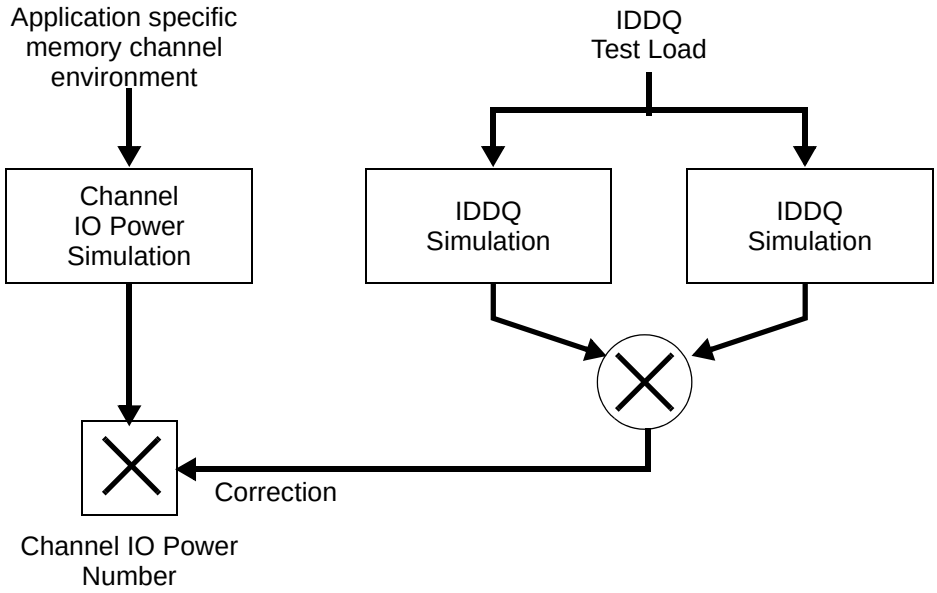


Figure 2 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

Table 1 -Timings used for IDD and IDDQ Measurement-Loop Patterns

Symbol		DDR3-800	DDR3-1066	Unit
		5-5-5	7-7-7	
t_{CK}		2.5	1.875	ns
CL		5	7	nCK
n_{RCD}		5	7	nCK
n_{RC}		20	27	nCK
n_{RAS}		15	20	nCK
n_{RP}		5	7	nCK
n_{FAW}	x4/x8	16	20	nCK
	x16	20	27	nCK
n_{RRD}	x4/x8	4	4	nCK
	x16	4	6	nCK
n_{RFC} -512Mb		36	48	nCK
n_{RFC}-1 Gb		44	59	nCK
n_{RFC}- 2 Gb		64	86	nCK
n_{RFC}- 4 Gb		120	160	nCK
n_{RFC}- 8 Gb		140	187	nCK

Table 2 -Basic IDD and IDDQ Measurement Conditions

Symbol	Description
I_{DD0}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 1 on page 26; BL: 8[a)]; AL: 0; $\overline{CS}$: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 3 on page 30; Data IO: FLOATING; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3 on page 30); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 3 on page 30
I_{DD1}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 1 on page 26; BL: 8[a)]; AL: 0; $\overline{CS}$: High between ACT, RD and PRE; Command, Address; Bank Address Inputs, Data IO: partially toggling according to Table 4 on page 31; DM: stable at 0; Bank Activity: Cycling with on bank active at a time: 0,0,1,1,2,2,... (see Table 4 on page 31); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 4 page 31

I_{DD2N}	Precharge Standby Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5 on page 32; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 5 on page 32
I_{DD2NT}	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 6 on page 32; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: toggling according to Table 6 on page 32; Pattern Details: see Table 6 on page 32
I_{DDQ2NT} (optional)	Precharge Standby ODT IDDQ Current Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
I_{DD2P0}	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit[c]
I_{DD2P1}	Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit[c]
I_{DD2Q}	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0
I_{DDQ4R} (optional)	Operating Burst Read IDDQ Current Same definition like for IDD4R, however measuring IDDQ current instead of IDD current

I_{DD3N}	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5 on page 32; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 5 on page 32
I_{DD3P}	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0
I_{DD4R}	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: High between RD; Command, Address, Bank Address Inputs: partially toggling according to Table 7 on page 33; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7 on page 33; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...(see Table 7 on page 33); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 7 on page 33
I_{DD4W}	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: High between WR; Command, Address, Bank Address Inputs: partially toggling according to Table 8 on page 34; Data IO: seamless read data burst with different data between one burst and the next one according to Table 8 on page 34; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...(see Table 8 on page 34); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at HIGH; Pattern Details: see Table 8 on page 34
I_{DD5B}	Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$: High between REF; Command, Address, Bank Address Inputs: partially toggling according to Table 9 on page 35; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nREF (see Table 9 on page 35); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 9 on page 35

I_{DD6}	Self-Refresh Current: Normal Temperature Range T_{CASE}: 0 - 85 °C; Auto Self-Refresh (ASR): Disabled[d];Self-Refresh Temperature Range (SRT): Normal[e]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: FLOATING
I_{DD6ET}	Self-Refresh Current: Extended Temperature Range (optional)[f] T_{CASE}: 0 - 95 °C; Auto Self-Refresh (ASR): Disabled[d];Self-Refresh Temperature Range (SRT): Extended[e]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: FLOATING; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: FLOATING
I_{DD6TC}	Auto Self-Refresh Current (optional)[f] T_{CASE}: 0 - 95 °C; Auto Self-Refresh (ASR): Enabled[d];Self-Refresh Temperature Range (SRT): Normal[e]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1 on page 26; BL: 8[a]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: FLOATING; DM: stable at 0; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: FLOATING
I_{DD7}	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, NRRD, nFAW, CL: see Table 1 on page 26; BL: 8[a]; AL: CL-1; $\overline{CS}$: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to Table 10 on page 36; Data IO: read data burst with different data between one burst and the next one according to Table 10 on page 36; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different addressing, wee Table 10 on page 36; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 10 on page 36

a) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
b) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B
c) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12 = 1B for Fast Exit
d) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
e) Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range
f) Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM device

Table 3 - IDD0 Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	00	00	0	0	F	0	-
			...	repeat pattern 1...4 until 1*nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 2*nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are FLOATING.
b) DQ signals are FLOATING.

Table 4 - IDD1 Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRCD - 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until nRC + nRCE - 1, truncate if necessary												
			1*nRC+nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			...	repeat pattern nRC + 1,...4 until nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until *2 nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise FLOATING.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are FLOATING.

Table 5 - IDD2N and IDD3N Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	8-11	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	12-15	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	16-19	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	20-23	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	24-17	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	28-31	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are FLOATING.
b) DQ signals are FLOATING.

Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	00000000
		1	4-7	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1												
		2	8-11	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2												
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3												
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4												
		5	20-23	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5												
		6	24-17	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are FLOATING.
b) DQ signals are FLOATING.

Table 7 - IDD4R and IDDQ24RMeasurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise FLOATING.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are FLOATING.

Table 8 - IDD4W Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to WR Commands, otherwise FLOATING.
b) Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are FLOATING.

Table 9 - IDD5B Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	-
		1	1.2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			5...8	repeat cycles 1...4, but BA[2:0] = 1												
			9...12	repeat cycles 1...4, but BA[2:0] = 2												
			13...16	repeat cycles 1...4, but BA[2:0] = 3												
			17...20	repeat cycles 1...4, but BA[2:0] = 4												
			21...24	repeat cycles 1...4, but BA[2:0] = 5												
			25...28	repeat cycles 1...4, but BA[2:0] = 6												
			29...32	repeat cycles 1...4, but BA[2:0] = 7												
		2	33...nRFC-1	repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary.												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are FLOATING.
b) DQ signals are FLOATING.

Table 10 - IDD7 Measurement-Loop Pattern[a)]

ATTENTION! Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD+1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD+2	D	1	0	0	0	0	1	00	0	0	F	0	-
			...	repeat above D Command until 2* nRRD - 1												
		2	2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4*nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
			...	Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW+nRRD	repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW+2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW+3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 7												
		9	nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
			...	Assert and repeat above D Command until 2* nFAW - 1, if necessary												
		10	2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
			2&nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2* nFAW + nRRD - 1												
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2&nFAW+nRRD+2	D	1	0	0	0	0	1	00	0	0	0	0	-
				Repeat above D Command until 2* nFAW + 2* nRRD - 1												
		12	2*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 2												
		13	2*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 3												
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	0	00	0	0	0	0	-
				Assert and repeat above D Command until 3* nFAW - 1, if necessary												
		15	3*nFAW	repeat Sub-Loop 10, but BA[2:0] = 4												
		16	3*nFAW+nRRD	repeat Sub-Loop 11, but BA[2:0] = 5												
		17	3*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 6												
		18	3*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 7												
		14	3*nFAW+4*nRRD	D	1	0	0	0	0	0	00	0	0	0	0	-
				Assert and repeat above D Command until 4* nFAW - 1, if necessary												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise FLOATING.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are FLOATING.

6. Electrical Characteristics and AC Timing

6.1 Refresh Parameters by Device Density

Parameter	Symbol		512Mb	1Gb	2Gb	4Gb	8Gb	Units
REF command to ACT or REF command time	tRFC		90	110	160	300	350	ns
Average periodic refresh interval	tREFI	0 ×C < T_{CASE} < 85 ×C	7.8	7.8	7.8	7.8	7.8	us
		85 ×C < T_{CASE} < 95 ×C	3.9	3.9	3.9	3.9	3.9	us

6.2 DDR3 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin

DDR3 800 Speed Bin			DDR3-800E		Unit	Notes
CL - nRCD - nRP			6-6-6			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	15	—	ns	
PRE command period		t_{RP}	15	—	ns	
ACT to ACT or REF command period		t_{RC}	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	1)2)3)4)
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1)2)3)
Supported CL Settings			6		n_{CK}	
Supported CWL Settings			5		n_{CK}	

DDR3 1066 Speed Bin			DDR3-1066F		Unit	Note
CL - nRCD - nRP			7-7-7			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.125	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.125	—	ns	
PRE command period		t_{RP}	13.125	—	ns	
ACT to ACT or REF command period		t_{RC}	50.625	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	1)2)3)4)6)
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	4)
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1)2)3)6)
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1)2)3)4)
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1)2)3)4)
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1)2)3)
Supported CL Settings			6, 7, 8		n_{CK}	
Supported CWL Settings			5, 6		n_{CK}	

Speed Bin Table Notes

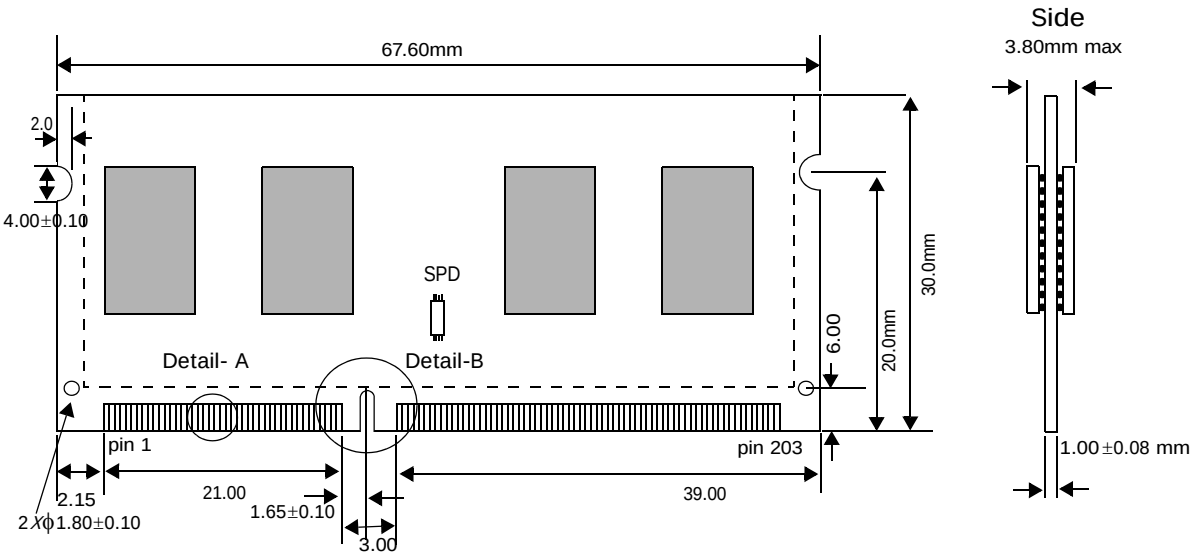
Absolute Specification (T_{OPER}; V_{DDQ} = V_{DD} = 1.5V +/- 0.075 V);

Notes:

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK (AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK (AVG) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK (AVG) [ns], rounding up to the next 'Supported CL'.
3. tCK(AVG).MAX limits: Calculate tCK (AVG) = tAA.MAX / CLSELECTED and round the resulting tCK (AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CLSELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

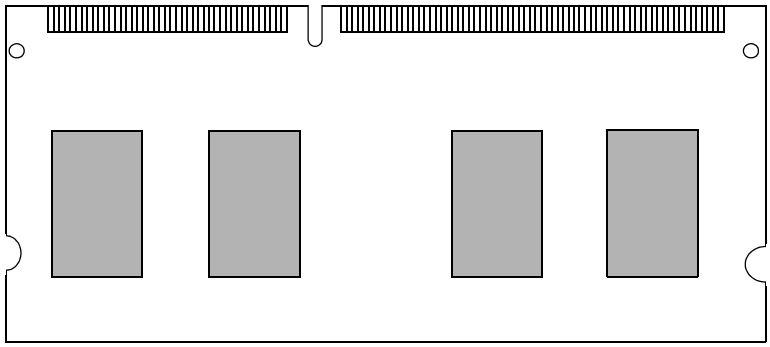
7. DIMM Outline Diagram

Front View

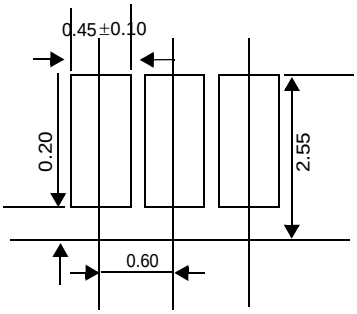


Side

Back View



Detail of Contacts A



Detail of Contacts B