Si5316

PRELIMINARY DATA SHEET

PRECISION CLOCK JITTER ATTENUATOR

Description

The Si5316 is a low jitter, precision jitter attenuator for high-speed communication systems, including OC-48, OC-192, 10G Ethernet, and 10G Fibre Channel. The Si5316 accepts dual clock inputs in the 19, 38, 77, 155, 311, or 622 MHz frequency range and generates a jitter-attenuated clock output at the same frequency. Within each of these clock ranges, the device can be tuned approximately 15% higher than nominal SONET/SDH frequencies, up to a maximum of 710 MHz in the 622 MHz range. The Si5316 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. The DSPLL loop bandwidth is digitally programmable, providing jitter performance optimization at the application level. Operating from a single 1.8, 2.5, or 3.3 V supply, the Si5316 is ideal for providing jitter attenuation in high performance timing applications.

Applications

- Optical modules
- SONET/SDH OC-48/OC-192 line cards
- 10GbE, 10GFC line cards
- ITU G.709 line cards
- Wireless basestations
- Test and measurement

Features

- Fixed frequency jitter attenuator with selectable clock ranges at 19, 38, 77, 155, 311, and 622 MHz (710 MHz max)
- Support for SONET, 10GbE, 10GFC, and corresponding FEC rates
- Ultra-low jitter clock output with jitter generation as low as 0.3 ps_{RMS} (50 kHz–80 MHz)
- Integrated loop filter with selectable loop bandwidth (100 Hz to 7.9 kHz)
- Meets OC-192 GR-253-CORE jitter specifications
- Dual clock inputs with integrated clock select mux
- One clock input can be 1x, 4x, or 32x the frequency of the second clock input
- Single clock output with selectable signal format: LVPECL, LVDS, CML, CMOS
- LOL, LOS alarm outputs
- Pin programmable settings
- On-chip voltage regulator for 1.8, 2.5, or 3.3 V ±10% operation
- Small size (6 x 6 mm 36-lead QFN)
- Pb-free, RoHS compliant

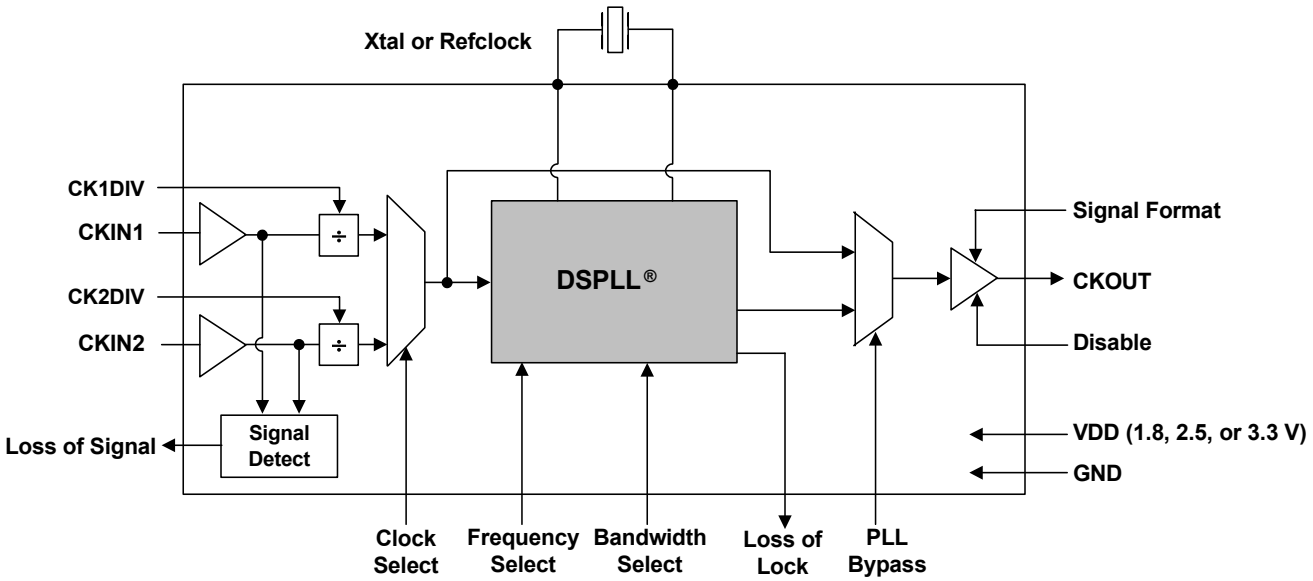


Table 1. Performance Specifications

(V_{DD} = 1.8, 2.5, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature Range	T_A		–40	25	85	ºC
Supply Voltage	V_{DD}		2.97	3.3	3.63	V
			2.25	2.5	2.75	V
			1.62	1.8	1.98	V
Supply Current	I_{DD}	f_{OUT} = 622.08 MHz LVPECL format output	—	217	243	mA
		f_{OUT} = 19.44 MHz CMOS format output	—	194	220	mA
		Tristate/Sleep Mode	—	TBD	TBD	mA
Input/Output Clock Frequency (CKIN1, CKIN2, CKOUT)	CK_F	FRQSEL[1:0] = LL FRQSEL[1:0] = LM FRQSEL[1:0] = LH FRQSEL[1:0] = ML FRQSEL[1:0] = MM FRQSEL[1:0] = MH	19.38 38.75 77.5 155.0 310.0 620.0	— — — — — —	22.28 44.56 89.13 178.25 356.5 710.0	MHz
Input Clocks (CKIN1, CKIN2)						
Differential Voltage Swing	CKN_{DPP}		0.25	—	1.9	V_{PP}
Common Mode Voltage	CKN_{VCM}	1.8V ±10%	0.9	—	1.4	V
		2.5V ±10%	1.0	—	1.7	V
		3.3V ±10%	1.1	—	1.95	V
Rise/Fall Time	CKN_{TRF}	20–80%	—	—	11	ns
Duty Cycle	CKN_{DC}	Whichever is less	40	—	60	%
			50	—	—	ns
Output Clock (CKOUT)						
Common Mode	V_{OCM}	LVPECL 100 Ω load line-to-line	V_{DD} – 1.42	—	V_{DD} – 1.25	V
Differential Output Swing	V_{OD}		1.1	—	1.9	V_{PP}
Single Ended Output Swing	V_{SE}		0.5	—	0.93	V
Rise/Fall Time	CKO_{TRF}	20–80%	—	230	350	ps
Duty Cycle	CKO_{DC}		45	—	55	%
PLL Performance						
Jitter Generation	J_{GEN}	f_{OUT} = 622.08 MHz, LVPECL output format 50 kHz–80 MHz	—	0.3	TBD	ps rms
		12 kHz–20 MHz	—	0.3	TBD	ps rms
Jitter Transfer	J_{PK}		—	0.05	0.1	dB

Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing.

Table 1. Performance Specifications (Continued)
(V_{DD} = 1.8, 2.5, or 3.3 V ±10%, T_A = –40 to 85 ºC)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Reference Jitter Transfer	J_{PKEXTN}		—	TBD	TBD	dB
Phase Noise	CKO_{PN}	f_{OUT} = 622.08 MHz 100 Hz offset	—	TBD	TBD	dBc/Hz
		1 kHz offset	—	TBD	TBD	dBc/Hz
		10 kHz offset	—	TBD	TBD	dBc/Hz
		100 kHz offset	—	TBD	TBD	dBc/Hz
		1 MHz offset	—	TBD	TBD	dBc/Hz
Subharmonic Noise	SP_{SUBH}	Phase Noise @ 100 kHz Offset	—	TBD	TBD	dBc
Spurious Noise	SP_{SPUR}	Max spur @ n x F3 (n ≥ 1, n x F3 < 100 MHz)	—	TBD	TBD	dBc
Package						
Thermal Resistance Junction to Ambient	θ_{JA}	Still Air	—	38	—	ºC/W

Note: For a more comprehensive listing of device specifications, please consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual. This document can be downloaded from www.silabs.com/timing.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	–0.5 to 3.6	V
LVCMOS Input Voltage	V_{DIG}	–0.3 to (V_{DD} + 0.3)	V
Operating Junction Temperature	T_{JCT}	–55 to 150	ºC
Storage Temperature Range	T_{STG}	–55 to 150	ºC
ESD HBM Tolerance (100 pF, 1.5 kΩ)		2	kV
ESD MM Tolerance		200	V
Latch-Up Tolerance		JESD78 Compliant	

Note: Permanent device damage may occur if the Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

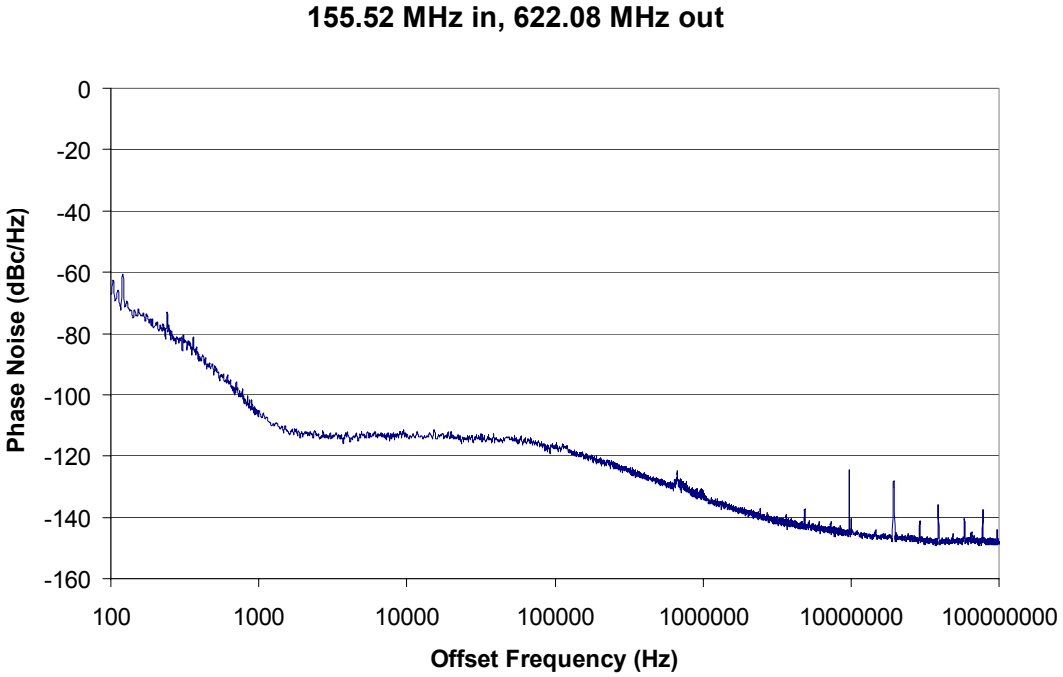
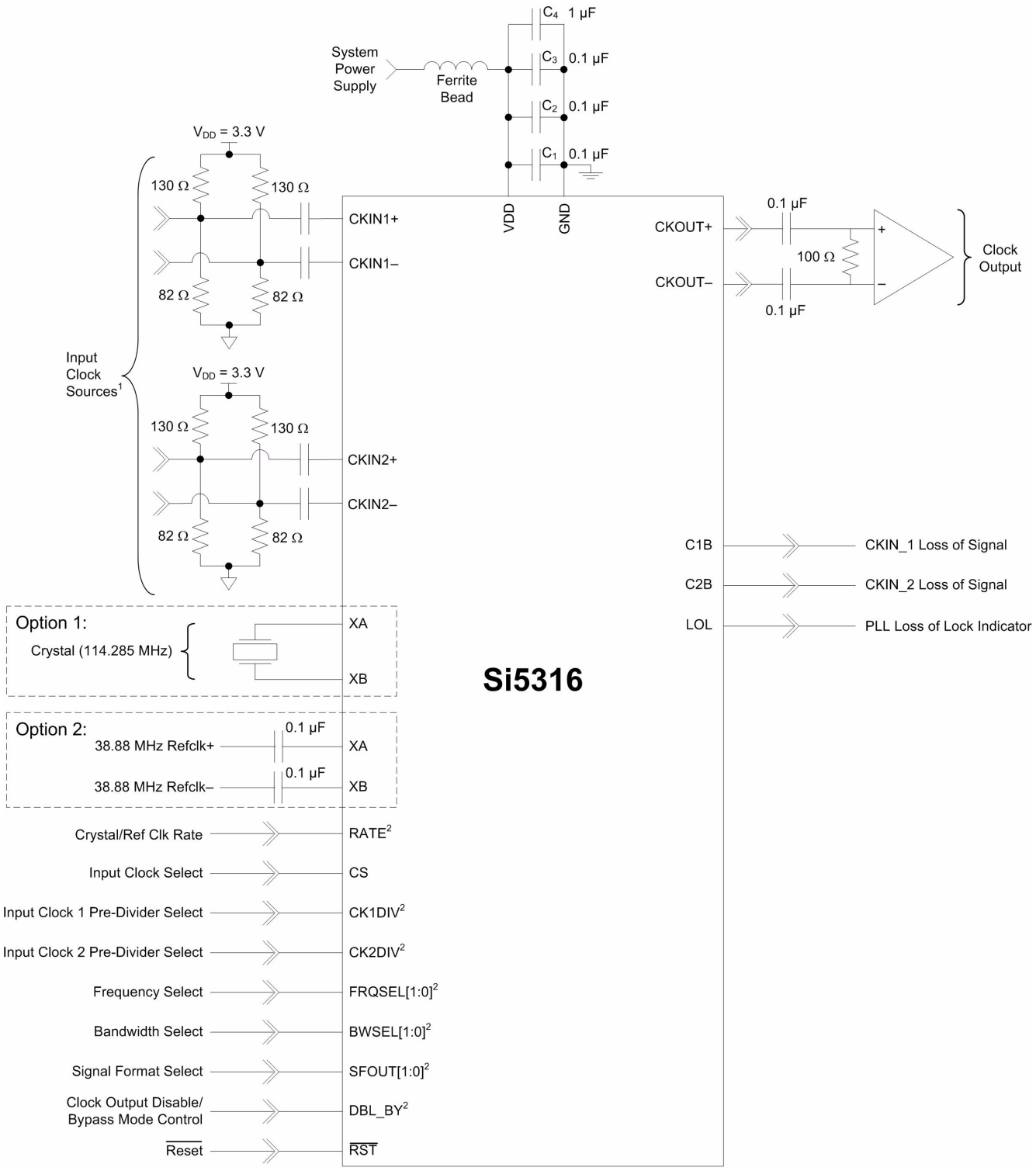


Figure 1. Typical Phase Noise Plot



Notes: 1. Assumes differential LVPECL termination (3.3 V) on clock inputs.

2. Denotes tri-level input pins with states designated as L (ground), M (V_{DD}/2), and H (V_{DD}).

Figure 2. Si5316 Typical Application Circuit

1. Functional Description

The Si5316 is a precision jitter attenuator for high-speed communication systems, including OC-48, OC-192, 10G Ethernet, and 10G Fibre Channel. The Si5316 accepts dual clock inputs in the 19, 38, 77, 155, 311, or 622 MHz frequency range and generates a jitter-attenuated clock output at the same frequency. Within each of these clock ranges, the device can be tuned approximately 15% higher than nominal SONET/SDH frequencies, up to a maximum of 710 MHz in the 622 MHz range. The Si5316 is based on Silicon Laboratories' 3rd-generation DSPLL® technology, which provides any-rate frequency synthesis and jitter attenuation in a highly integrated PLL solution that eliminates the need for external VCXO and loop filter components. For applications which require input clocks at different frequencies, the frequency of CKIN1 can be 1x, 4x, or 32x the frequency of CKIN2 as specified by the CK1DIV and CK2DIV inputs.

The Si5316 PLL loop bandwidth is selectable via the BWSEL[1:0] pins and supports a range from 100 Hz to 7.9 kHz. To calculate potential loop bandwidth values for a given input/output clock frequency, Silicon Laboratories offers a PC-based software utility, DSPLL*sim*, that calculates valid loop bandwidth settings automatically. This utility can be downloaded from www.silabs.com/timing.

The Si5316 supports manual active input clock selection. The Si5316 monitors both input clocks for loss-of-signal and provides a LOS alarm when it detects missing pulses on either input clock. Hitless switching is not supported by the Si5316. During a clock transition, the phase of the output clock will slew at a rate defined by the PLL loop bandwidth until the original input clock phase to output clock phase is restored. The device monitors the lock status of the PLL. The lock detect algorithm works by continuously monitoring the phase of the input clock in relation to the phase of the feedback clock.

The Si5316 has one differential clock output. The electrical format of the clock output is programmable to support LVPECL, LVDS, CML, or CMOS loads. For system-level debugging, a bypass mode is available which drives the output clock directly from the input clock, bypassing the internal DSPLL. The device is powered by a single 1.8, 2.5, or 3.3 V supply.

1.1. External Reference

An external, 38.88 MHz clock or a low-cost 114.285 MHz 3rd overtone crystal is used as part of a fixed-frequency oscillator within the DSPLL. This external reference is required for the device to perform jitter attenuation. Silicon Laboratories recommends using a high-quality crystal from TXC (www.txc.com.tw), part number 7MA1400014. An external 38.88 MHz clock from a high quality OCXO or TCXO can also be used as a reference for the device.

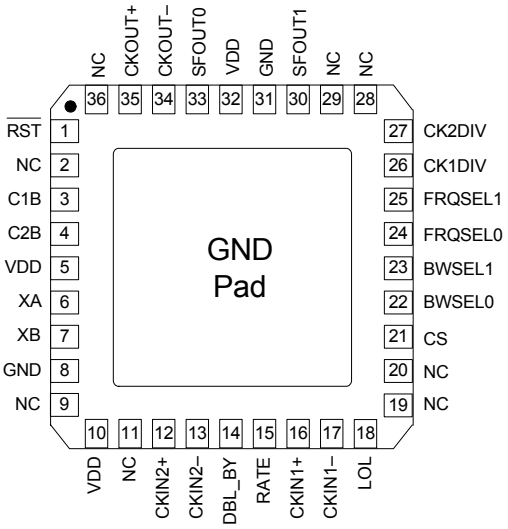
In digital hold, the DSPLL remains locked to this external reference. Any changes in the frequency of this reference when the DSPLL is in digital hold will be tracked by the output of the device. Note that crystals can have temperature sensitivities.

1.2. Further Documentation

Consult the Silicon Laboratories Any-Rate Precision Clock Family Reference Manual (FRM) for more detailed information about the Si5316. The FRM can be downloaded from www.silabs.com/timing.

Silicon Laboratories has developed a PC-based software utility called DSPLL*sim* to simplify device configuration, including frequency planning and loop bandwidth selection. This utility can be downloaded from www.silabs.com/timing.

2. Pin Descriptions: Si5316



Pin assignments are preliminary and subject to change.

Table 3. Si5316 Pin Descriptions

Pin #	Pin Name	I/O	Signal Level	Description
1	$\overline{\text{RST}}$	I	LVCMOS	**External Reset.** Active low input that performs external hardware reset of device. Resets all internal logic to a known state. Clock outputs are tristated during reset. After rising edge of $\overline{\text{RST}}$ signal, the Si5316 will perform an internal self-calibration. This pin has a weak pull-up.
2, 9, 11, 19, 20, 28, 29, 36	NC	—	—	**No Connect.** These pins must be left unconnected for normal operation.
3	C1B	O	LVCMOS	**CKIN1 Loss of Signal.** Active high Loss-of-signal indicator for CKIN1. Once triggered, the alarm will remain active until CKIN1 is validated. 0 = CKIN1 present 1 = LOS on CKIN1
4	C2B	O	LVCMOS	**CKIN2 Loss of Signal.** Active high Loss-of-signal indicator for CKIN2. Once triggered, the alarm will remain active until CKIN2 is validated. 0 = CKIN2 present 1 = LOS on CKIN2
5, 10, 32	V_{DD}	V_{DD}	Supply	**Supply.** The device operates from a 1.8, 2.5, or 3.3 V supply. Bypass capacitors should be associated with the following V_{DD} pins: 5 0.1 µF 10 0.1 µF 32 0.1 µF A 1.0 µF should be placed as close to device as is practical.

Table 3. Si5316 Pin Descriptions (Continued)

Pin #	Pin Name	I/O	Signal Level	Description
7 6	XB XA	I	Analog	**External Crystal or Reference Clock.** External crystal should be connected to these pins to use internal oscillator based reference. If external reference is used, apply reference clock to XA input and leave XB pin floating. External reference must be from a high-quality clock source (TCXO, OCXO). Frequency of crystal or external clock is set by the RATE pin.
8, 31	GND	GND	Supply	**Ground.** Must be connected to system ground. Minimize the ground path impedance for optimal performance of this device.
15	RATE	I	3-Level	**External Crystal or Reference Clock Rate.** Three level input that selects the type and rate of external crystal or reference clock to be applied to the XA/XB port. L = 38.88 MHz external clock M = 114.285 MHz 3rd OT crystal H = Reserved
12 13	CKIN2+ CKIN2–	I	Multi	**Clock Input 2.** Differential input clock. This input can also be driven with a single-ended signal.
14	DBL_BY	I	3-Level	**Output Disable/Bypass Mode Control.** Controls enable of CKOUT divider/output buffer path and PLL bypass mode. L = CKOUT enabled M = CKOUT disabled H = Bypass mode with CKOUT enabled
16 17	CKIN1+ CKIN1–	I	Multi	**Clock Input 1.** Differential input clock. This input can also be driven with a single-ended signal.
18	LOL	O	LVCMOS	**PLL Loss of Lock Indicator.** This pin functions as the active high PLL loss of lock indicator. 0 = PLL locked 1 = PLL unlocked
21	CS	I	LVCMOS	**Input Clock Select.** This pin functions as the input clock selector. This input is internally deglitched to prevent inadvertent clock switching during changes in the CKSEL input state. 0 = Select CKIN1 1 = Select CKIN2
23 22	BWSEL1 BWSEL0	I	3-Level	**Bandwidth Select.** Three level inputs that select the DSPLL closed loop bandwidth. Detailed operations and timing characteristics for these pins may be found in the Any-Rate Precision Clock Family Reference Manual.
25 24	FRQSEL1 FRQSEL0	I	3-Level	**Frequency Select.** Sets the output frequency of the device. When the frequency of CKIN1 is not equal to CKIN2, the lower frequency input clock must be equal to the output clock frequency.

Table 3. Si5316 Pin Descriptions (Continued)

<table>
<tr><th>Pin #</th><th>Pin Name</th><th>I/O</th><th>Signal Level</th><th>Description</th></tr>
<tr><td>26</td><td>CK1DIV</td><td>I</td><td>3-Level</td><td>Input Clock 1 Pre-Divider Select.
Pre-divider on CKIN1. Used with CK2DIV to divide input clock frequencies to a common value. When the frequencies applied to CKIN1 and CKIN2 are equal, CK1DIV must be tied low.
L = CKIN1 input divider set to 1.
M = CKIN1 input divider set to 4.
H = CKIN1 input divider set to 32.</td></tr>
<tr><td>27</td><td>CK2DIV</td><td>I</td><td>3-Level</td><td>Input Clock 2 Pre-Divider Select.
Pre-divider on CKIN2. Used with CK1DIV to divide input clock frequencies to a common value. When the frequencies applied to CKIN1 and CKIN2 are equal, CK2DIV must be tied low.
L = CKIN2 input divider set to 1.
M = CKIN2 input divider set to 4.
H = CKIN2 input divider set to 32.</td></tr>
<tr><td>33
30</td><td>SFOUT0
SFOUT1</td><td>I</td><td>3-Level</td><td>Signal Format Select.
Three level inputs that select the output signal format (common mode voltage and differential swing) for CKOUT. Valid settings include LVPECL, LVDS, and CML. Also includes selections for CMOS mode, tristate mode, and tristate/sleep mode.
<table>
<tr><th>SFOUT[1:0]</th><th>Signal Format</th></tr>
<tr><td>HH</td><td>Reserved</td></tr>
<tr><td>HM</td><td>Reserved</td></tr>
<tr><td>HL</td><td>CML</td></tr>
<tr><td>MH</td><td>LVPECL</td></tr>
<tr><td>MM</td><td>Reserved</td></tr>
<tr><td>ML</td><td>LVDS</td></tr>
<tr><td>LH</td><td>CMOS</td></tr>
<tr><td>LM</td><td>Tristate/Sleep</td></tr>
<tr><td>LL</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>34
35</td><td>CKOUT–
CKOUT+</td><td>O</td><td>Multi</td><td>Clock Output.
Differential output clock with a frequency selected from a table of values. Output signal format is selected by SFOUT pins. Output is differential for LVPECL, LVDS, and CML compatible modes. For CMOS format, both output pins drive identical single-ended clock outputs.</td></tr>
<tr><td>GND PAD</td><td>GND</td><td>GND</td><td>Supply</td><td>Ground Pad.
The ground pad must provide a low thermal and electrical impedance to a ground plane.</td></tr>
</table>

3. Ordering Guide

Ordering Part Number	Package	Temperature Range
Si5316-B-GM	36-Lead 6 x 6 mm QFN	–40 to 85 °C

4. Package Outline: 36-Lead QFN

Figure 3 illustrates the package details for the Si5316. Table 4 lists the values for the dimensions shown in the illustration.

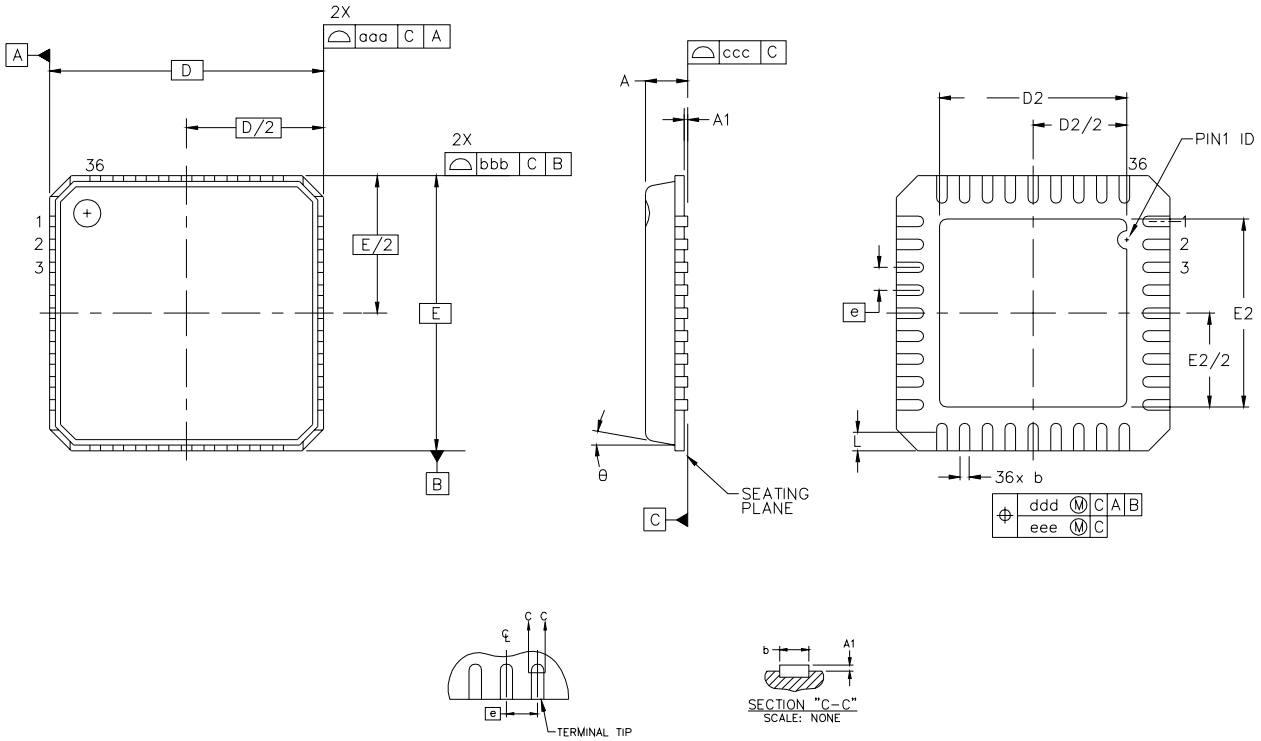


Figure 3. 36-Pin Quad Flat No-lead (QFN)

Table 4. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.01	0.05
b	0.18	0.23	0.30
D		6.00 BSC	
D2	3.95	4.10	4.25
e		0.50 BSC	
E		6.00 BSC	
E2	3.95	4.10	4.25

Symbol	Millimeters		
	Min	Nom	Max
L	0.50	0.60	0.75
θ	—	—	12º
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.05
ddd	—	—	0.10
eee	—	—	0.05

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VJJD.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

5. Recommended PCB Layout

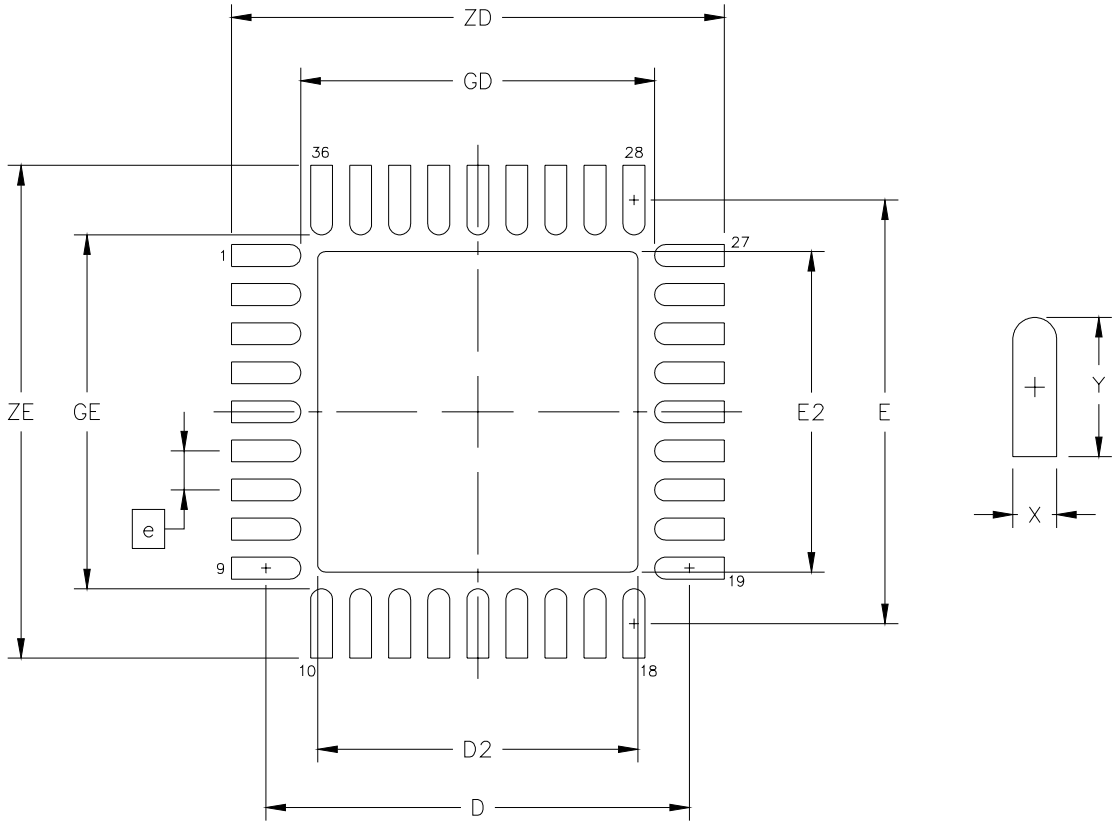


Figure 4. PCB Land Pattern Diagram

Table 5. PCB Land Pattern Dimensions

Dimension	MIN	MAX
e	0.50 BSC.	
E	5.42 REF.	
D	5.42 REF.	
E2	4.00	4.20
D2	4.00	4.20
GE	4.53	—
GD	4.53	—
X	—	0.28
Y	0.89 REF.	
ZE	—	6.31
ZD	—	6.31

Notes (General):

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Notes (Solder Mask Design):

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Notes (Stencil Design):

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
4. A 4 x 4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Notes (Card Assembly):

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

DOCUMENT CHANGE LIST

Revision 0.23 to 0.24

- Changed LVTTL to LVCMOS in Table 2, “Absolute Maximum Ratings,” on page 3.
- Added Figure 1, “Typical Phase Noise Plot,” on page 4.
- Showed preferred interface for an external reference clock in Figure 2, “Si5316 Typical Application Circuit,” on page 5.
- Updated 3. "Ordering Guide" on page 10.
- Added “5. Recommended PCB Layout”.

NOTES:

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