v00.0609

HMC791LC4B

DIVIDE-BY-2, DIVIDE-BY-4
0.1 - 28 GHz

Typical Applications

The HMC791LC4B is ideal for:

- Frequency Division up to 28 GHz
- Short, Intermediate, Long Haul Fiber Optic Applications
- 100 GbE Applications
- Serial Data Transmission Systems up to 28 GHz
- Broadband Test and Measurement Applications

Features

Supports Clock Frequencies up to 28 GHz

Simultaneous Divide-by-2 and Divide-by-4 Outputs

Differential and Single-Ended Operation [1]

Fast Rise and Fall Times (12 / 14 ps)

Low Power Consumption: 660mW

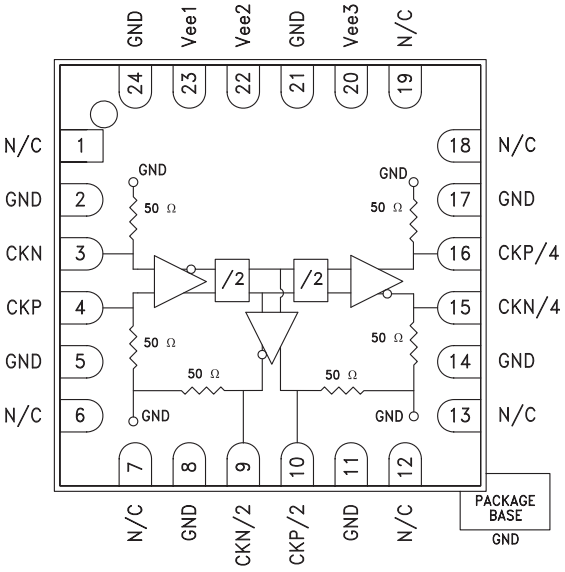
Single Negative Power Supply (-3.3V)

Output Signal Swing: 600mV p-p Differential

Ultra Low SSB Phase Noise: -151 dBc/Hz

24 Lead 4x4mm SMT Package: $16mm^2$

Functional Diagram



General Description

The HMC791LC4B is a low-noise divide-by-2, divide-by-4 designed to support input clock frequencies as high as 28 GHz. When an input clock signal is applied, divide-by-2 and divide-by-4 outputs are observed simultaneously. All input signals to the HMC791-LC4B are terminated with 50Ω to ground on-chip, and may be either AC or DC coupled. Outputs can be connected directly to a 50Ω terminated system, while DC blocking capacitors must be used if the terminating system is 50Ω to a non-zero voltage. The HMC791LC4B operates from a single -3.3V DC supply and is available in a ceramic RoHS compliant SMT package.

Electrical Specifications, T_A = +25° C, Vee = Vee1 = Vee2 = Vee3 = -3.3V

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supply Voltage	±10% Tolerance	-3.0	-3.3	-3.6	V
Total Supply Current			200		mA
Input Frequency		0.1		28	GHz
Input Amplitude Range (Single-Ended) [2]	1.0 - 6 GHz	-10		+6	dBm
	6 - 12 GHz	-20		+6	dBm
	12 - 16 GHz	-20		+3	dBm
	16 - 28 GHz	-20		+5	dBm
Input Return Loss	<20 GHz		9		dB
Input High Voltage	GND Referenced	-0.5		0.5	V
Input Low Voltage	GND Referenced	-1		0	V

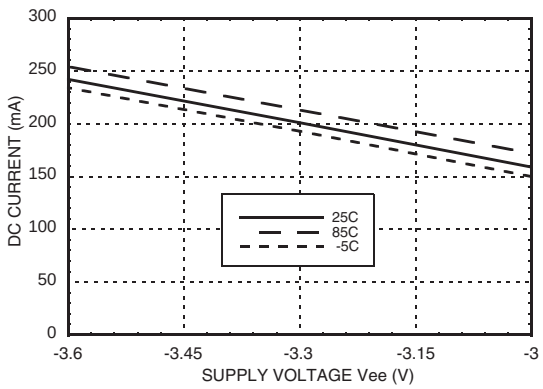
[1] See recommended single ended and differential configurations
[2] See recommended single ended configuration.

Electrical Specifications, T_A = +25° C, Vee = Vee1 = Vee2 = Vee3 = -3.3V

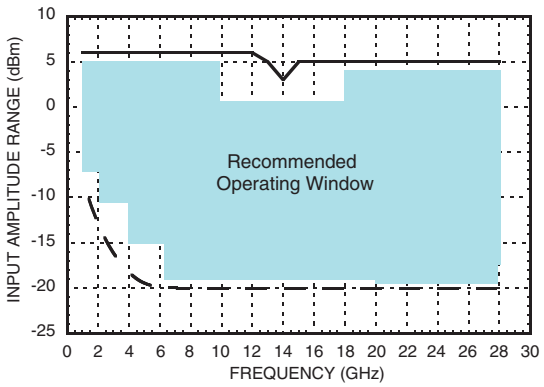
Parameter	Conditions	Min.	Typ.	Max.	Units
CK/2 Output Amplitude	Differential p-p		600		mV
CK/4 Output Amplitude	Differential p-p		600		mV
CK/2 Output Return Loss	<14 GHz		10		dB
CK/4 Output Return Loss	<7 GHz		15		dB
CK/2 Output High Voltage	GND Referenced		-10		mV
CK/2 Output Low Voltage	GND Referenced		-340		mV
CK/4 Output High Voltage	GND Referenced		-9		mV
CK/4 Output Low Voltage	GND Referenced		-350		mV
Additive Random Jitter [1]	@ 28 GHz, CK/2 Output, RMS		200		fs
	@ 28 GHz, CK/4 Output, RMS		280		fs
CK/2 Output Rise/Fall Time	@ 28 GHz Input, 20% - 80%		12 / 14		ps
CK/4 Output Rise/Fall Time	@ 28 GHz Input, 20% - 80%		17 / 16		ps
CK/2 SSB Phase Noise	10 GHz input @ 100 kHz Offset		-151		dBc/Hz
CK/4 SSB Phase Noise	10 GHz input @ 100 kHz Offset		-150		dBc/Hz

[1] Cable and eval board contribution is de-embedded. $RJ_{added} = \sqrt{[(RJ_{tested})^2 - (RJ_{thru})^2]}$

DC Current vs. Vee Over Temperature

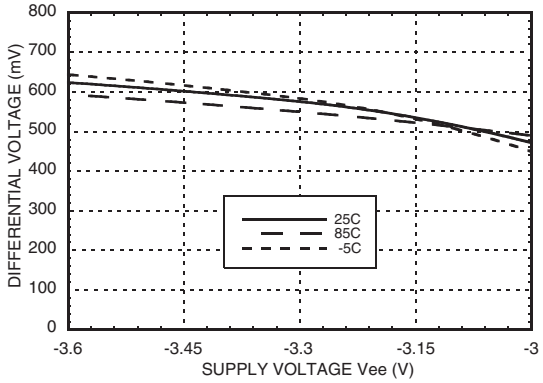


Recommended Operating Window [2]

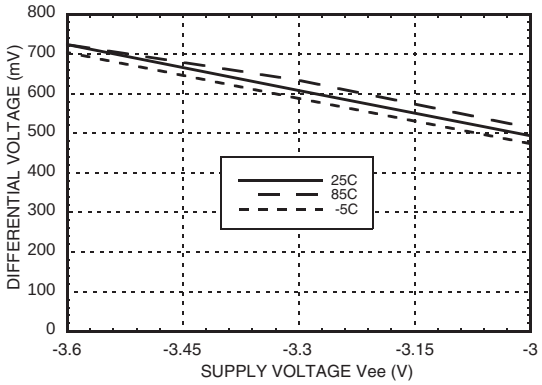


[2] See recommended single ended configuration.

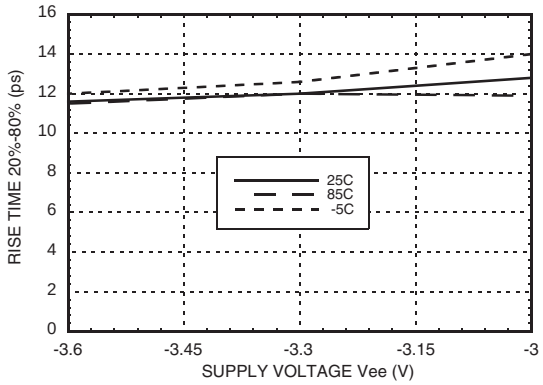
Differential Output Voltage vs. Vee Over Temperature, Divide-by-2



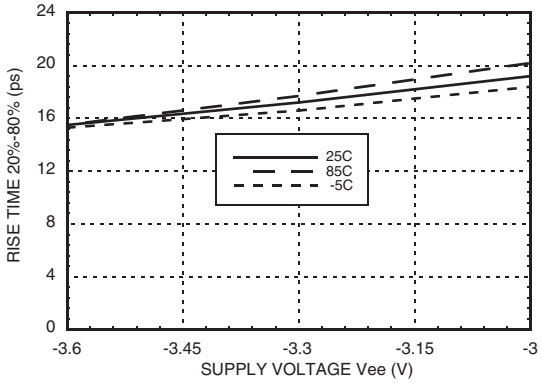
Differential Output Voltage vs. Vee Over Temperature, Divide-by-4



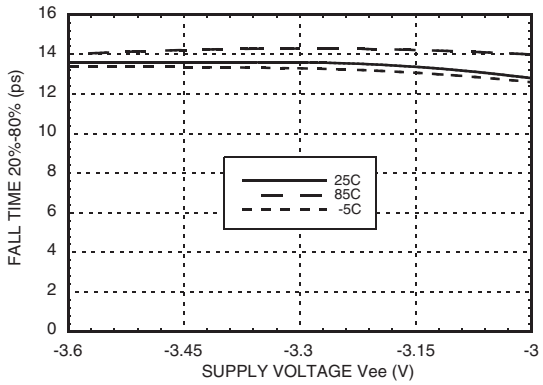
Rise Time vs. Vee Over Temperature, Divide-by-2



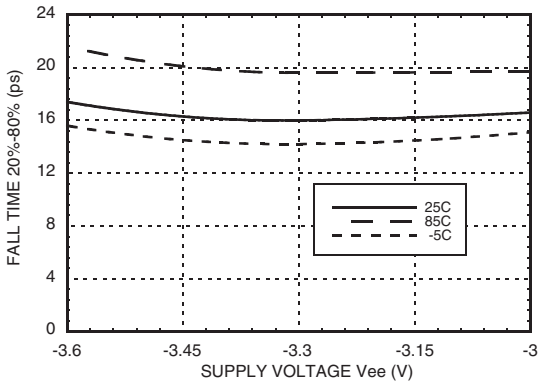
Rise Time vs. Vee Over Temperature, Divide-by-4



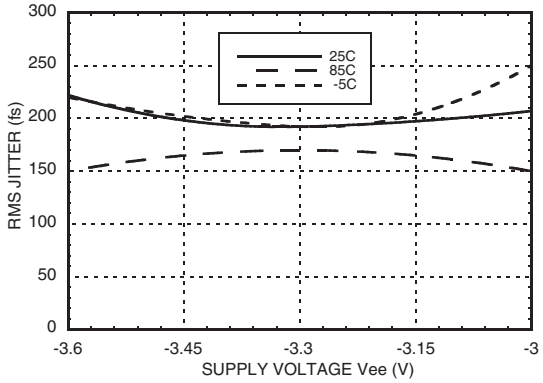
Fall Time vs. Vee Over Temperature, Divide-by-2



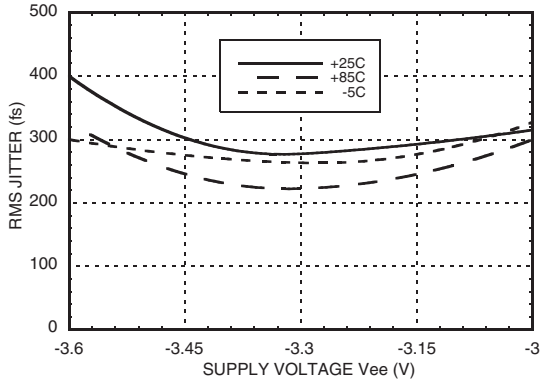
Fall Time vs. Vee Over Temperature, Divide-by-4



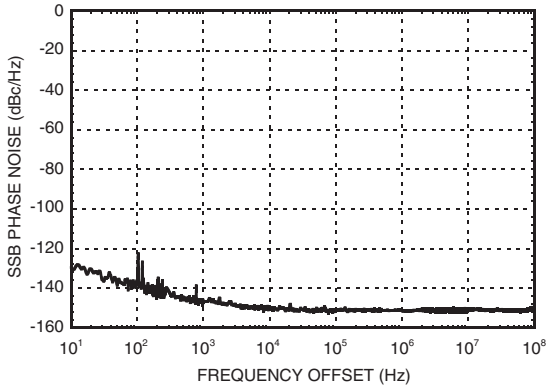
RMS Jitter vs. Vee Over Temperature, Divide-by-2



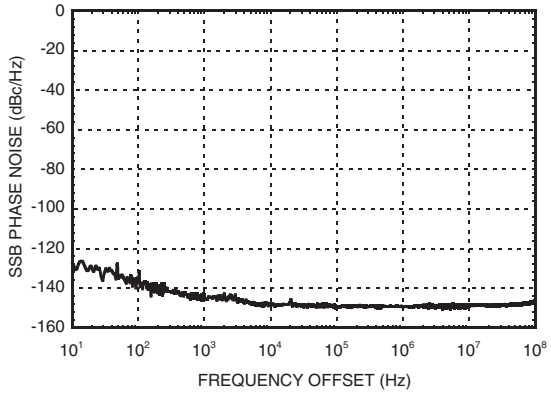
RMS Jitter vs. Vee Over Temperature, Divide-by-4



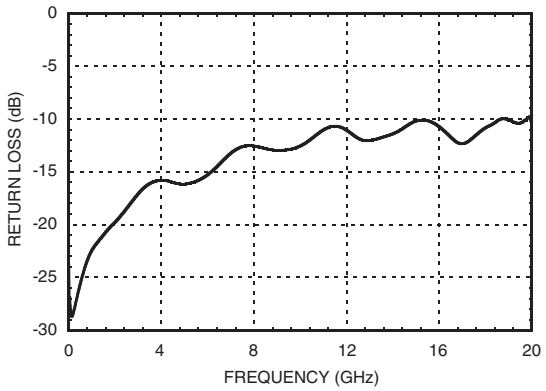
Phase Noise vs. Offset Frequency, Divide-by-2 [1]



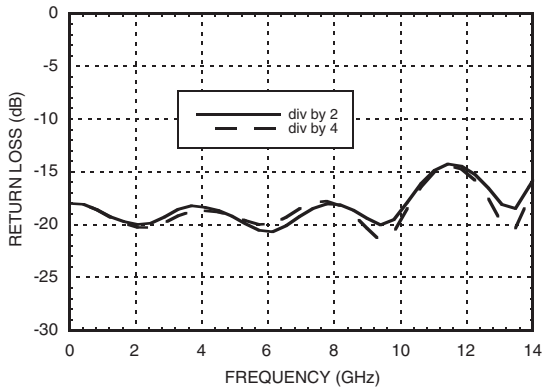
Phase Noise vs. Offset Frequency, Divide-by-4 [1]



Input Return Loss vs. Frequency

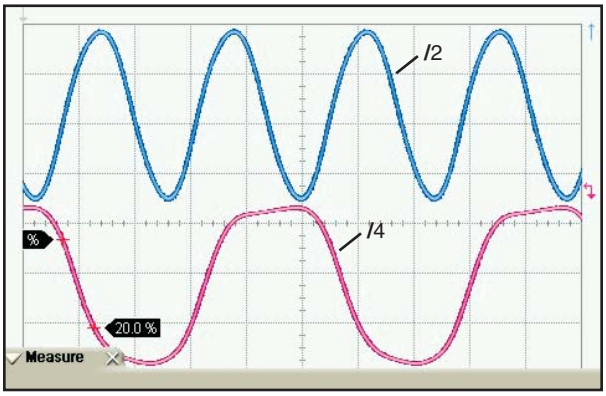


Output Return Loss vs. Frequency



[1] Input Frequency = 10 GHz

Output Signal

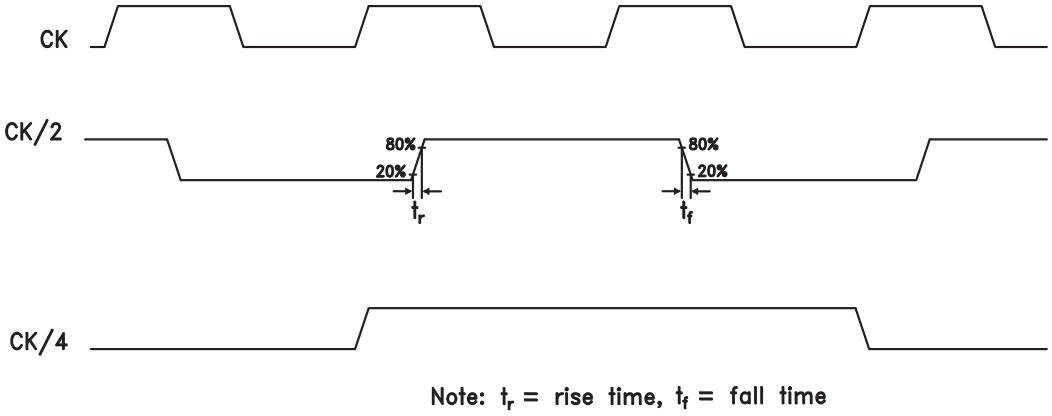


	Measurements			
	Current	Minimum	Maximum	Total Count
Rise Time (/2)	12.00 ps	12.00 ps	12.67 ps	50
Fall Time (/2)	12.67 ps	12.67 ps	13.33 ps	51
Rise Time (/4)	16.67 ps	16.00 ps	16.67 ps	51
Fall Time (/4)	16.67 ps	16.67 ps	16.67 ps	51

Vertical Scale (/2)	65 mV/div
Vertical Scale (/4)	80 mV/div
Horizontal Scale	30.0.ps/div

[1] Test Conditions:
CK/2 and CK/4 outputs are presented on an Infinium 86100C
Input Clock Frequency = 28 GHz
Vin = -6 dBm

Timing Diagram



Note: t_r = rise time, t_f = fall time

Truth Table

Inputs	Outputs (Q_{k-1})		Outputs (Q_k)	
CK	CK/2	CK/4	CK/2	CK/4
L → H	H	H	L	H
L → H	L	H	H	H
L → H	H	L	L	L
L → H	L	L	H	L
H → L	H	H	H	L
H → L	L	H	L	L
H → L	H	L	H	H
H → L	L	L	L	H

Notes:
CK = CKP- CKN
CK/2 = CKP/2 – CKN/2
CK/4 = CKP/4 – CKN/4
H denotes high voltage level
L denotes low voltage level
L → H denotes rising edge
H → L denotes falling edge

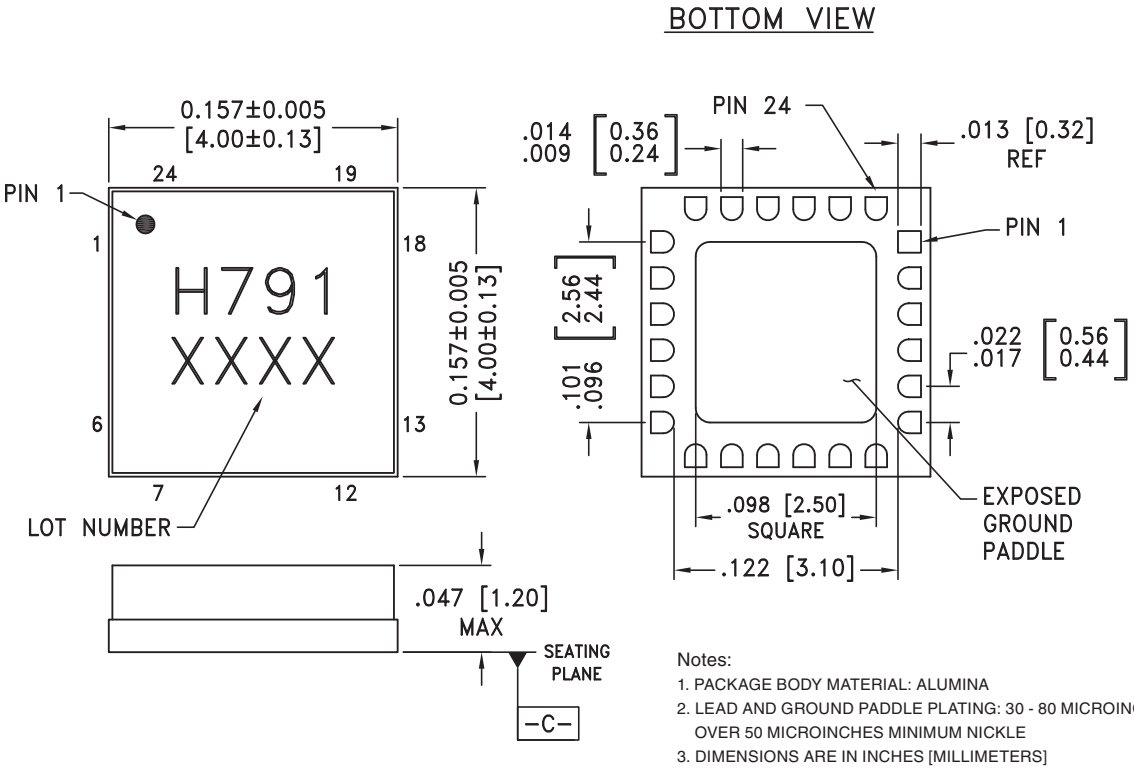
RoHS✓ EARTH FRIENDLY

Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.7V to +0.5V
Input Voltage (Single Ended)	-1.5V to +0.5V
Channel Temperature	125°C
Continuous Pdiss (T = 85°C) (derate 26.4 mW/°C above 85°C)	1.06 W
Thermal Resistance (channel to ground paddle)	37.88 C/W
Storage Temperature	-65°C to +125°C
Operating Temperature	-5°C to +85°C

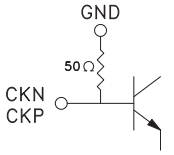
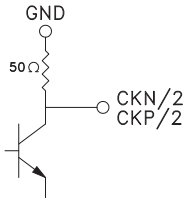
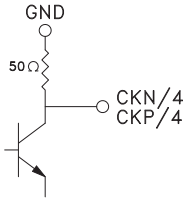
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing

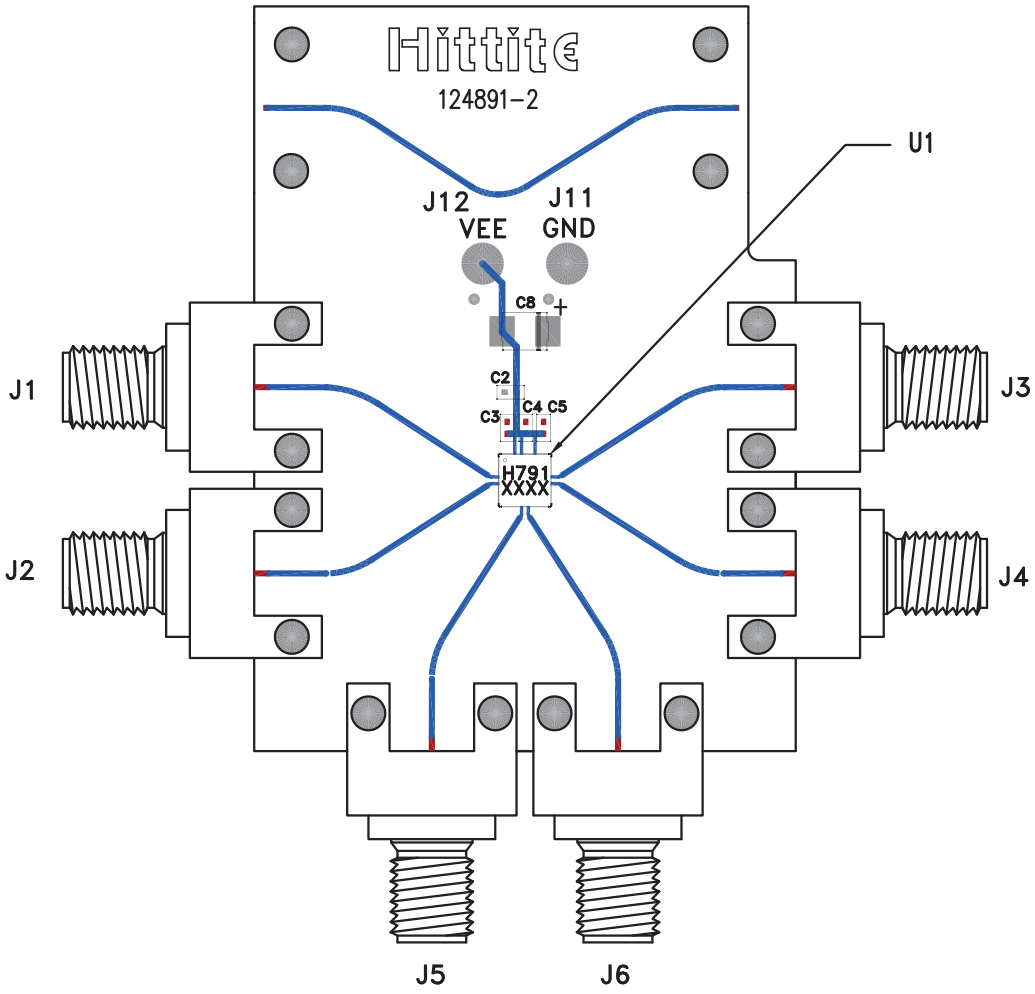


Notes:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30 - 80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKLE
3. DIMENSIONS ARE IN INCHES [MILLIMETERS]
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND
7. CLASSIFIED AS A MOISTURE SENSITIVITY LEVEL (MSL) 1.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 6, 7, 12, 13, 18, 19	N/C	No connection	
2, 5, 8, 11, 14, 17, 21, 24	GND	Signal and Supply Ground	
3, 4	CKN, CKP	Differential (CKP-CKN) or single ended (CKP) clock inputs	
9, 10	CKN/2, CKP/2	Differential divide-by-2 outputs	
15, 16	CKN/4, CKP/4	Differential divide-by-4 outputs	
20, 22, 23	Vee3, Vee2, Vee1	Power Supply (-3.3V)	

Evaluation PCB



List of Materials for Evaluation PCB 126499 [1]

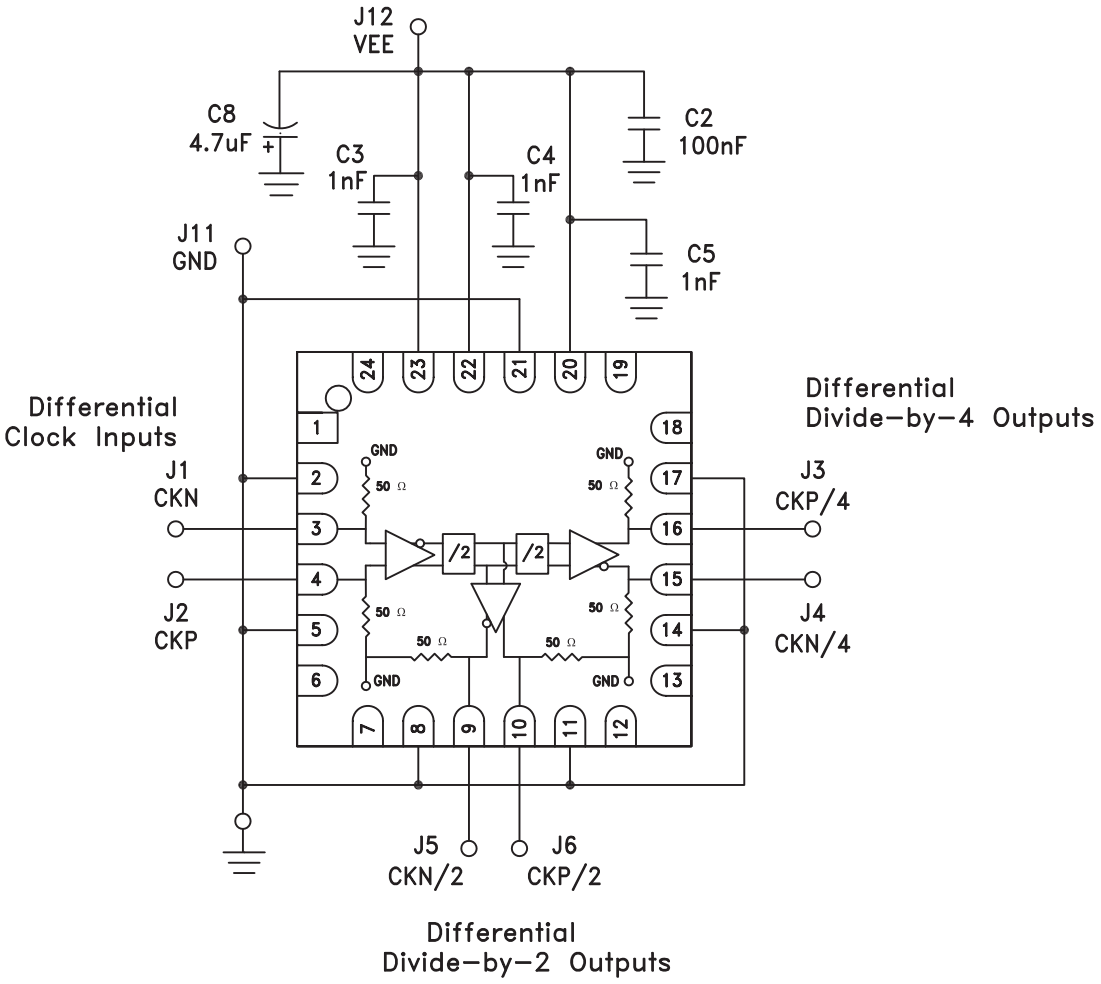
Item	Description
J1 - J6	K Connector
J11 - J12	DC Pin
C2	100 pF Capacitor, 0402 Pkg.
C3 - C5	1 nF Capacitor, 0402 Pkg.
C8	4.7 µF Capacitor, Tantalum
U1	HMC791LC4B Divide-by-2, Divide-by-4
PCB [2]	124891 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed packaged base should be connected to GND. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit - Recommended Differential Configuration



Application Circuit - Recommended Single-Ended Configuration