16M x 32 Mobile DDR Synchronous DRAM (SDRAM)

Etron Confidential **Advanced (Rev. 1.0 Mar. /2009)**

Features

- Fast clock rate: 166/133 MHz
- Differential Clock CK & $\overline{CK}$
- Bi-directional DQS
- Four internal banks, 4M x 32-bit for each bank
- Edge-aligned with read data, centered in write data
- Programmable Mode and Extended Mode Registers
  - $\overline{CAS}$ Latency: 2, or 3
  - Burst length: 2, 4, 8, or 16
  - Burst Type: Sequential & Interleaved
  - PASR (Partial Array Self Refresh)
  - Auto TCSR (Temperature Compensated Self Refresh)
  - DS (Drive Strength)
- Individual byte writes mask control
- DM Write Latency = 0
- Precharge Standby Current = 300 μA
- Self Refresh Current = 700 μA
- Deep power-down Current = 10 μA max. at 85°C
- Auto Refresh and Self Refresh
- 8192 refresh cycles / 64ms
- No DLL (Delay Lock Loop), to reduce power; CK to DQS is not synchronized.
- Power supplies: V_{DD} & V_{DDQ} = +1.8V+0.15V/-0.1V
- Interface: LVCMOS
- Ambient Temperature T_A = -25 ~ 85°C,
- 90-ball 8mm x 13mm VFBGA package
  - Pb free and Halogen free

Overview

The EM68B32D is 536,870,912 bits of double data rate synchronous DRAM organized as 4 banks of 4,194,304 words by 32 bits. The synchronous operation with Data Strobe allows extremely high performance. EM68B32D is applied to reduce leakage and refresh currents while achieving very high speed. I/O transactions are possible on both edges of the clock. The ranges of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

Table 1. Ordering Information

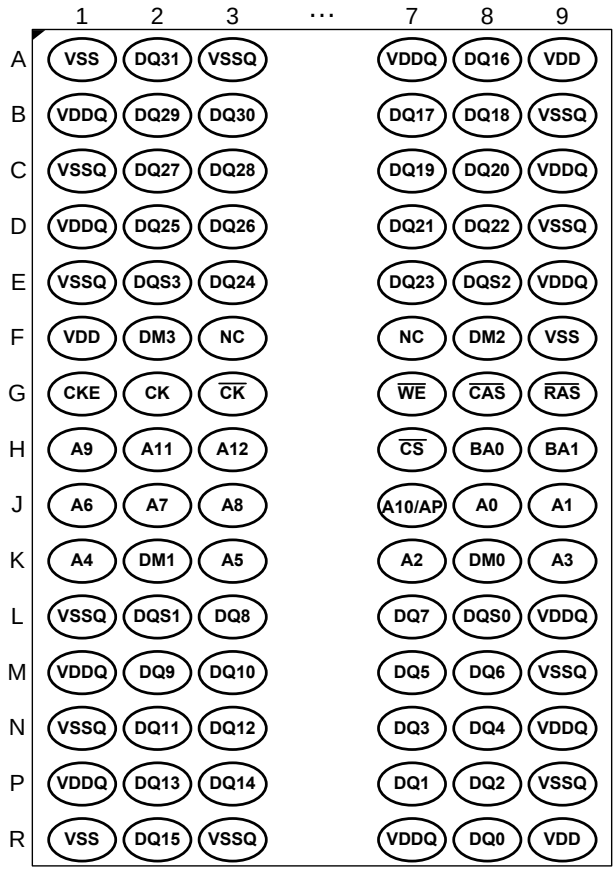
Part Number	Clock Frequency	Data Rate	IDD6	Package
EM68B32DVKA-6H	166MHz	333Mbps/pin	700 μA	VFBGA
EM68B32DVKA-75H	133MHz	266Mbps/pin	700 μA	VFBGA

VK: indicates VFBGA package

A: indicates Generation Code

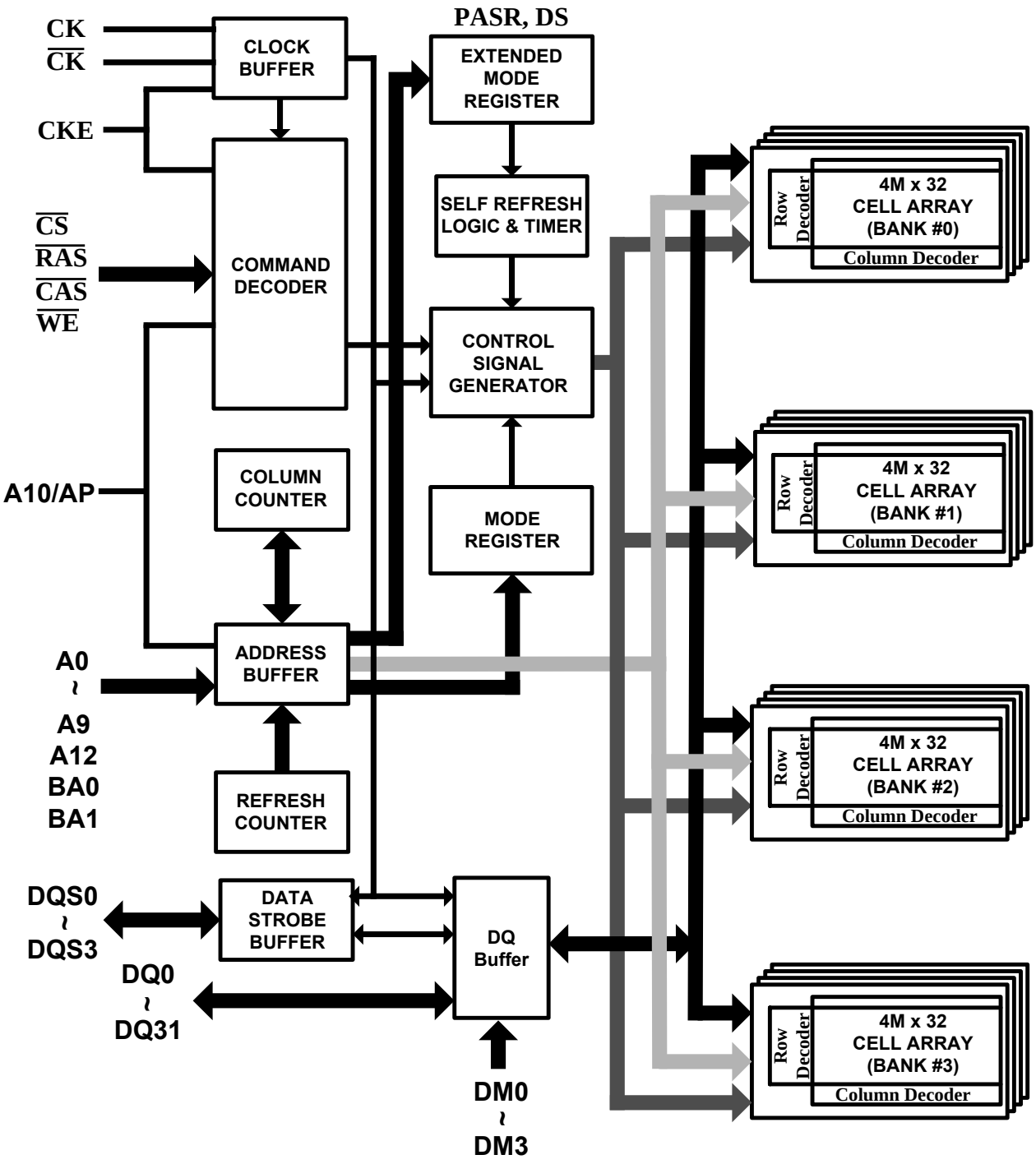
H: indicates Pb and Halogen Free for VFBGA Package

Figure 1. Ball Assignment (Top View)



Etron Technology, Inc.
No. 6, Technology Rd. V, Hsinchu Science Park, Hsinchu, Taiwan 30078, R.O.C.
TEL: (886)-3-5782345 FAX: (886)-3-5778671

Figure 2. Block Diagram



Pin Descriptions

Table 2. Pin Details of EM68B32D

Symbol	Type	Description
CK, $\overline{CK}$	Input	**Differential Clock:** CK, $\overline{CK}$ are driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. Both CK and $\overline{CK}$ increment the internal burst counter and controls the output registers.
CKE	Input	**Clock Enable:** CKE activates (HIGH) and deactivates (LOW) the CK signal. Internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power Down and Self Refresh operation (all banks idle) or Active Power Down (Row Active in any bank). CKE is synchronous for all functions except for disabling outputs, which is asynchronous. Input buffers, excluding CK, $\overline{CK}$ and CKE, are disabled during Power Down and Self Refresh modes to reduce standby power consumption.
BA0, BA1	Input	**Bank Activate:** BA0 and BA1 define to which bank the BankActivate, Read, Write, or BankPrecharge command is being applied. BA0 and BA1 also determine which mode register (MRS or EMRS) is loaded during a Mode Register Set command.
A0-A12	Input	**Address Inputs:** A0-A12 are sampled during the BankActivate command (row address A0-A12) and Read/Write command (column address A0-A8 with A10 defining Auto Precharge).
$\overline{CS}$	Input	**Chip Select:** $\overline{CS}$ enables (sampled LOW) and disables (sampled HIGH) the command decoder. All commands are masked when $\overline{CS}$ is sampled HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. It is considered part of the command code.
$\overline{RAS}$	Input	**Row Address Strobe:** The $\overline{RAS}$ signal defines the operation commands in conjunction with the $\overline{CAS}$ and $\overline{WE}$ signals and is latched at the positive edges of CK. When $\overline{RAS}$ and $\overline{CS}$ are asserted "LOW" and $\overline{CAS}$ is asserted "HIGH," either the BankActivate command or the Precharge command is selected by the $\overline{WE}$ signal. When the $\overline{WE}$ is asserted "HIGH," the BankActivate command is selected and the bank designated by BA is turned on to the active state. When the $\overline{WE}$ is asserted "LOW," the Precharge command is selected and the bank designated by BA is switched to the idle state after the precharge operation.
$\overline{CAS}$	Input	**Column Address Strobe:** The $\overline{CAS}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{WE}$ signals and is latched at the positive edges of CK. When $\overline{RAS}$ is held "HIGH" and $\overline{CS}$ is asserted "LOW," the column access is started by asserting $\overline{CAS}$ "LOW." Then, the Read or Write command is selected by asserting $\overline{WE}$ "HIGH " or LOW"."
$\overline{WE}$	Input	**Write Enable:** The $\overline{WE}$ signal defines the operation commands in conjunction with the $\overline{RAS}$ and $\overline{CAS}$ signals and is latched at the positive edges of CK. The $\overline{WE}$ input is used to select the BankActivate or Precharge command and Read or Write command.
DQS0 -DQS3	Input / Output	**Bidirectional Data Strobe:** The DQSx signals are mapped to the following data bytes: DQS0 to DQ0-DQ7, DQS1 to DQ8-DQ15, DQS2 to DQ16-DQ23, and DQS3 to DQ24-DQ31.
DM0 - DM3	Input	**Data Input Mask:** DM0-DM3 are byte specific. Input data is masked when DM is sampled HIGH during a write cycle. DM3 masks DQ31-DQ24, DM2 masks DQ23-DQ16, DM1 masks DQ15-DQ8, and DM0 masks DQ7-DQ0.

DQ0 – DQ31	Input / Output	**Data I/O:** The DQ0-DQ31 input and output data are synchronized with the positive edges of CK and $\overline{CK}$. The I/Os are byte-maskable during Writes.
V_{DD}	Supply	**Power Supply:** +1.8V+0.15V/-0.1V
V_{SS}	Supply	**Ground**
V_{DDQ}	Supply	**DQ Power:** +1.8V+0.15V/-0.1V. Provide isolated power to DQs for improved noise immunity.
V_{SSQ}	Supply	**DQ Ground:** Provide isolated ground to DQs for improved noise immunity.
NC	-	**No Connect:** No internal connection, these pins suggest to be left unconnected.

Operation Mode

Fully synchronous operations are performed to latch the commands at the positive edges of CK. Table 3 shows the truth table for the operation commands.

Table 3. Truth Table (Note (1), (2))

Command	State	CKEn-1	CKEn	DM	BA1	BA0	A10	A12-A11, A9-0	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
BankActivate	Idle(3)	H	X	X	V	V	Row Address		L	L	H	H
BankPrecharge	Any	H	X	X	V	V	L	X	L	L	H	L
PrechargeAll	Any	H	X	X	X	X	H	X	L	L	H	L
Write	Active(3)	H	X	V	V	V	L	Column Address A0~A8	L	H	L	L
Write and AutoPrecharge	Active(3)	H	X	V	V	V	H		L	H	L	L
Read	Active(3)	H	X	X	V	V	L		L	H	L	H
Read and Autoprecharge	Active(3)	H	X	X	V	V	H		L	H	L	H
Mode Register Set	Idle	H	X	X	L	L	OP code		L	L	L	L
Extended Mode Register Set	Idle	H	X	X	H	L			L	L	L	L
No-Operation	Any	H	X	X	X	X	X	X	L	H	H	H
Device Deselect	Any	H	X	X	X	X	X	X	H	X	X	X
Burst Stop	Active(4)	H	X	X	X	X	X	X	L	H	H	L
AutoRefresh	Idle	H	H	X	X	X	X	X	L	L	L	H
SelfRefresh Entry	Idle	H	L	X	X	X	X	X	L	L	L	H
SelfRefresh Exit	Idle (Self Refresh)	L	H	X	X	X	X	X	H	X	X	X
									L	H	H	H
Power Down Mode Entry	Idle/Active(5)	H	L	X	X	X	X	X	H	X	X	X
									L	H	H	H
Power Down Mode Exit	Any (Power Down)	L	H	X	X	X	X	X	H	X	X	X
									L	H	H	H
Deep Power Down Entry	Any	H	L	X	X	X	X	X	L	H	H	L
Deep Power Down Exit	Any	L	H	X	X	X	X	X	H	X	X	X
Data Mask Enable	Active	H	X	L	X	X	X	X	X	X	X	X
Data Mask Disable	Active	H	X	H	X	X	X	X	X	X	X	X

Note: 1. V = Valid data, X = Don't Care, L = Low level, H = High level
2. CKE_n signal is input level when commands are provided.
CKE_{n-1} signal is input level one clock cycle before the commands are provided.
3. These are states of bank designated by BA0, BA1signals.
4. Read burst stop with BST command for all burst types.
5. Power Down Mode can not enter in the burst operation.
When this command is asserted in the burst cycle, device state is clock suspend mode.

Functional Description

This 512Mb Mobile DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM. Each of the 134,217,728-bit banks is organized as 8,192 rows by 512 columns by 32 bits. The 512Mb Mobile DDR SDRAM uses a double data rate architecture to achieve high speed operation. EM68B32D is applied to reduce leakage and refresh currents while achieving very high speed. The double data rate architecture is essentially a 2n-prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O balls. Single read or write access for the 512Mb Mobile DDR SDRAM consists of a single 2n-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O balls.

Read and write accesses to the Mobile DDR SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0, BA1 select the bank, A0-A12 select the row). The address bits (BA0, BA1 select the bank, A0-A8 select the column) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Note that the DLL (Delay Lock Loop) circuitry used on standard DDR devices is not included in the Mobile DDR SDRAM. It has been omitted to save power.

Prior to normal operation, the Mobile DDR SDRAM must be initialized.

● Power-Up and Initialization

Mobile DDR SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. To properly initialize the Mobile DDR SDRAM, this sequence must be followed:

1. To prevent device latch-up, it is recommended that core power (V_{DD}) and I/O power (V_{DDQ}) be from the same power source and be brought up simultaneously. If separate power sources are used, V_{DD} must lead V_{DDQ}.
2. Once power supply voltages are stable and CKE has been driven High, it is safe to apply the clock.
3. Once the clock is stable, a 200μs (minimum) delay is required by the Mobile DDR SDRAM prior to applying an executable command. During this time, NOP or Deselect commands must be issued on the command bus.
4. Issue a Precharge All command.
5. Issue NOP or Deselect commands for at least t_{RP} time.
6. Issue an Auto Refresh command followed by NOP or Deselect commands for at least t_{RFC} time. Issue a second Auto Refresh command followed by NOP or Deselect commands for at least t_{RFC} time. As part of the individualization sequence, two Auto Refresh commands must be issued. Typically, both of these commands are issued at this stage as described above. Alternately, the second Auto Refresh command and NOP or Deselect sequence can be issued between steps 10 and 11.
7. Using the Mode Register Set command, load the standard Mode Register as desired.
8. Issue NOP or Deselect commands for at least t_{MRD} time.
9. Using the Mode Register Set command, load the Extended Mode Register to the desired operating modes. Note that the sequence in which the standard and extended mode registers are programmed is not critical.
10. Issue NOP or Deselect commands for at least t_{MRD} time.
11. The Mobile DDR SDRAM has been properly initialized and is ready to receive any valid command.

● Mode Register Set(MRS)

The Mode Register stores the data for controlling various operating modes of a DDR SDRAM. It programs $\overline{CAS}$ Latency, Burst Type, and Burst Length to make the Mobile DDR SDRAM useful for a variety of applications. The default value of the Mode Register is not defined; therefore the Mode Register must be written by the user. Values stored in the register will be retained until the register is reprogrammed, the device enters Deep Power Down mode, or power is removed from the device. The Mode Register is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA1 and BA0 (the device should have all banks idle with no bursts in progress prior to writing into the mode register, and CKE should be High). The state of address pins A0~A12 and BA0, BA1 in the same cycle in which $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are asserted Low is written into the Mode Register. A minimum of two clock cycles, t_{MRD}, are required to complete the write operation in the Mode Register. The Mode Register is divided into various fields depending on functionality. The Burst Length uses A0~A2, Burst Type uses A3, and $\overline{CAS}$ Latency (read latency from column address) uses A4~A6. A logic 0 should be programmed to all the undefined addresses to ensure future compatibility. Reserved states should not be used to avoid unknown device operation or incompatibility with future versions. Refer to the table for specific codes for various burst lengths, burst types and $\overline{CAS}$ latencies.

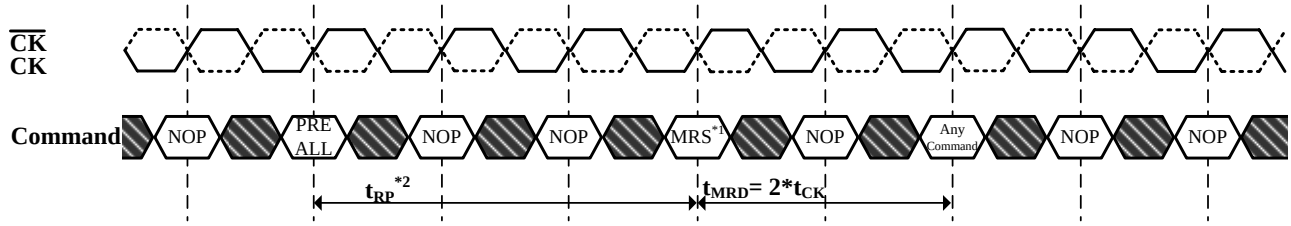
Table 4. Mode Register Bitmap

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
															Address Field
0	0	0	0			0	0	$\overline{CAS}$ Latency			BT	Burst Length			Mode Register

A6	A5	A4	$\overline{CAS}$ Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved



***1: MRS can be issued only with all banks in the idle state.**
***2: A minimum delay of tRP is required before issuing an MRS command.**

Don't Care

Figure 3.Mode Register Set Cycle

Burst Mode Operation

Burst Mode operation is used to provide a constant flow of data to memory locations (write cycle) or from memory locations (read cycle). There are two parameters that define how the Burst Mode operates. These parameters include Burst Type and Burst Length and are programmed by addresses A0~A3 during the Mode Register Set command. Burst Type is used to define the sequence in which the burst data will be delivered from or stored to the DDR SDRAM. Two types of burst sequences are supported, Sequential and Interleaved. See the table below. The Burst Length controls the number of bits that will be output after a read command, or the number of bits to be input after a write command. The Burst Length can be programmed to have a value of 2, 4, 8, or 16.

Table 5.Burst Definition

Burst Length	Start Address				Sequential	Interleave
	A3	A2	A1	A0		
2	X	X	X	0	0,1	0,1
	X	X	X	1	1,0	1,0
4	X	X	0	0	0, 1, 2, 3	0, 1, 2, 3
	X	X	0	1	1, 2, 3, 0	1, 0, 3, 2
	X	X	1	0	2, 3, 0, 1	2, 3, 0, 1
	X	X	1	1	3, 0, 1, 2	3, 2, 1, 0
8	X	0	0	0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	X	0	0	1	1, 2, 3,4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
	X	0	1	0	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
	X	0	1	1	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
	X	1	0	0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	X	1	0	1	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
	X	1	1	0	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
	X	1	1	1	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0
16	0	0	0	0	0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15	0,1,2,3,4,5,6,7,8,9,10,11,12,13,14,15
	0	0	0	1	1,2,3,4,5,6,7,8,9,10,11,12,13,14,15,0	1,0,3,2,5,4,7,6,9,8,11,10,13,12,15,14
	0	0	1	0	2,3,4,5,6,7,8,9,10,11,12,13,14,15,0,1	2,3,0,1,6,7,4,5,10,11,8,9,14,15,12,13
	0	0	1	1	3,4,5,6,7,8,9,10,11,12,13,14,15,0,1,2	3,2,1,0,7,6,5,4,11,10,9,8,15,14,13,12
	0	1	0	0	4,5,6,7,8,9,10,11,12,13,14,15,0,1,2,3	4,5,6,7,0,1,2,3,12,13,14,15,8,9,10,11
	0	1	0	1	5,6,7,8,9,10,11,12,13,14,15,0,1,2,3,4	5,4,7,6,1,0,3,2,13,12,15,14,9,8,11,10
	0	1	1	0	6,7,8,9,10,11,12,13,14,15,0,1,2,3,4,5	6,7,4,5,2,3,0,1,14,15,12,13,10,11,8,9
	0	1	1	1	7,8,9,10,11,12,13,14,15,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0,15,14,13,12,11,10,9,8
	1	0	0	0	8,9,10,11,12,13,14,15,0,1,2,3,4,5,6,7	8,9,10,11,12,13,14,15,0,1,2,3,4,5,6,7
	1	0	0	1	9,10,11,12,13,14,15,0,1,2,3,4,5,6,7,8	9,8,11,10,13,12,15,14,1,0,3,2,5,4,7,6
	1	0	1	0	10,11,12,13,14,15,0,1,2,3,4,5,6,7,8,9	10,11,8,9,14,15,12,13,2,3,0,1,6,7,4,5
	1	0	1	1	11,12,13,14,15,0,1,2,3,4,5,6,7,8,9,10	11,10,9,8,15,14,13,12,3,2,1,0,7,6,5,4
	1	1	0	0	12,13,14,15,0,1,2,3,4,5,6,7,8,9,10,11	12,13,14,15,8,9,10,11,4,5,6,7,0,1,2,3
	1	1	0	1	13,14,15,0,1,2,3,4,5,6,7,8,9,10,11,12	13,12,15,14,9,8,11,10,5,4,7,6,1,0,3,2
	1	1	1	0	14,15,0,1,2,3,4,5,6,7,8,9,10,11,12,13	14,15,12,13,10,11,8,9,6,7,4,5,2,3,0,1
	1	1	1	1	15,0,1,2,3,4,5,6,7,8,9,10,11,12,13,14	15,14,13,12,11,10,9,8,7,6,5,4,3,2,1,0

Extended Mode Register Set (EMRS)

The Extended Mode Register is designed to support Partial Array Self Refresh and Driver Strength. The EMRS cycle is not mandatory, and the EMRS command needs to be issued only when either PASR or DS is used. The Extended Mode Register is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and BA0 and High on BA1 (the device should have all banks idle with no bursts in progress prior to writing into the Extended Mode Register, and CKE should be High). Values stored in the register will be retained until the register is reprogrammed, the device enters Deep Power Down mode, or power is removed from the device. The state of address pins A0~A12 and BA0, BA1 in the same cycle in which $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are asserted Low is written into the Extended Mode Register. Two clock cycles, t_{MRD}, are required to complete the write operation in the Extended Mode Register. A0~A2 are used for Partial Array Self Refresh and A5~A6 are used for Driver Strength. An automatic Temperature Compensated Self Refresh function is included with a temperature sensor embedded into this device. A3~A4 are no longer used to control this function; any inputs applied to A3~A4 during EMRS are ignored. All the other address pins, A7~A12 and BA0, must be set to Low for proper EMRS operation. Refer to the tables below for specific codes. If the user does not write values to the Extended Mode Register, DS defaults to Full Strength; and PASR defaults to the Full Array.

Table 6. Extend Mode Register Bitmap

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	
1	0	0	0			0	0	DS		0	0	PASR			Mode Register

A6	A5	Drive Strength
0	0	Full Strength
0	1	1/2 Strength
1	0	1/4 Strength
1	1	1/8 Strength

A2	A1	A0	Partial Array Self Refresh Coverage
0	0	0	Full Array (All Banks)
0	0	1	Half of Full Array (BA1=0)
0	1	0	Quarter of Full Array (BA1=BA0=0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

TEMPERATURE COMPENSATED SELF REFRESH

In order to reduce power consumption, a Mobile DDR SDRAM includes the internal temperature sensor and other circuitry to control Self Refresh operation automatically according to two temperature ranges: max. 40°C and max. 85°C

Table 7. IDD6 Specifications and Conditions

Temperature Range	Self Refresh Current (I_{DD6})			
	Full Array	1/2 of Full Array	1/4 of Full Array	Unit
Max. 40°C	490	350	280	μA
Max. 85°C	700	460	340	μA

PARTIAL ARRAY SELF REFRESH

For further power savings during Self Refresh, the PASR feature allows the controller to select the amount of memory that will be refreshed during Self Refresh. The refresh options are all banks (banks 0, 1, 2 and 3); two banks (bank 0 and 1); and one bank (bank 0). Write and Read commands can still affect any bank during standard operations, but only the selected banks will be refreshed during Self Refresh. Data in unselected banks will be lost.

Bank Activation / Row Address Command

The Bank Activation / Row Address command, also called the Active command, is issued by holding $\overline{CAS}$ and $\overline{WE}$ High with $\overline{CS}$ and $\overline{RAS}$ Low at the rising edge of the clock (CK). The DDR SDRAM has four independent banks, so two Bank Select Addresses (BA0, BA1) are required. The Active command must be applied before any read or write operation is executed. The delay from the Active command to the first Read or Write command must meet or exceed the minimum of $\overline{RAS}$ to $\overline{CAS}$ delay time (t_{RCD} min). Once a bank has been activated, it must be precharged before another Active command can be applied to the same bank. The minimum time interval between interspersed Active commands (Bank 0 to Bank 3, for example) is the bank to bank delay time (t_{RRD} min).

Burst Read Operation

Burst Read operation in a DDR SDRAM is initiated by asserting $\overline{CS}$ and $\overline{RAS}$ Low while holding $\overline{RAS}$ and $\overline{WE}$ High at the rising edge of the clock (CK) after tRCD from the Active command. The address inputs (A0~A8) determine the starting address for the Burst. The Mode Register sets the type of burst (Sequential or Interleaved) and the burst length (2, 4, 8, or 16). The first output data is available after the $\overline{CAS}$ Latency from the Read command, and the consecutive data bits are presented on the falling and rising edges of Data Strobe (DQS) as supplied by the DDR SDRAM until the burst is completed.

Burst Write Operation

The Burst Write command is issued by having $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ Low while holding $\overline{RAS}$ High at the rising edge of the clock (CK). The address inputs determine the starting column address. There is no write latency relative to DQS required for the Burst Write cycle. The first data for a Burst Write cycle must be applied at the first rising edge of the data strobe enabled after t_{DQSS} from the rising edge of the clock when the Write command was issued. The remaining data inputs must be supplied on each subsequent falling and rising edge of Data Strobe until the burst length is completed. After the burst has finished, any additional data supplied to the DQ pins will be ignored.

Burst Interruption

Read Interrupted by Read

Burst Read can be interrupted before completion of the burst by a new Read command to any bank. When the previous burst is interrupted, data bits from the remaining addresses are overridden by data from the new addresses with the full burst length. The data from the previous Read command continues to appear on the outputs until the $\overline{CAS}$ latency from the interrupting Read command is satisfied. At this point the data from the interrupting Read command appears. The Read to Read interval is a minimum of 1 clock.

Read Interrupted by Burst Stop & Write

To interrupt Burst Read with a write command, the Burst Stop command must be asserted to avoid data contention on the I/O bus by placing the DQ (output drivers) in a high impedance state. To ensure the DQ are tri-stated one cycle before the beginning of the write operation, the Burst Stop command must be applied at least 2 clock cycles for CL = 2 and at least 3 clock cycles for CL = 3 before the Write command.

Read Interrupted by Precharge

Burst Read can be interrupted by a Precharge of the same bank. A minimum of 1 clock cycle is required for the read precharge interval. A Precharge command to output disable latency is equivalent to the $\overline{CAS}$ latency.

Write Interrupted by Write

A Burst Write can be interrupted by the new Write command before completion of the previous Burst Write, with the only restriction being that the interval that separates the commands must be at least one clock cycle. When the previous burst is interrupted, the remaining addresses are overridden by the new addresses and the new data will be written into the device until the programmed Burst Length is satisfied.

Write Interrupted by Read & DM

A Burst Write can be interrupted by a Read command to any bank. The DQ must be in the high impedance state at least one clock cycle before the interrupting read data appears on the outputs to avoid data contention. When the Read command is to be asserted, any residual data from the Burst Write sequence must be masked by DM. The delay from the last data to the Read command (t_{WTR}) is required to avoid data contention inside the DRAM. Data presented on the DQ pins before the Read command is initiated will actually be written to the memory. A Read command interrupting a write sequence can not be issued at the next clock edge following the Write command.

Write Interrupted by Precharge & DM

A Burst Write can be interrupted by a Precharge of the same bank before completion of the previous burst. A write recovery time (t_{WR}) is required from the last data to the Precharge command. When the Precharge command is asserted, any residual data from the Burst Write cycle must be masked by DM.

● Burst Stop Command

The Burst Stop command is initiated by having $\overline{RAS}$ and $\overline{CAS}$ High with $\overline{CS}$ and $\overline{WE}$ Low at the rising edge of the clock only. The Burst Stop command has the fewest restrictions, making it the easiest method to use when terminating a burst operation before it has been completed. When the Burst Stop command is issued during a Burst Read cycle, both the data and DQS (Data Strobe) go to a high impedance state after a delay which is equal to the $\overline{CAS}$ latency set in the Mode Register. The Burst Stop command, however, is not supported during a Burst Write operation.

● DM Masking Function

The DDR SDRAM has a Data Mask function that can be used in conjunction with the data write cycle only, not the read cycle. When the Data Mask is activated (DM High) during a write operation, the write data is masked immediately (DM to Data Mask latency is zero). DM must be issued at the rising edge or the falling edge of Data Strobe instead of at a clock edge.

● Auto Precharge Operation

Auto Precharge is a feature which performs the same individual bank precharge function as described above, but without requiring an explicit command. This is accomplished by using A10 (A10 = High), to enable Auto Precharge in conjunction with a specific READ or WRITE command. A precharge of the bank / row that is addressed with the READ or WRITE command is automatically performed upon completion of the read or write burst. Auto Precharge is non persistent in that it is either enabled or disabled for each individual READ or WRITE command. Auto Precharge ensures that a precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharging time (t_{RP}) is completed. When the Auto Precharge command is activated, the active bank automatically begins to precharge at the earliest possible moment during a read or write cycle after t_{RAS} (min) is satisfied.

● Precharge Command

The Precharge command is issued when $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ are Low and $\overline{CAS}$ is High at the rising edge of the clock (CK). The Precharge command can be used to precharge any bank individually or all banks simultaneously. The Bank Select addresses (BA0, BA1) are used to define which bank is precharged when the command is initiated. For a write cycle, t_{WR} (min) must be satisfied from the start of the last Burst Write cycle until the Precharge command can be issued. After t_{RP} from the precharge, an Active command to the same bank can be initiated.

Auto Refresh

An Auto Refresh command is issued by having $\overline{CS}$, $\overline{RAS}$, and $\overline{CAS}$ held Low with CKE and $\overline{WE}$ High at the rising edge of the clock (CK). All banks must be precharged and idle for a tRP (min) before the Auto Refresh command is applied. The refresh addressing is generated by the internal refresh address counter. This makes the address bits " Don't Care " during an Auto Refresh command. When the refresh cycle is complete, all banks will be in the idle state. A delay between the Auto Refresh command and the next Active command or subsequent Auto Refresh command must be greater than or equal to the t_{RFC} (min).

Self Refresh

A Self Refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE Low with $\overline{WE}$ High at the rising edge of the clock (CK). Once the Self Refresh command has been initiated, CKE must be held Low to keep the device in Self Refresh mode. During the Self Refresh operation, all inputs except CKE are ignored. The clock is internally disabled during Self Refresh operation to reduce power consumption. To exit the Self Refresh mode, supply a stable clock input before returning CKE high, assert Deselect or a NOP command, and then assert CKE high.

Power Down Mode

The device enters Power Down mode when CKE is brought Low, and it exits when CKE returns High. Once the Power Down mode is initiated, all of the receiver circuits except CK and CKE are gated off to reduce power consumption. All banks should be in an idle state prior to entering the Precharge Power Down mode and CKE should be set high at least t_{XP} prior to an Active command. During Power Down mode, refresh operations cannot be performed; therefore the device must remain in Power Down mode for a shorter time than the refresh period (t_{REF}) of the device.

Deep Power Down

Deep Power Down achieves maximum power reduction by eliminating the power of the whole memory array and surrounding circuitry. Data will not be retained in the memory storage array, the Mode Register, or the Extended Mode Register once the device enters Deep Power Down mode.

This mode is entered by having all banks idle then $\overline{CS}$ and $\overline{WE}$ held Low with $\overline{RAS}$ and $\overline{CAS}$ held High at the rising edge of the clock, while CKE is Low. This mode is exited by asserting CKE High, applying only NOP commands for 200 microseconds, and then continuing with steps 4 through 11 of the Power Up and Initialization sequence..

Table 8. Absolute Maximum Rating

Symbol	Parameter	Rating	Unit
		-6/75	
V_{IN}, V_{OUT}	I/O Pins Voltage	-0.5~2.7	V
V_{DD}, V_{DDQ}	Power Supply Voltage	-0.5~2.7	V
T_A	Ambient Temperature	-25~85	°C
T_{STG}	Storage Temperature	- 55~150	°C
P_D	Power Dissipation	0.7	W
I_{OUT}	Short Circuit Output Current	50	mA

Note:

1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage of the devices.
2. All voltages are referenced to V_{SS}.
3. Functional operation should be restricted to Recommended Operating Conditions.
4. Exposure to higher than the recommended voltages for extended periods of time could affect device reliability

Table 9. Recommended D.C. Operating Conditions (V_{DD}=1.7V~1.95V, T_A =-25~85°C)

Parameter	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	1.7	1.95	V	
Power Supply Voltage (for I/O Buffer)	V_{DDQ}	1.7	1.95	V	
Input High Voltage (DC)	V_{IH} (DC)	0.7 x V_{DDQ}	V_{DDQ} + 0.3	V	
Input Low Voltage (DC)	V_{IL} (DC)	-0.3	0.3 x V_{DDQ}	V	
Input leakage current	I_{IL}	-2	2	μA	
Output leakage current	I_{OZ}	-5	5	μA	
Output High Voltage	V_{OH}	0.9 x V_{DDQ}	-	V	I_{OH}=-0.1mA
Output Low Voltage	V_{OL}	-	0.1 x V_{DDQ}	V	I_{OL}=0.1mA

Note: These parameters are guaranteed by design, periodically sampled and are not 100% tested.

Table 10. Capacitance (V_{DD}=1.7V~1.95V, f = 1MHz, T_A = 25 °C)

Symbol	Parameter	Min.	Max.	Delta	Unit
C_{IN1}	Input Capacitance (CK, $\overline{CK}$)	1.5	3	0.25	pF
C_{IN2}	Input Capacitance (all other input-only pins)	1.5	3	0.5	pF
$C_{I/O}$	DQ, DQS, DM Input/Output Capacitance	3	5	0.5	pF

Note: These parameters are guaranteed by design, periodically sampled and are not 100% tested.

Table 11. D.C. Characteristics (V_{DD}=1.7V~1.95V, T_A =-25~85°C)

Parameter & Test Condition		Symbol	-6	-75	Unit
			MAX		
Operating one bank active-precharge current: $t_{RC}=t_{RC}$(min); $t_{CK}=t_{CK}$(min); CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; Address inputs are SWITCHING; data bus inputs are STABLE		IDD0	70	65	mA
Precharge power-down standby current: All banks idle, CKE is LOW; $\overline{CS}$ is HIGH, $t_{CK}=t_{CK}$(min); address and control inputs are SWITCHING; data bus inputs are STABLE		IDD2P	0.3	0.3	mA
Precharge power-down standby current with clock stop: All banks idle, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		IDD2PS	0.3	0.3	mA
Precharge non power-down standby current: All banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, $t_{CK}=t_{CK}$(min); address and control inputs are SWITCHING; data bus inputs are STABLE		IDD2N	15	15	mA
Precharge non power-down standby current with clock stop: All banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		IDD2NS	8	8	mA
Active power-down standby current: One bank active, CKE is LOW; $\overline{CS}$ is HIGH, $t_{CK}=t_{CK}$(min); address and control inputs are SWITCHING; data bus inputs are STABLE		IDD3P	0.5	0.5	mA
Active power-down standby current with clock stop: One bank active, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		IDD3PS	0.5	0.5	mA
Active non power-down standby current: One bank active, CKE is HIGH; $\overline{CS}$ is HIGH, $t_{CK}=t_{CK}$(min) address and control inputs are SWITCHING; data bus inputs are STABLE		IDD3N	15	15	mA
Active non power-down standby current with clock stop: One bank active, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, $\overline{CK}$ = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		IDD3NS	10	10	mA
Operating burst read current: One bank active; BL = 4; CL = 3; $t_{CK}=t_{CK}$(min); continuous read bursts; I_{OUT} = 0 mA address inputs are SWITCHING; 50% data change each burst transfer		IDD4R	130	110	mA
Operating burst write current: One bank active; BL = 4; $t_{CK}=t_{CK}$(min); continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer		IDD4W	130	110	mA
Auto-Refresh current: t_{RC} = t_{RFC}(min); $t_{CK}=t_{CK}$(min); burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		IDD5	90	90	mA
Self refresh current: CKE is LOW, CK = LOW, $\overline{CK}$ = HIGH; Extended Mode Register set to all address and control inputs are STABLE; data bus inputs are STABLE	TCSR Range	IDD6	Max.40	Max.85	℃
	Full Array		490	700	μA
	1/2 Full Array		350	460	μA
	1/4 Full Array		280	340	μA
Deep Power Down Mode Current		IDD8	10		μA

Note:

1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage of the device.
2. All voltages are referenced to V_{SS}.
3. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of t_{CK} and t_{RC}. Input signals are changed one time per two clock cycles.

Table 12. Electrical AC Characteristics (V_{DD}=1.7V~1.95V, T_A =-25~85°C)

Symbol	Parameter		-6		-75		Unit	Note
			Min.	Max.	Min.	Max.		
t_{CK}	Clock cycle time	CL = 2	12	-	12	-	ns	1
		CL = 3	6	100	7.5	100	ns	1
t_{CH}	Clock high level width		0.45	0.55	0.45	0.55	t_{CK}	
t_{CL}	Clock low level width		0.45	0.55	0.45	0.55	t_{CK}	
t_{DQSCK}	DQS-out access time from CK, $\overline{CK}$		2	5.5	2	6	ns	
t_{AC}	Output access time from CK, $\overline{CK}$		2	5.5	2	6	ns	2
t_{DQSQ}	DQS-DQ Skew		-	0.5	-	0.6	ns	
t_{RPRE}	Read preamble		0.9	1.1	0.9	1.1	t_{CK}	
t_{RPST}	Read postamble		0.4	0.6	0.4	0.6	t_{CK}	
t_{DQSS}	CK to valid DQS-in		0.75	1.25	0.75	1.25	t_{CK}	
t_{WPRES}	DQS-in setup time		0	-	0	-	ns	3
t_{WPRE}	DQS write preamble		0.25	-	0.25	-	t_{CK}	
t_{WPST}	DQS write postamble		0.4	0.6	0.4	0.6	t_{CK}	
t_{DQSH}	DQS in high level pulse width		0.4	0.6	0.4	0.6	t_{CK}	
t_{DQSL}	DQS in low level pulse width		0.4	0.6	0.4	0.6	t_{CK}	
t_{IS}	Address and Control input setup time		1.1	-	1.3	-	ns	1
t_{IH}	Address and Control input hold time		1.1	-	1.3	-	ns	1
t_{DS}	DQ & DM setup time to DQS		0.6	-	0.8	-	ns	4, 5
t_{DH}	DQ & DM hold time to DQS		0.6	-	0.8	-	ns	4, 5
t_{HP}	Clock half period		t_{CLMIN} or t_{CHMIN}	-	t_{CLMIN} or t_{CHMIN}	-	ns	
t_{QH}	Output DQS valid window		t_{HP} – 0.65	-	t_{HP} – 0.75	-	ns	
t_{RC}	Row cycle time		60	-	67.5	-	ns	
t_{RFC}	Refresh row cycle time		110	-	110	-	ns	
t_{RAS}	Row active time		42	100K	45	100K	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay for Read or Write		18	-	22.5	-	ns	
t_{RP}	Row precharge time		18	-	22.5	-	ns	
t_{RRD}	Row active to Row active delay		12	-	15	-	ns	
t_{WR}	Write recovery time		12	-	15	-	ns	8
t_{DAL}	Auto precharge write recovery + Precharge		tWR+tRP	-	tWR+tRP	-	t_{CK}	
t_{WTR}	Internal Write to Read Delay		2	-	1	-	t_{CK}	7
t_{CCD}	Col. Address to Col. Address delay		1	-	1	-	t_{CK}	
t_{MRD}	Mode register set cycle time		2	-	2	-	t_{CK}	
t_{XSR}	Self refresh exit to next valid command delay		200	-	200	-	ns	
t_{XP}	Exit Power Down mode to first valid command		25	-	25	-	ns	6
t_{REFI}	Refresh interval time		-	7.8	-	7.8	µs	

Note:

1. Table 13.Input Setup / Hold Slew Rate Derating

Input Setup/Hold Slew Rate (V/ns)	$\triangle t_{IS}$ (ps)	$\triangle t_{IH}$ (ps)
1.0	0	0
0.8	+50	+50
0.6	+100	+100

This derating table is used to increase t_{IS} / t_{IH} in the case where the input slew rate is below 1.0V/ns.

2. Driver Strength should be selected based on actual system loading conditions. Figure 3, the AC Output Load Circuit, represents the reference load used in defining the relevant timing parameters of this device.The 20pF load capacitance is not expected to be a precise representation of either a typical system load or the production test environment but is appropriate for Full Driver Strength. Setting the output drivers to 1/2 Driver Strength, for a further example, is appropriate for a 10pF load.

3. The specific requirement is that DQS be Valid (High or Low) on or before this CK edge. The case shown (DQS going from High-Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on t_{DQSS}.

4. Table 14. I/O Setup / Hold Slew Rate Derating

I/O Setup/Hold Slew Rate (V/ns)	$\triangle t_{DS}$ (ps)	$\triangle t_{DH}$ (ps)
1.0	0	0
0.8	+75	+75
0.6	+150	+150

This derating table is used to increase t_{DS} / t_{DH} in the case where the I/O slew rate is below 1.0V/ns

5. Table 15. I/O Delta Rise / Fall Derating

I/O Delta Rise / Fall Rate (ns/V)	$\triangle t_{DS}$ (ps)	$\triangle t_{DH}$ (ps)
1.0	0	0
±0.25	+50	+50
±0.50	+100	+100

This derating table is used to increase t_{DS}/t_{DH} in the case where the DQ and DQS slew rates differ. The Delta Rise / Fall Rate is calculated as 1/SlewRate1-1/SlewRate2. For example, if SlewRate1 = 1.0V/ns and SlewRate2 = 0.8V/ns, then the Delta Rise / Fall Rate = -0.25ns/V.

6. There must be at least one clock (CK) pulse during the t_{XP} period.

7. t_{WTR} is referenced from the positive clock edge after the last Data In pair.

8. t_{WR} is referenced from the positive clock edge after the last desired Data In pair.

Table 16. Recommended A.C. Operating Conditions (V_{DD}=1.7V~1.95V, T_A =-25~85°C)

Parameter	Symbol	Min.	Max.	Unit	Note
Input High Voltage (AC)	V_{IH} (AC)	0.8 x V_{DDQ}	V_{DDQ}+0.3	V	1
Input Low Voltage (AC)	V_{IL} (AC)	-0.3	0.2 x V_{DDQ}	V	1
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	V_{IX} (AC)	0.4 x V_{DDQ}	0.6 x V_{DDQ}	V	2

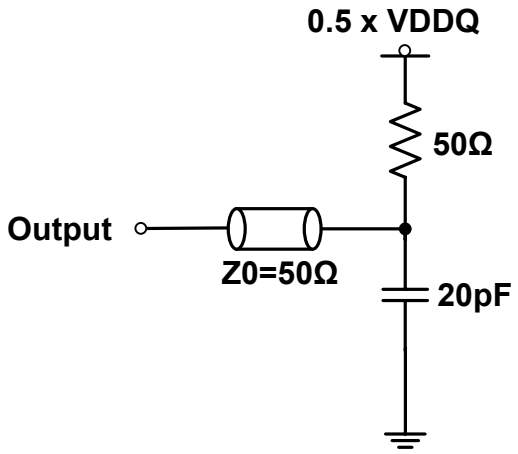
Note:

1. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation.
2. The value of V_{IX} is expected to equal 0.5 x V_{DDQ} of the transmitting device and must track variation in the DC level of the same.

Table 17. LVCMOS Interface

Reference Level of Output Signals	0.5 x V_{DDQ}
Output Load	Reference to the Test Load
Input Signal Levels (V_{IH}/ V_{IL})	0.8 x V_{DDQ} / 0.2 x V_{DDQ}
Input Signals Slew Rate	1 V/ns
Reference Level of Input Signals	0.5 x V_{DDQ}

Figure 4. LVCMOS A.C. Test Load



Timing Waveforms

Figure 5. Initialization Waveform Sequence

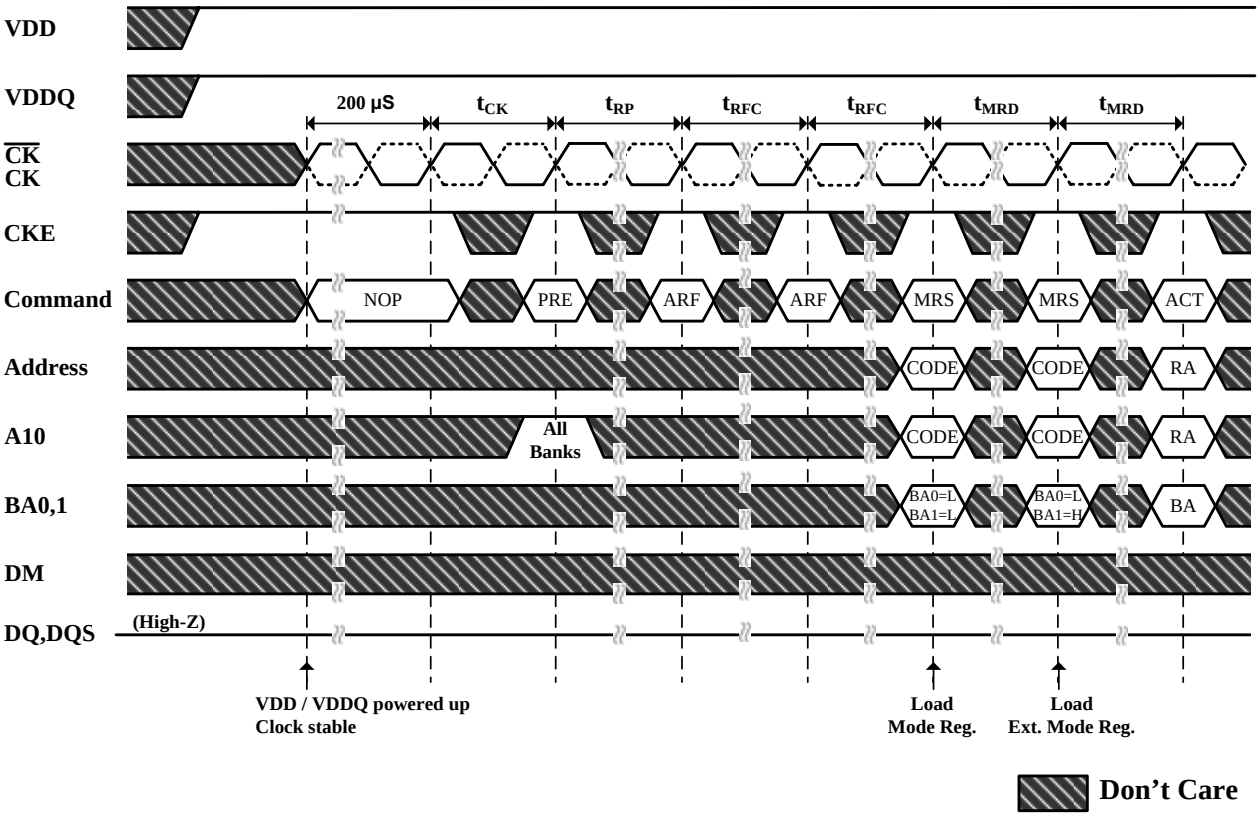
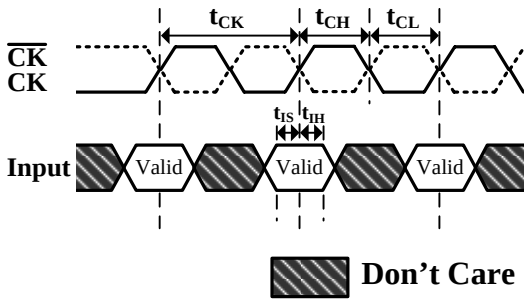


Figure 6. Basic Timing Parameters for Commands



Notes: Input = A0 - A12, BA0,BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$;

Figure 7. NOP Command

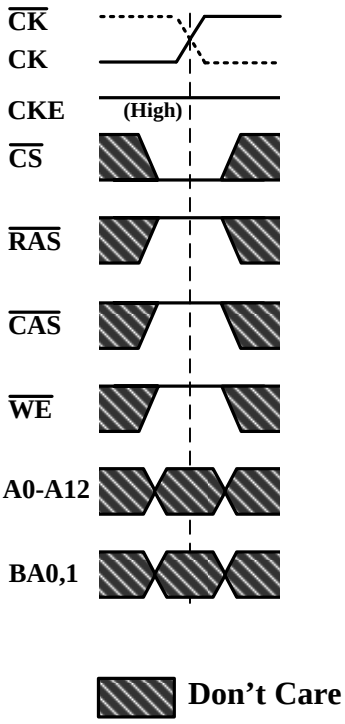


Figure 8. Mode Register Set Command

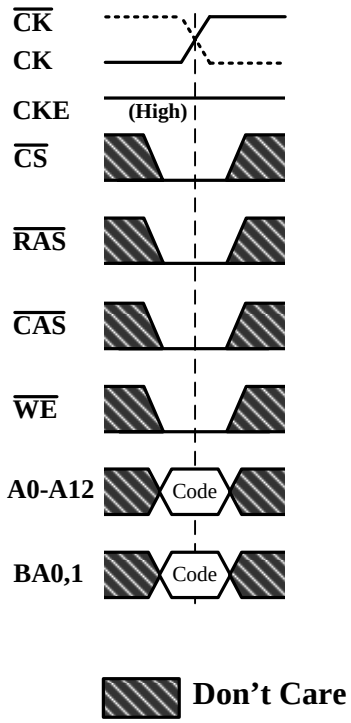
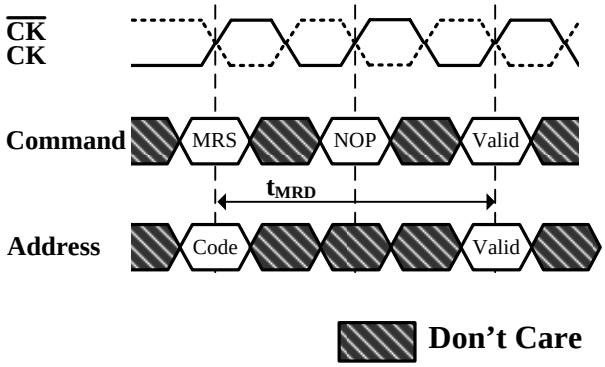


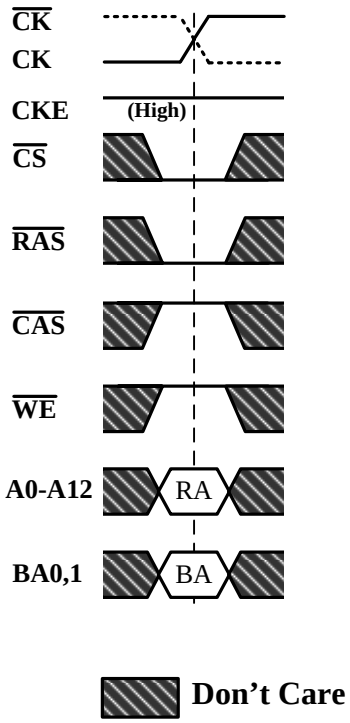
Figure 9. Mode Register Set Command Timing



Notes: Code = Mode Register / Extended Mode Register selection (BA0, BA1) and op-code (A0- A12)

.

Figure 10. Active Command



BA = Bank Address
RA = Row Address

Figure 11. Bank Activation Command Cycle

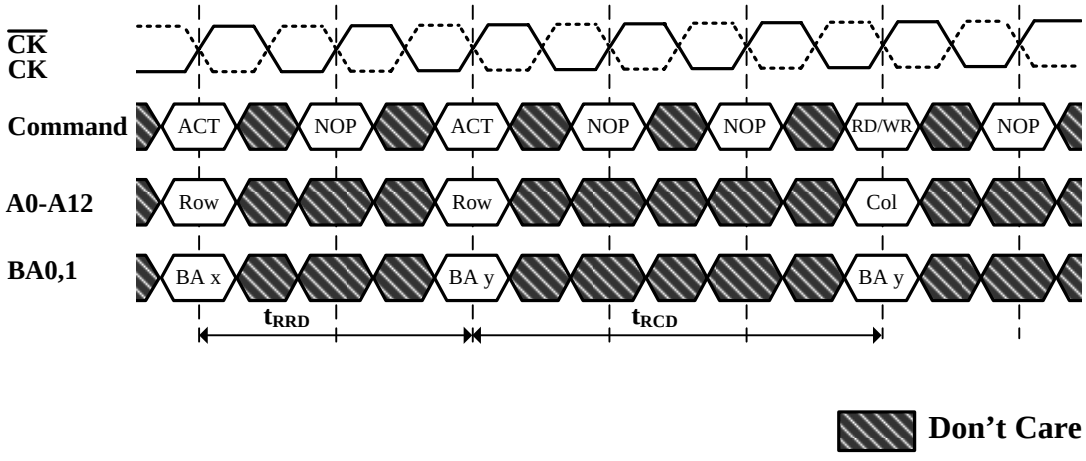
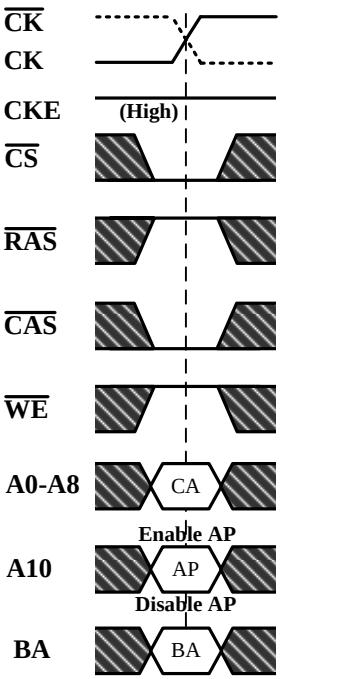


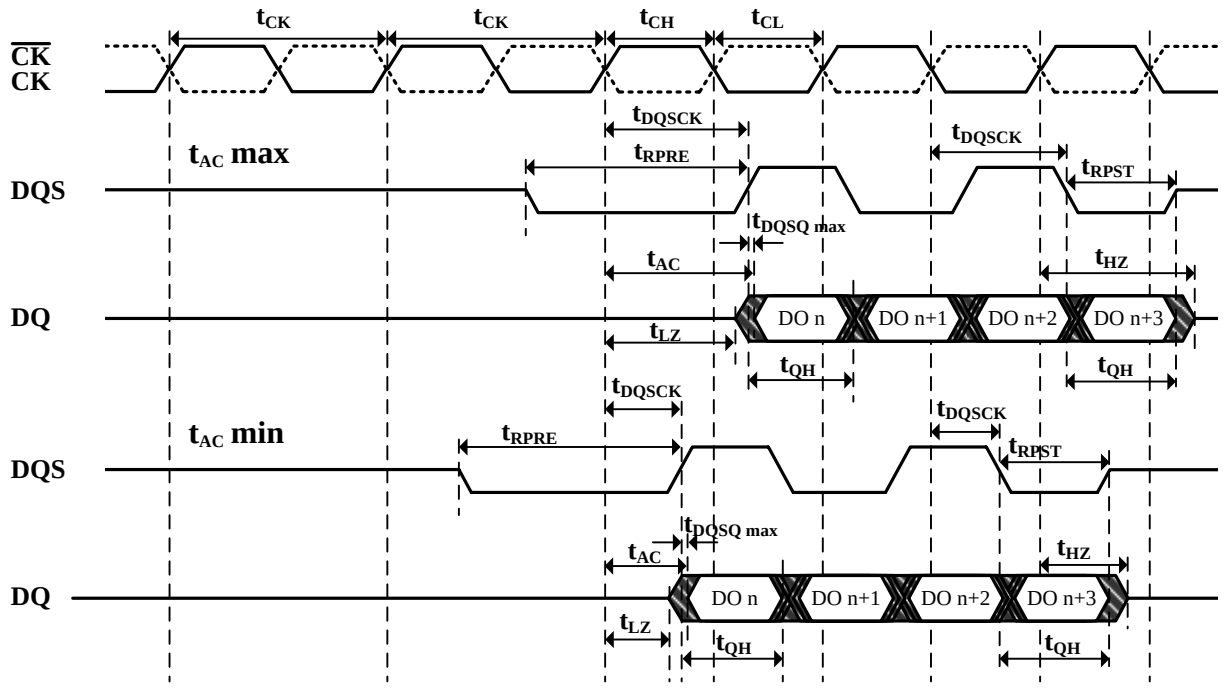
Figure 12. Read Command



Don't Care

BA = Bank Address
CA = Column Address
AP = Auto Precharge

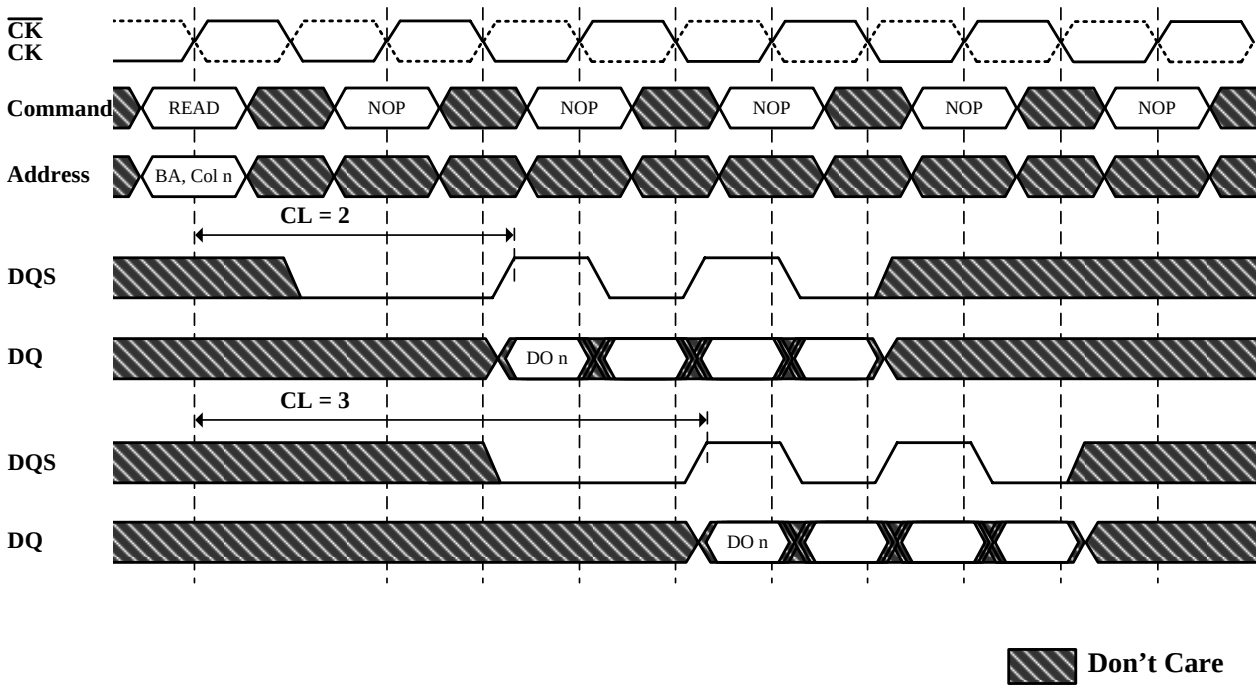
Figure 13. Basic Read Timing Parameters



(1) DO n = Data Out from column n
(2) All DQ are valid tAC after the CK edge.
All DQ are valid tDQSQ after the DQS edge, regardless of tAC

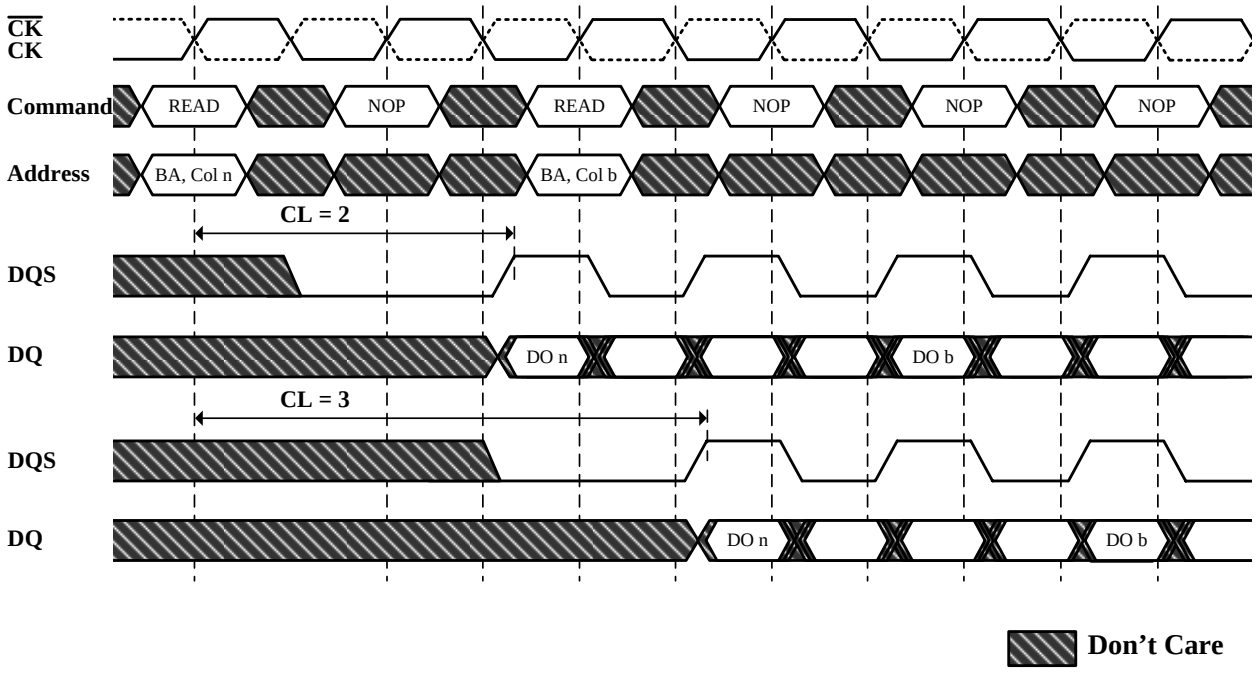
Don't Care

Figure 14. Read Burst Showing $\overline{CAS}$ Latency



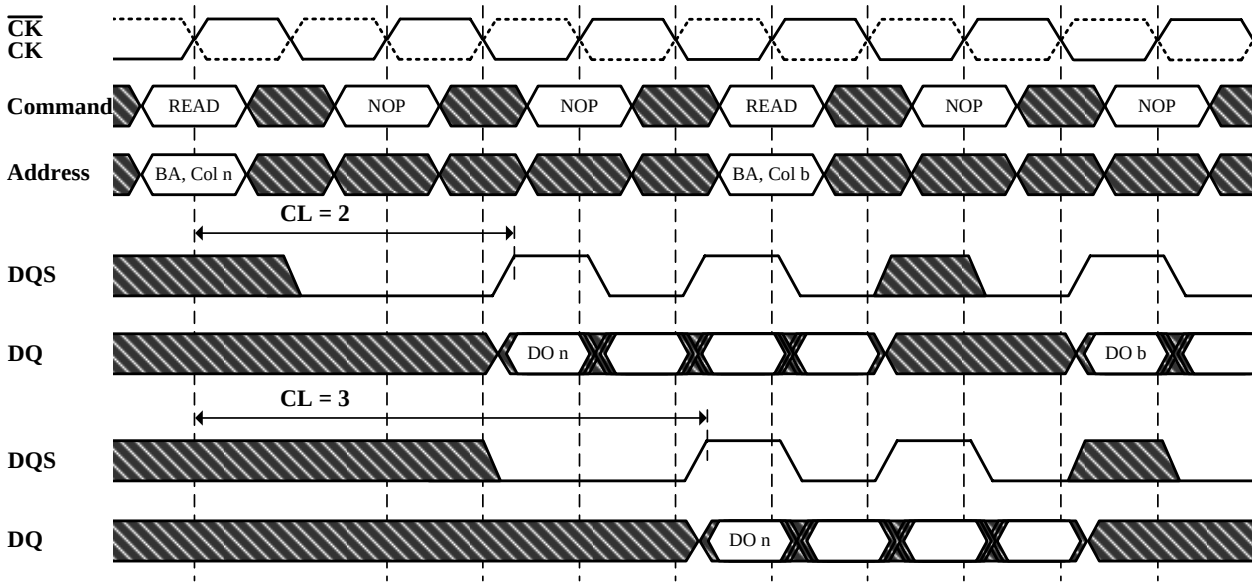
(1) DO n = Data Out from column n
(2) BA, Col n = Bank A, Column n
(3) Burst Length = 4; 3 subsequent elements of Data Out appear in the programmed order following DO n
(4) Shown with nominal tAC, tDQSCK and tDQSQ

Figure 15. Consecutive Read Bursts



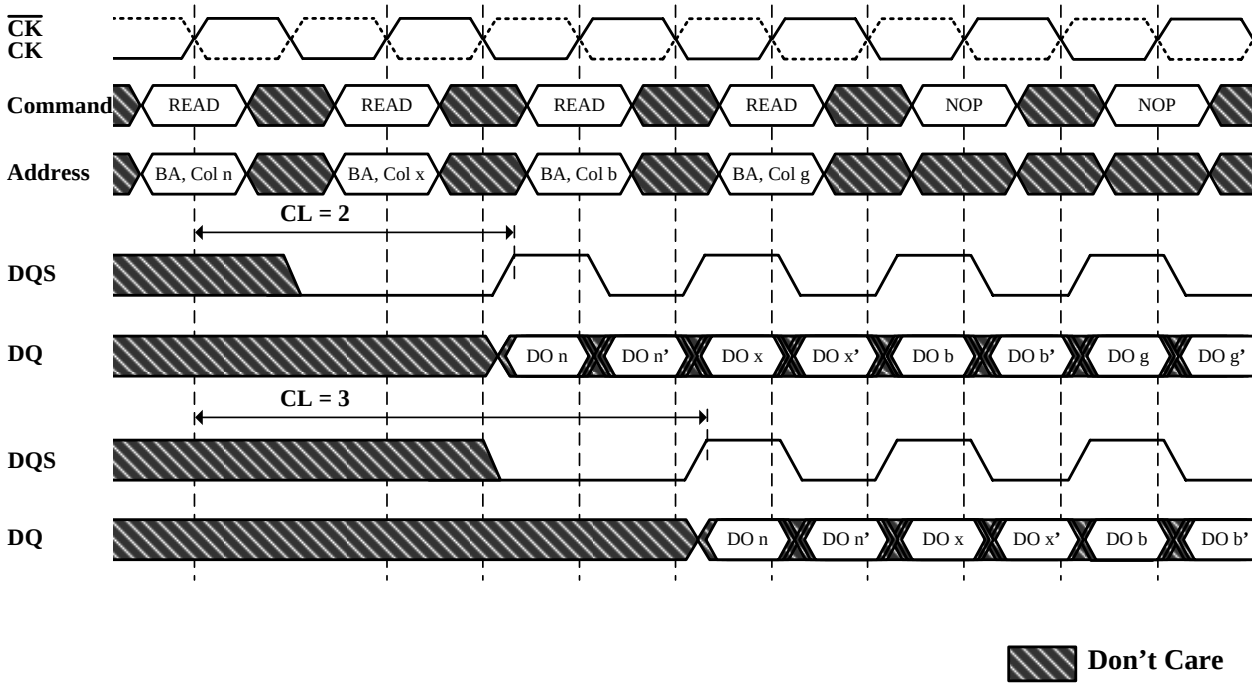
(1) DO n (or b) = Data Out from column n (or column b)
(2) Burst Length = 4,8 or 16 (if 4, the bursts are concatenated; if 8 or 16, the second burst interrupts the first)
(3) Read bursts are to an active row in any bank
(4) Shown with nominal tAC, tDQSCK and tDQSQ

Figure 16. Non-Consecutive Read Bursts



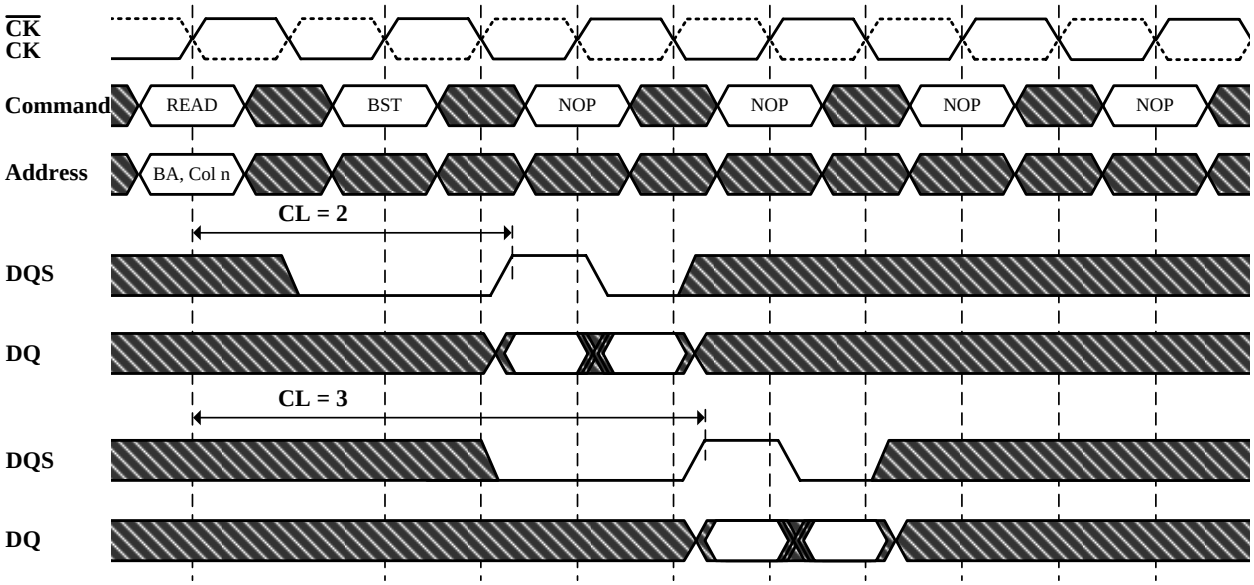
(1) DO n (or b) = Data Out from column n (or column b)
(2) BA Col n (b) = Bank A, Column n (b)
(3) Burst Length = 4; 3 subsequent elements of Data Out appear in the programmed order following DO n (b)
(4) Shown with nominal tAC, tDQSCK and tDQSQ

Figure 17. Random Read Bursts



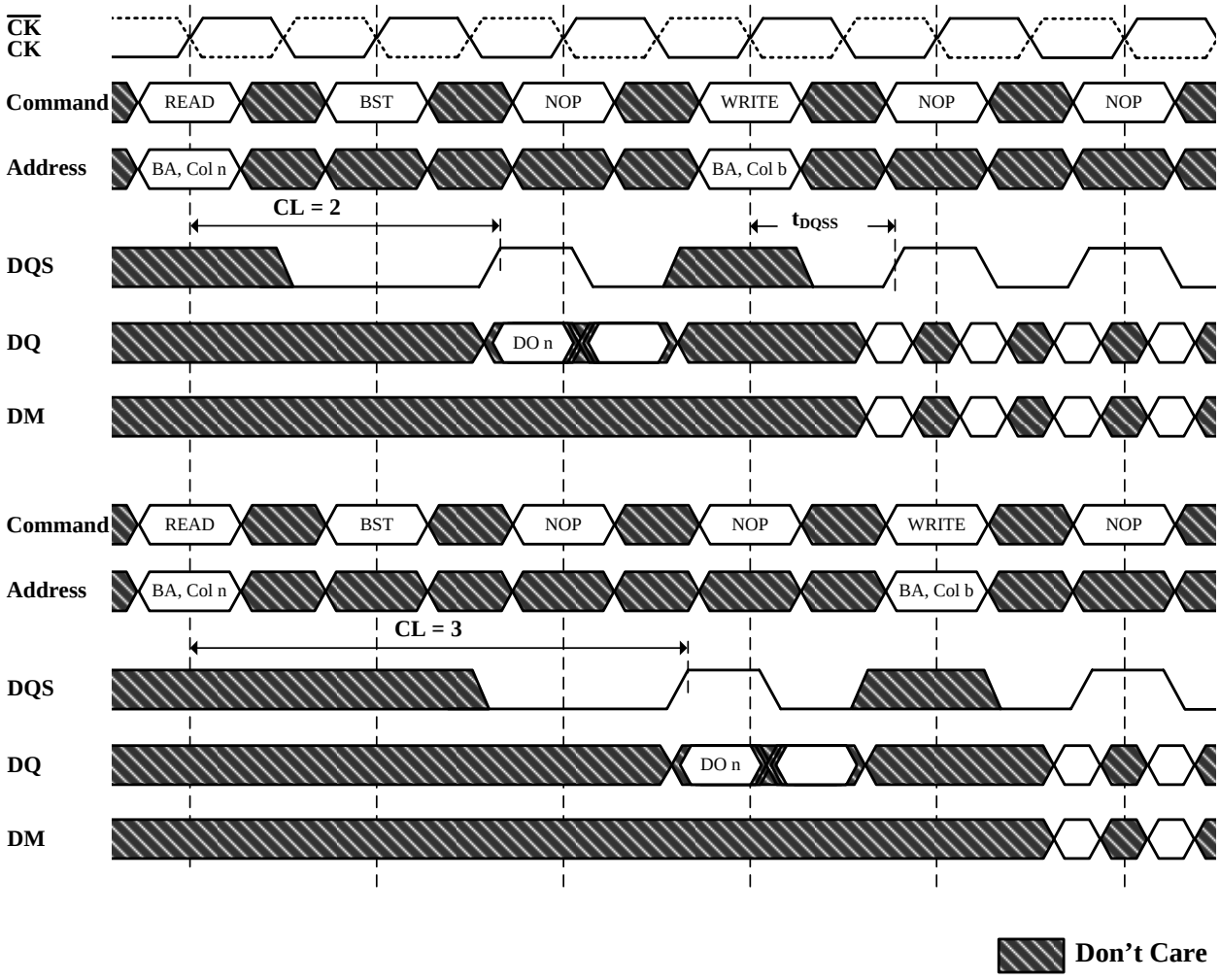
(1) DO n, etc. = Data Out from column n, etc.
n', x', etc. = Data Out elements, according to the programmed burst order
(2) BA, Col n = Bank A, Column n
(3) Burst Length = 2, 4, 8 or 16 in cases shown (if burst of 4, 8 or 16, the burst is interrupted)
(4) Reads are to active rows in any banks

Figure 18. Terminating a Read Burst



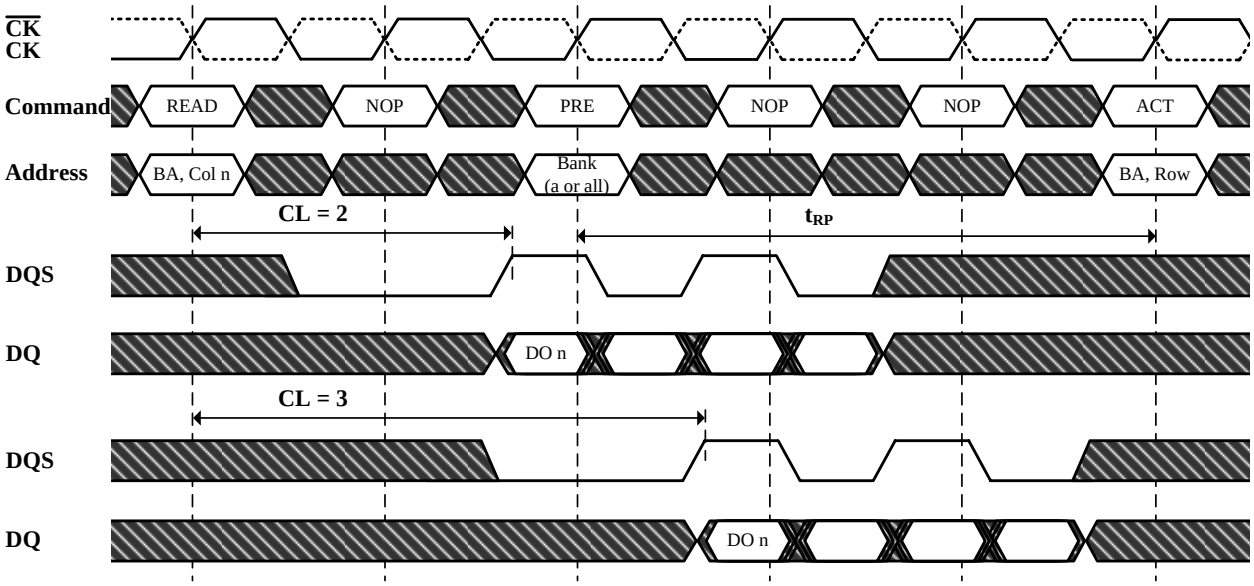
(1) DO n = Data Out from column n
(2) BA Col n = Bank A, Column n
(3) Cases shown are bursts of 4, 8 or 16 teminated after 2 data elements.
(4) Shown with nominal tAC, tDQSCK and tDQSQ

Figure 19. Read to Write



(1) DO n = Data Out from column n; DI b = Data In to column b
(2) Burst length = 4, 8 or 16 in the cases shown; if the burst length is 2, the BST command can be ommitted
(3) Shown with nominal tAC, tDQSCK and tDQSQ

Figure 20. Read to precharge



(1) DO n = Data Out from column n
(2) Cases shown are either uninterrupted burst of 4, or interrupted bursts of 8.
(3) Shown with nominal tAC, tDQSCK and tDQSQ.
(4) Precharge may be applied at (BL/2) tCK after the READ command.
(5) Note that Precharge may not be issued before tRAS ns after the ACTIVE command for applicable banks.
(6) The ACTIVE command may be applied if tRC has been met.

Figure 21. Burst Terminate Command

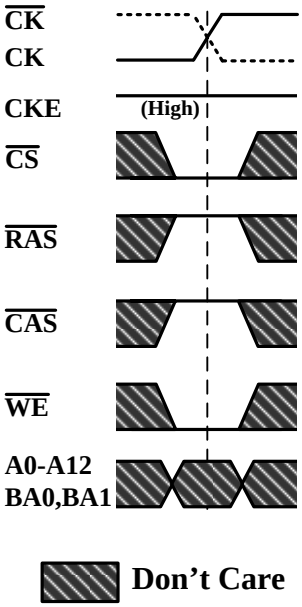
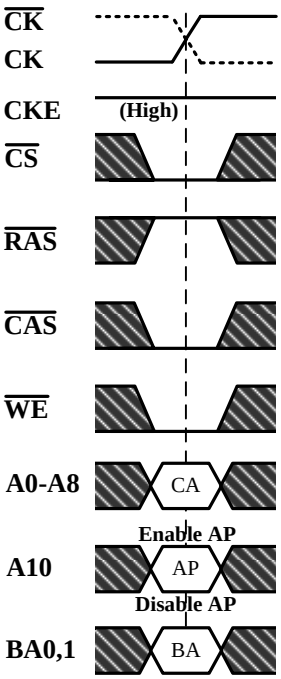


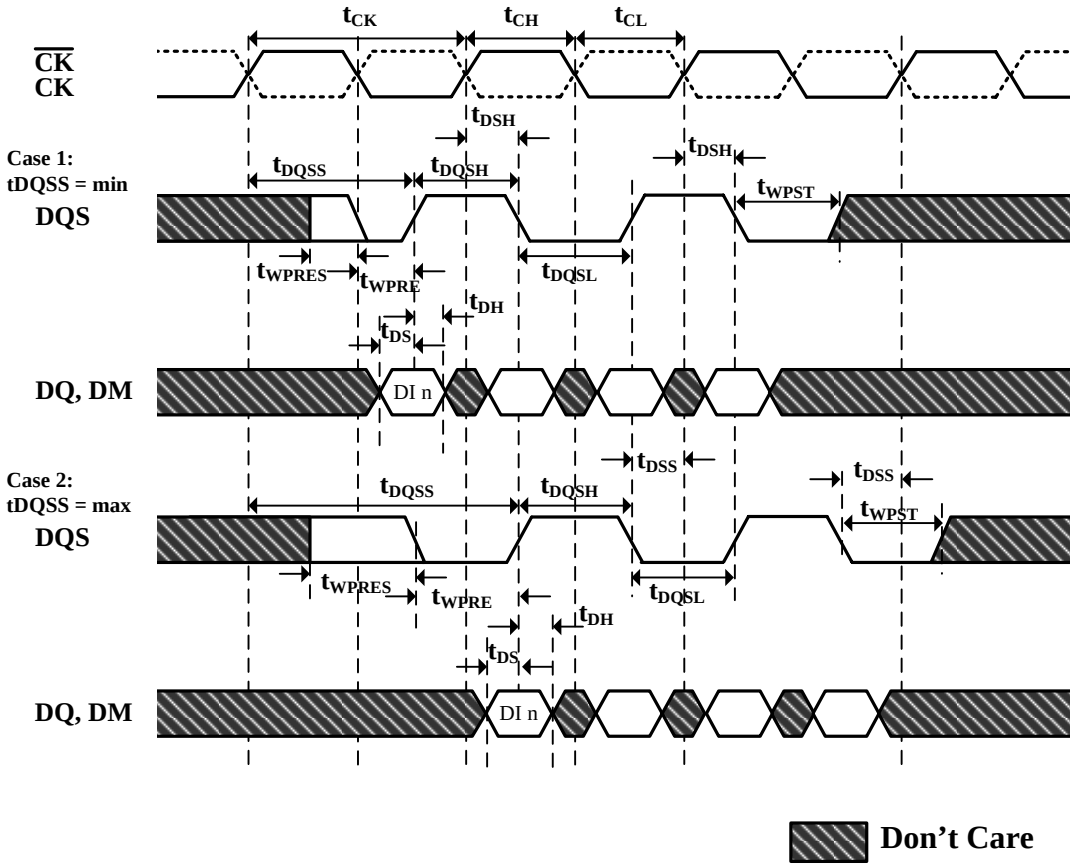
Figure 22. Write Command



Don't Care

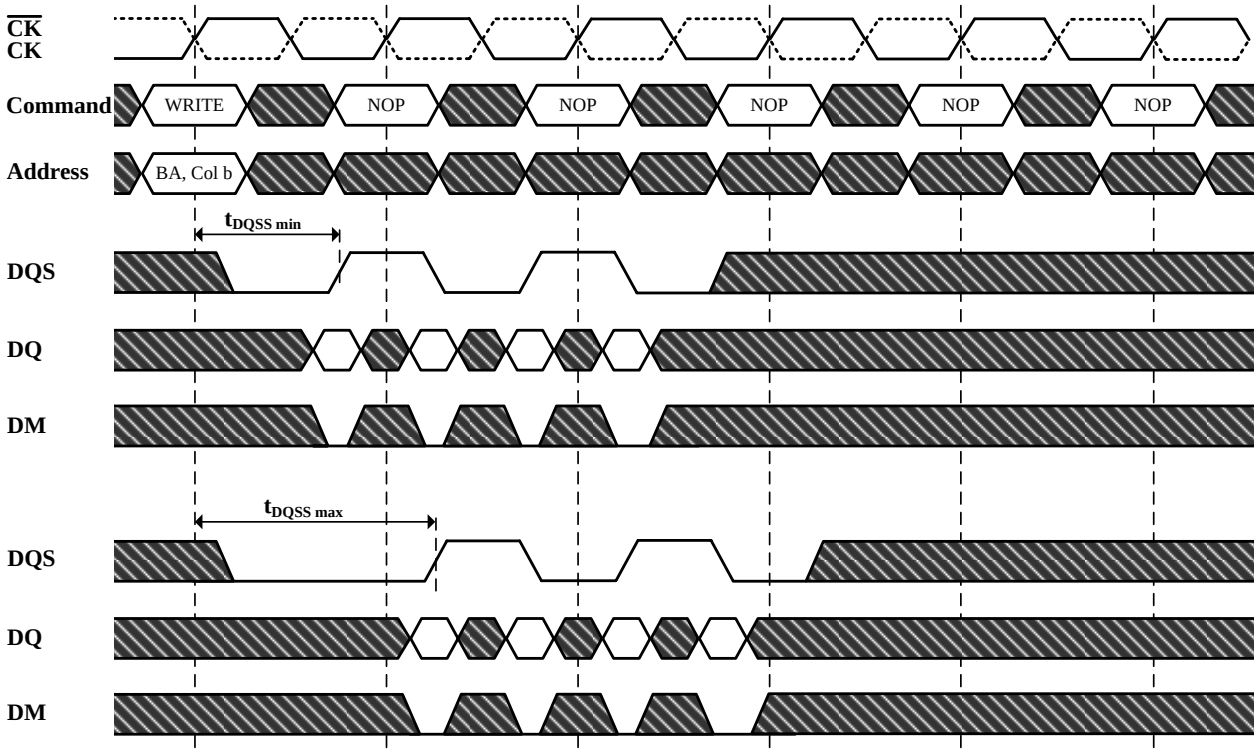
BA = Bank Address
CA = Column Address
AP = Auto Precharge

Figure 23. Basic Write Timing Parameters



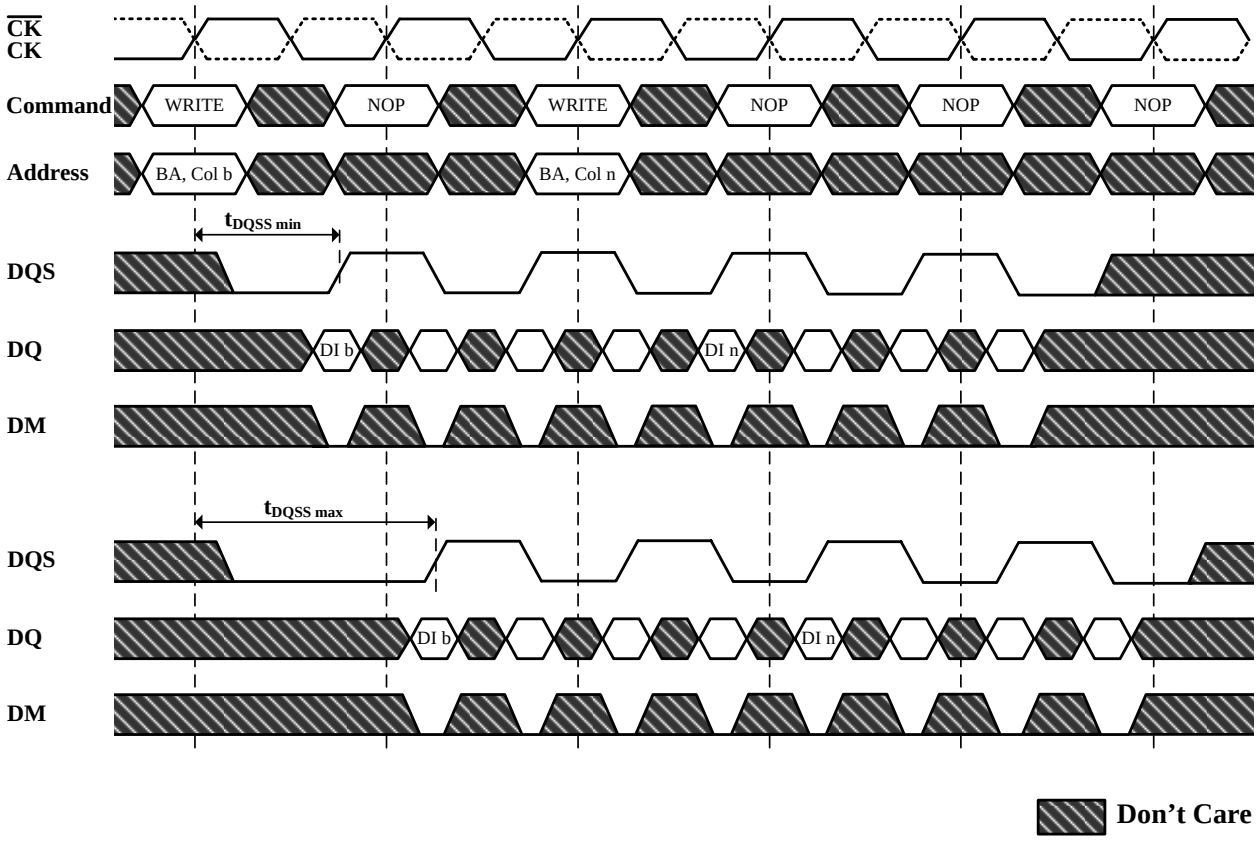
(1) DI n = Data In for column n
(2) 3 subsequent elements of Data In are applied in the programmed order following DI n.
(3) tDQSS: each rising edge of DQS must fall within the ±25% window of the corresponding positive clock edge.

Figure 24. Write Burst (min. and max. t_{DQSS})



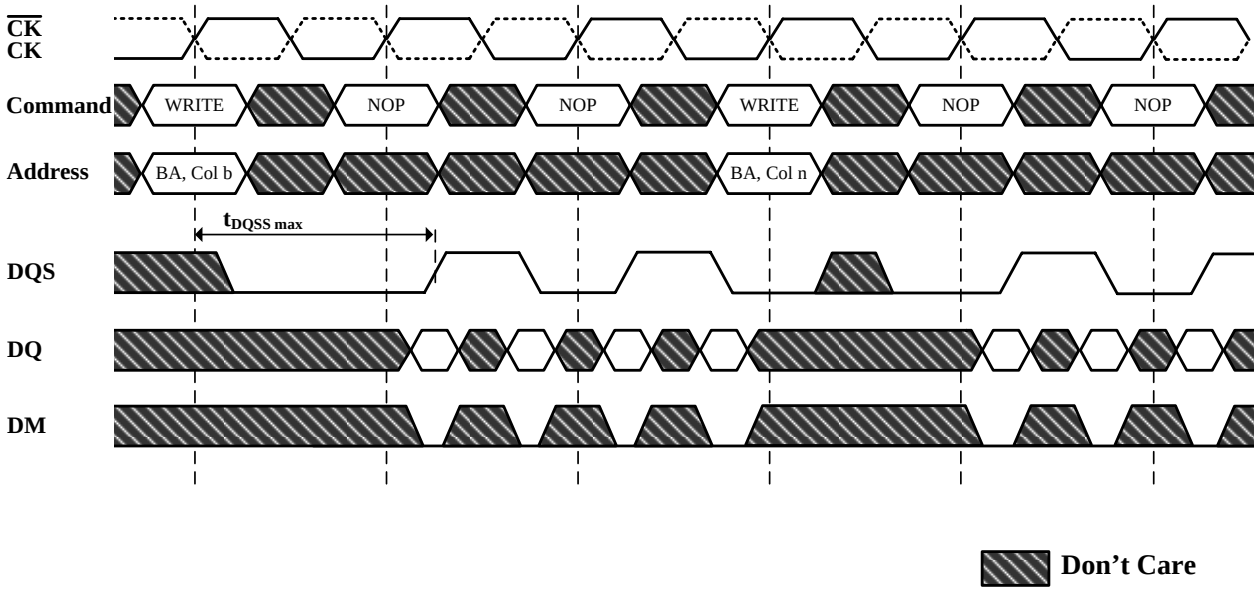
(1) DI b = Data In to column b.
(2) 3 subsequent elements of Data In are applied in the programmed order following DI b.
(3) A non-interrupted burst of 4 is shown.
(4) A10 is LOW with the WRITE command (Auto Precharge is disabled)

Figure 25. Concatenated Write Bursts



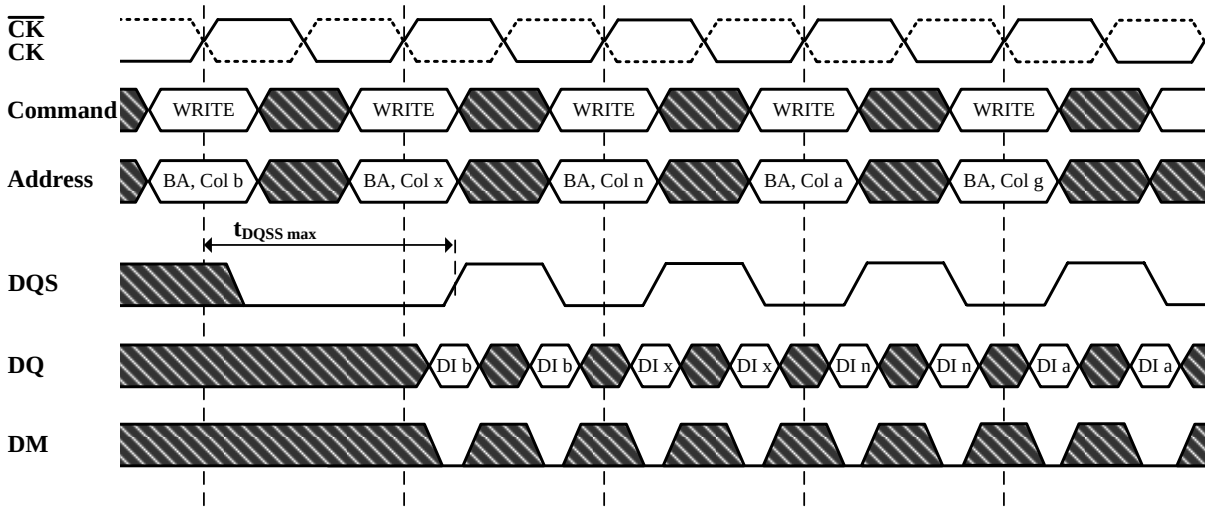
(1) DI b (n) = Data In to column b (column n).
(2) 3 subsequent elements of Data In are applied in the programmed order following DI b.
3 subsequent elements of Data In are applied in the programmed order following DI n.
(3) Non-interrupted bursts of 4 are shown.
(4) Each WRITE command may be to any active bank

Figure 26. Non-Concatenated Write Bursts



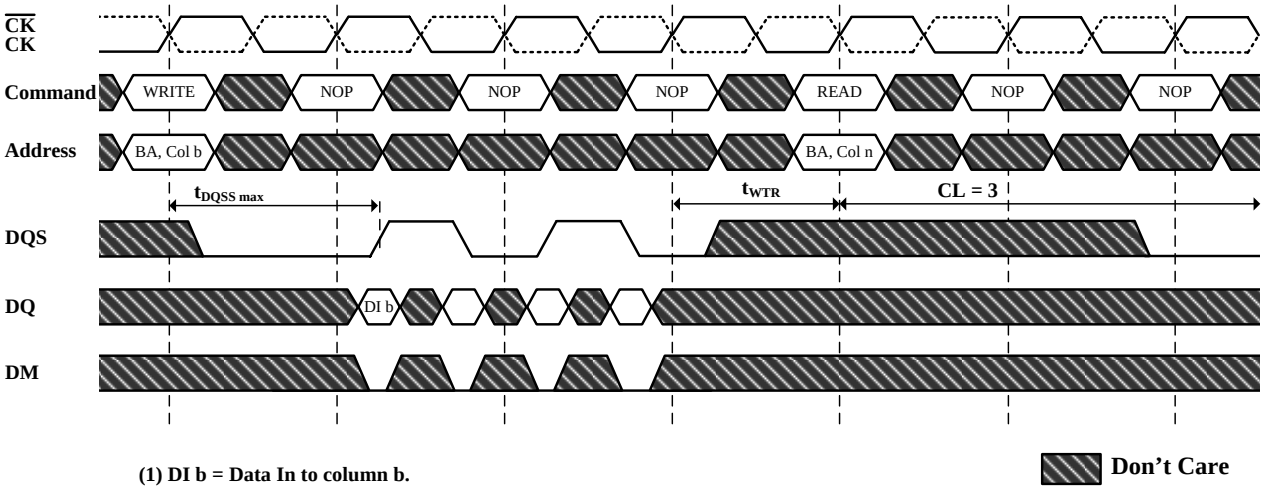
(1) DI b (n) = Data In to column b (or column n).
(2) 3 subsequent elements of Data In are applied in the programmed order following DI b.
3 subsequent elements of Data In are applied in the programmed order following DI n.
(3) Non-interrupted bursts of 4 are shown.
(4) Each WRITE command may be to any active bank and may be to the same or different devices

Figure 27. Random Write Cycles



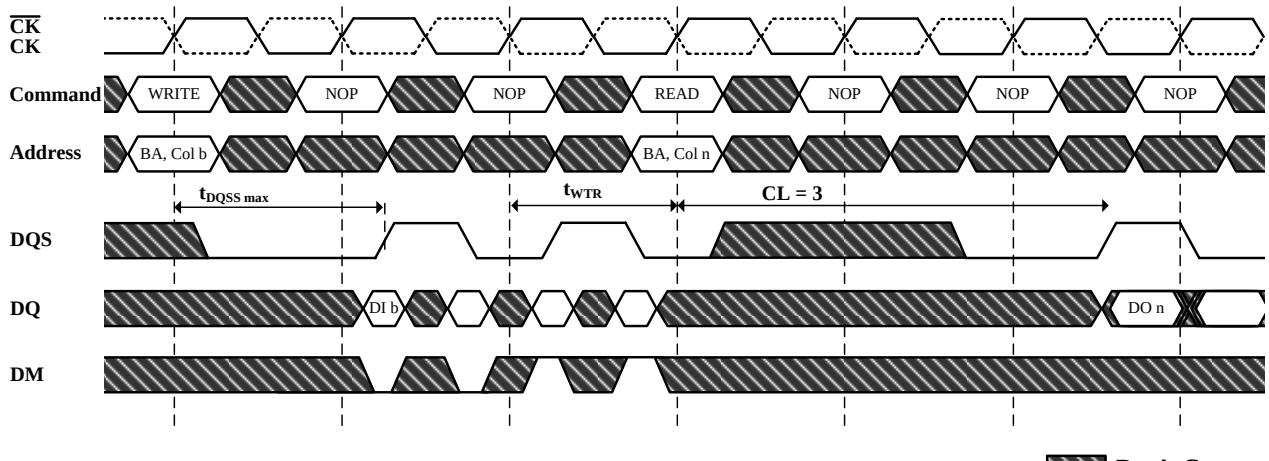
(1) DI b etc. = Data In to column b, etc. ;
b', etc. = the next Data In following DI b, etc. according to the programmed burst order
(2) Programmed burst length = 2, 4, 8 or 16 in cases shown. If burst of 4, 8 or 16, burst would be truncated.
(3) Each WRITE command may be to any active bank and may be to the same or different devices.

Figure 28. Non-Interrupting Write to Read



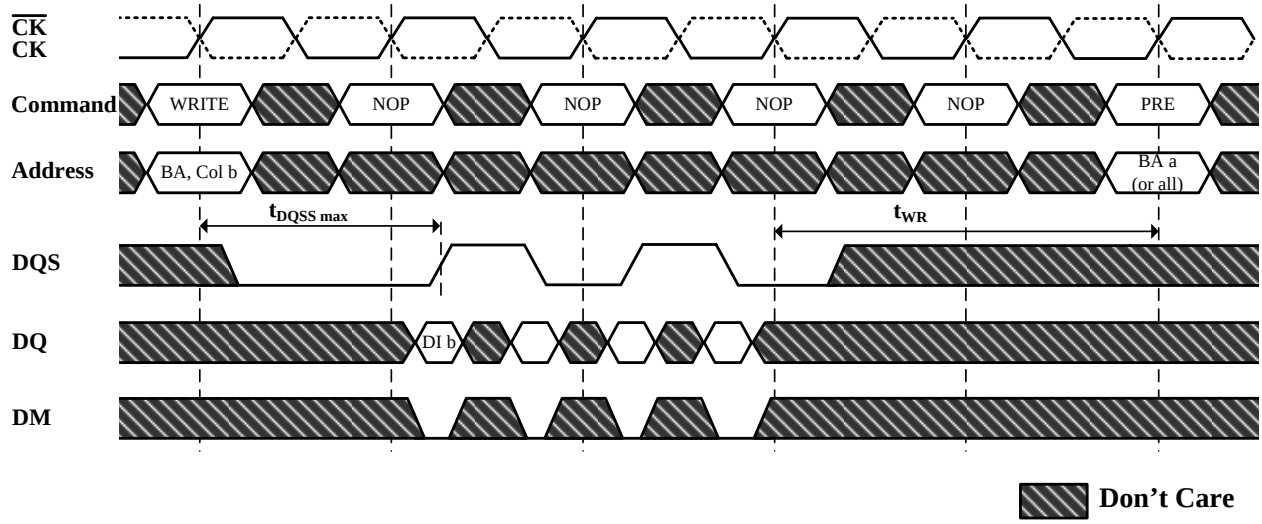
(1) DI b = Data In to column b.
3 subsequent elements of Data In are applied in the programmed order following DI b.
(2) A non-interrupted burst of 4 is shown.
(3) tWTR is referenced from the positive clock edge after the last Data In pair.
(4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
(5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

Figure 29. Interrupting Write to Read



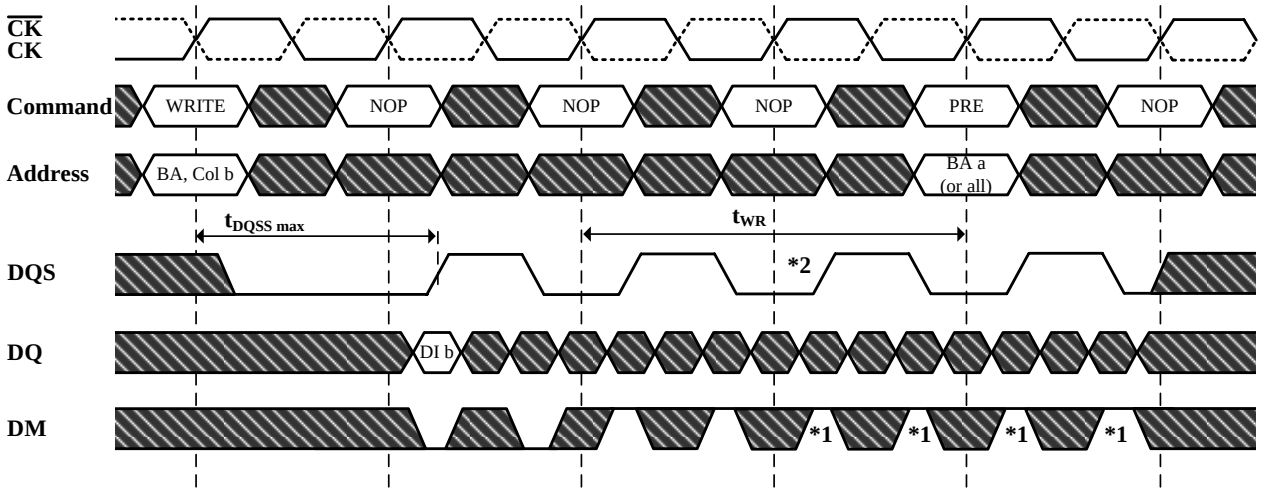
(1) DI b = Data In to column b. DO n = Data Out from column n.
(2) An interrupted burst of 4 is shown, 2 data elements are written.
3 subsequent elements of Data In are applied in the programmed order following DI b.
(3) tWTR is referenced from the positive clock edge after the last Data In pair.
(4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
(5) The READ and WRITE commands are to the same device but not necessarily to the same bank.

Figure 30. Non Interrupting Write to Precharge



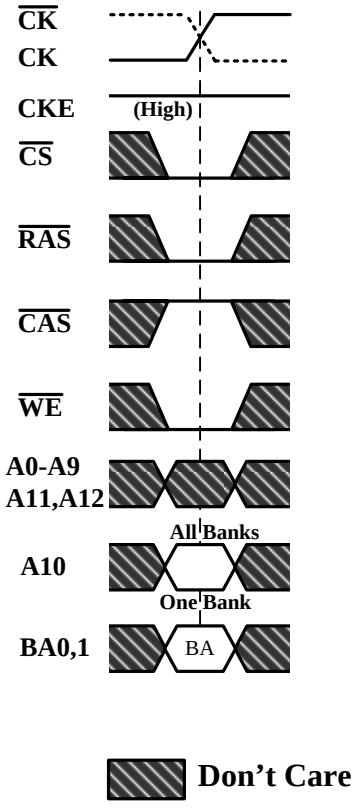
(1) DI b = Data In to column b.
3 subsequent elements of Data In are applied in the programmed order following DI b.
(2) A non-interrupted burst of 4 is shown.
(3) tWR is referenced from the positive clock edge after the last Data in pair.
(4) A10 is LOW with the WRITE command (Auto Precharge is disabled)

Figure 31. Interrupting Write to Precharge



(1) DI b = Data In to column b.
(2) An interrupted burst of 4 or 8 is shown, 2 data elements are written.
(3) tWTR is referenced from the positive clock edge after the last desired Data in pair.
(4) A10 is LOW with the WRITE command (Auto Precharge is disabled)
(5) *1 = can be Don't Care for programmed burst length of 4
(6) *2 = for programmed burst length of 4, DQS becomes Don't Care at this point

Figure 32. Precharge Command



BA = Bank Address
(if A10 = L, otherwise Don't Care)

Figure 33. Auto Refresh Command

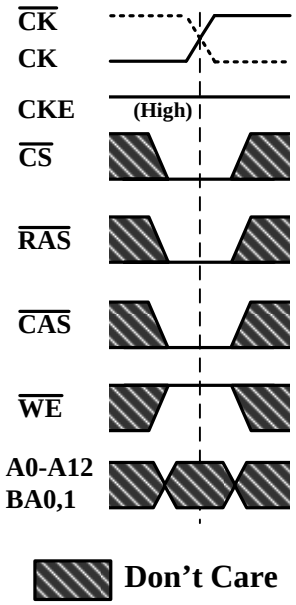


Figure 34. Self Refresh Command

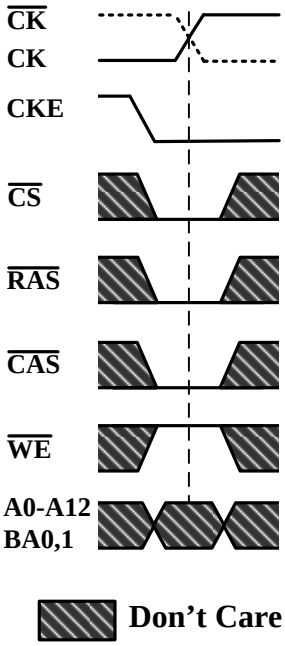


Figure 35. Auto Refresh Cycles Back-to-Back

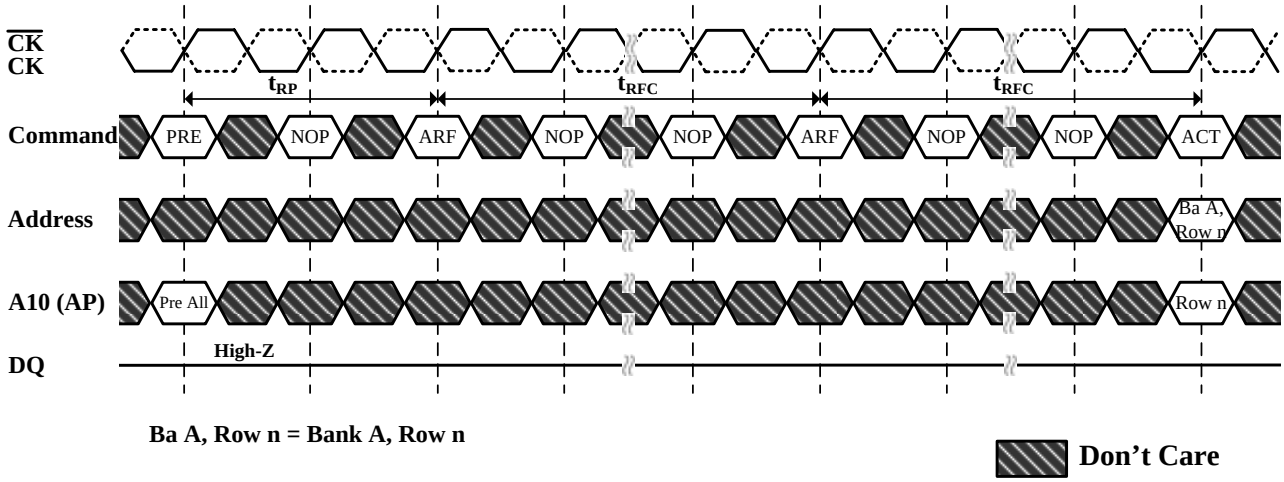


Figure 36. Self Refresh Entry and Exit

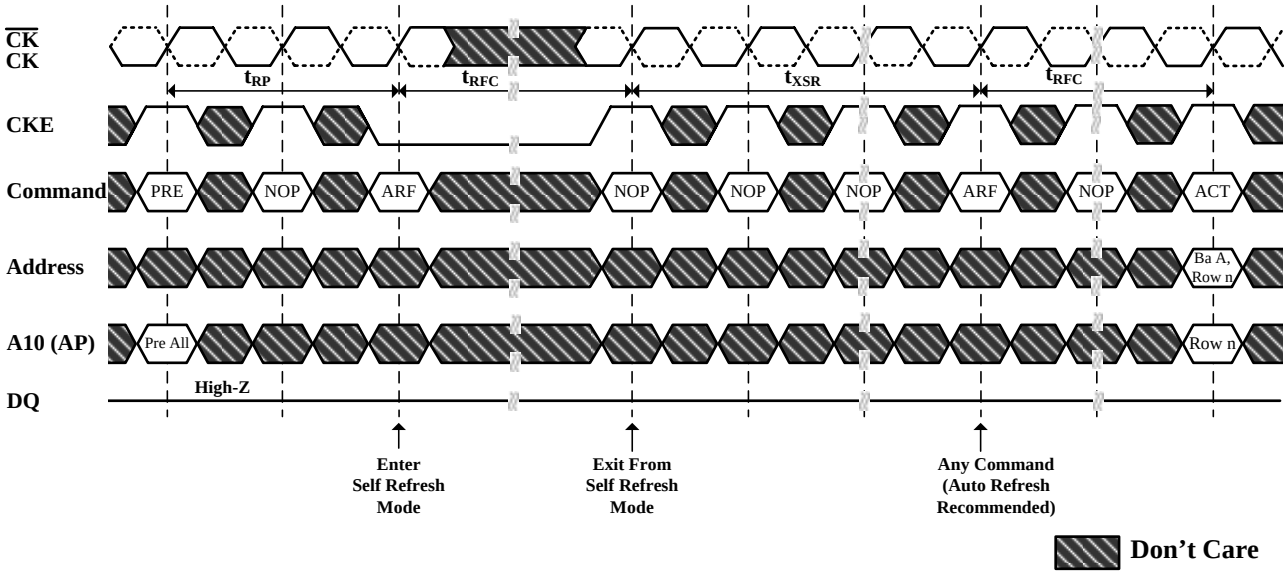
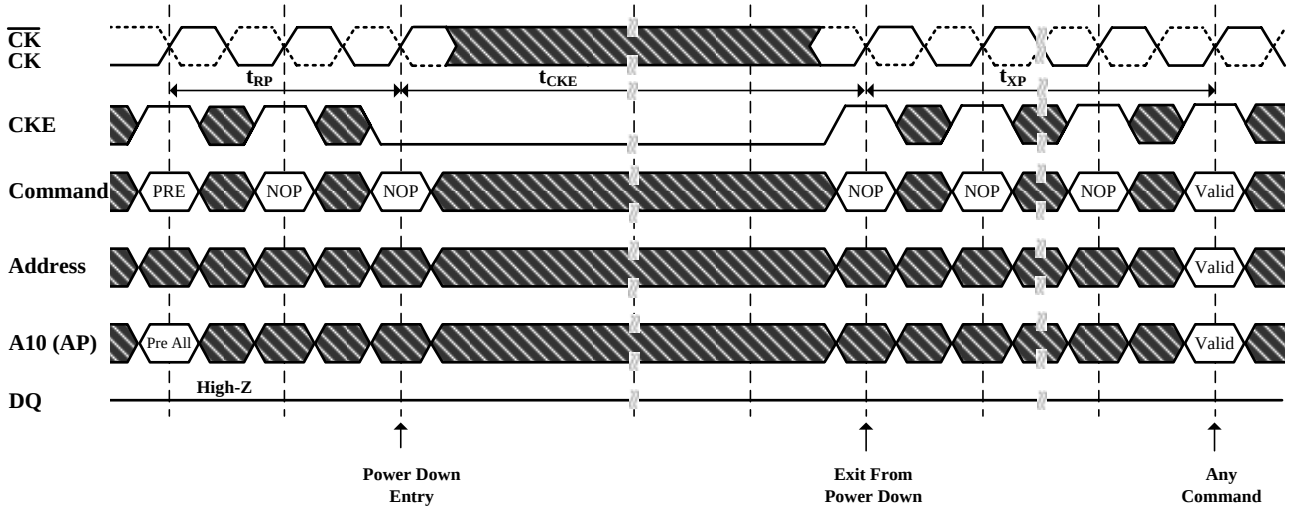


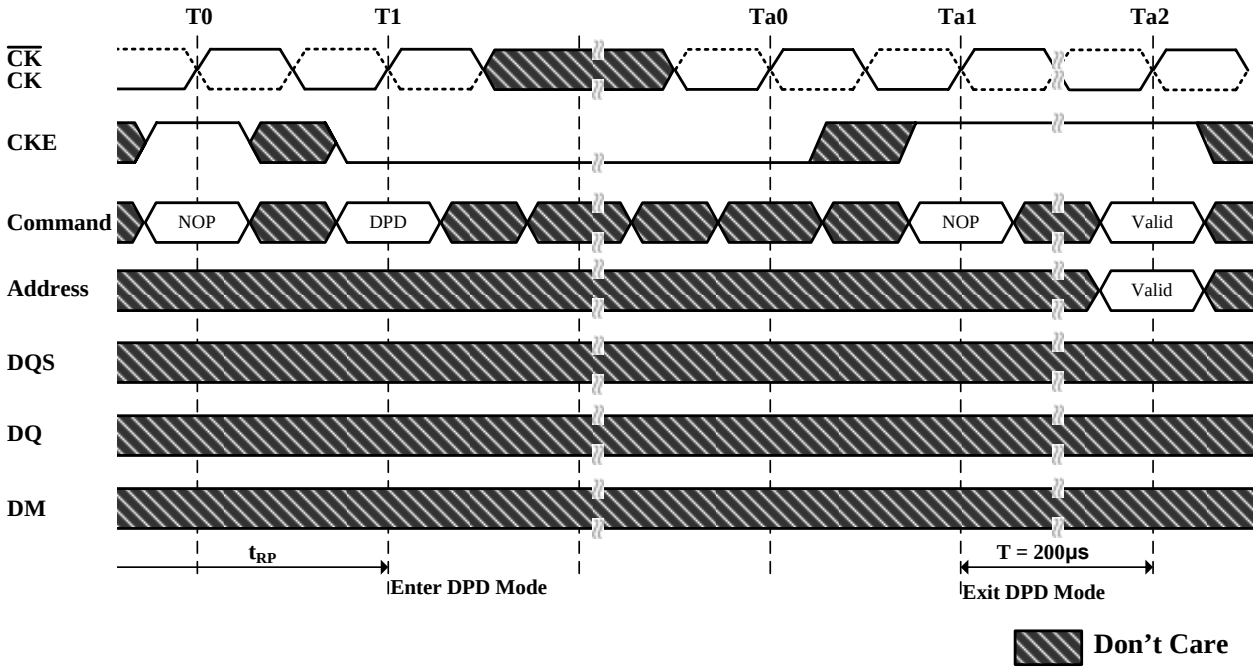
Figure 37. Power-Down Entry and Exit



Precharge Power-Down mode shown: all banks are idle and tRP is met when Power-Down Entry command is issued

Don't Care

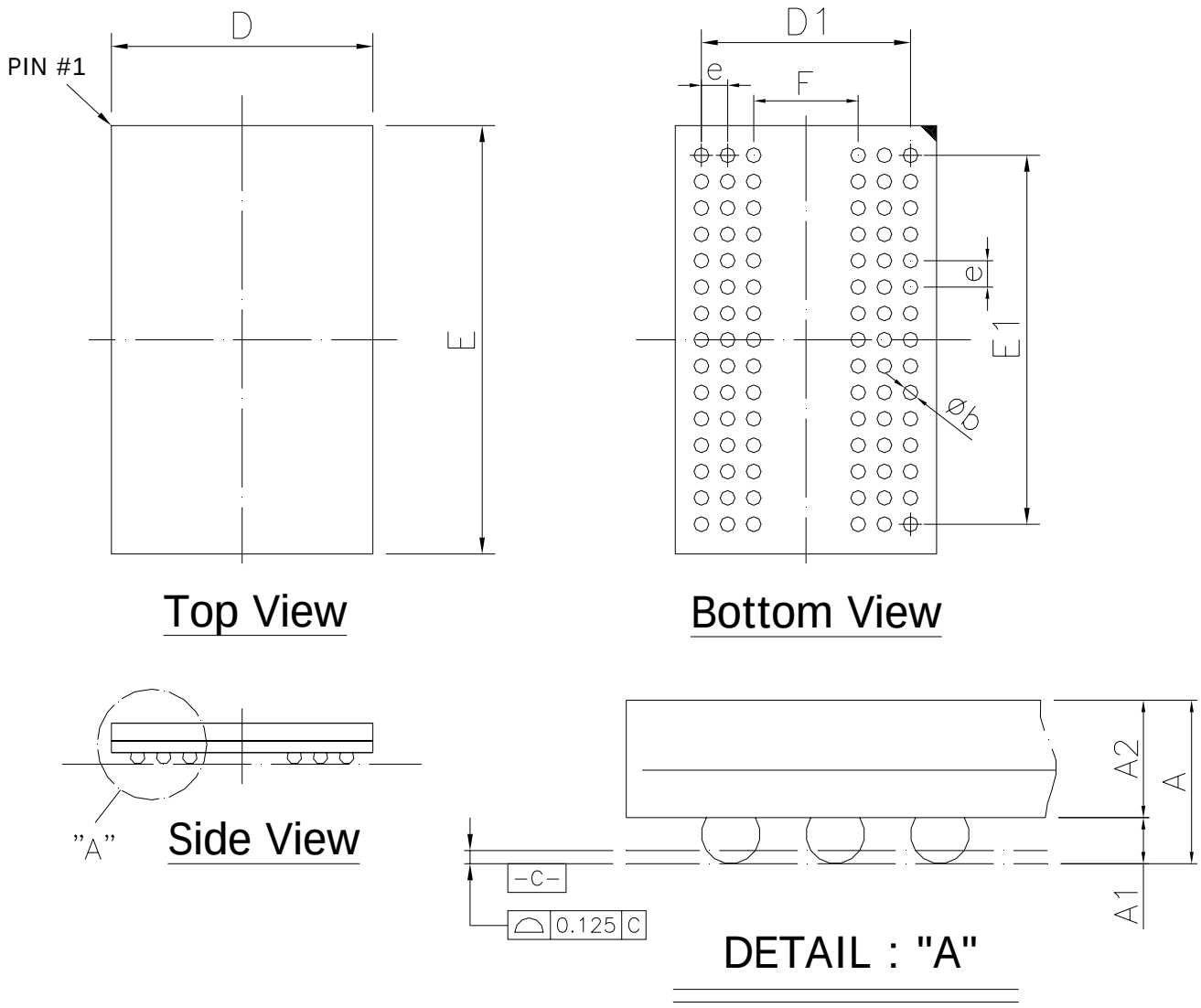
Figure 38. Deep Power-Down Entry and Exit



Don't Care

(1) Clock must be stable before exiting Deep Power-Down mode. That is, the clock must be cycling within specifications by Ta0
(2) Device must be in the all banks idle state prior to entering Deep Power-Down mode
(3) 200µs is required before any command can be applied upon exiting Deep Power-Down mode
(4) Upon exiting Deep Power-Down mode a PRECHARGE ALL command must be issued, followed by two AUTO REFRESH commands and a load mode register sequence

Figure 39. VFBGA 90ball 8x13x1.0mm(max)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	--	--	0.039	--	--	1.0
A1	0.012	0.014	0.016	0.30	0.35	0.40
A2	0.022	0.023	0.024	0.54	0.58	0.62
D	0.311	0.315	0.319	7.90	8.00	8.10
E	0.508	0.512	0.516	12.90	13.00	13.10
D1	--	0.252	--	--	6.40	--
E1	--	0.441	--	--	11.2	--
e	--	0.031	--	--	0.80	--
b	0.016	0.018	0.020	0.40	0.45	0.50
F	--	0.126	--	--	3.2	--