ELPIDA

PRELIMINARY DATA SHEET

256M bits DDR SDRAM

EDD2508AMTA (32M words × 8 bits)
EDD2516AMTA (16M words × 16 bits)

Description

The EDD2508AM is a 256M bits Double Data Rate (DDR) SDRAM organized as 8,388,608 words × 8 bits × 4 banks. The EDD2516AM is a 256M bits DDR SDRAM organized as 4,194,304 words × 16 bits × 4 banks. Read and write operations are performed at the cross points of the CK and the /CK. This high-speed data transfer is realized by the 2 bits prefetch-pipelined architecture. Data strobe (DQS) both for read and write are available for high speed and reliable data bus design. By setting extended mode resister, the on-chip Delay Locked Loop (DLL) can be set enable or disable. They are packaged in standard 66-pin plastic TSOP (II).

Features

- 2.5 V power supply: VDDQ = 2.5V ± 0.2V
  : VDD = 2.5V ± 0.2V
- Data rate: 333Mbps/266Mbps (max.)
- Double Data Rate architecture; two data transfers per clock cycle
- Bi-directional, data strobe (DQS) is transmitted /received with data, to be used in capturing data at the receiver
- Data inputs, outputs, and DM are synchronized with DQS
- 4 internal banks for concurrent operation
- DQS is edge aligned with data for READs; center aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Auto precharge option for each burst access
- 2.5 V (SSTL_2 compatible) I/O
- Programmable burst length (BL): 2, 4, 8
- Programmable /CAS latency (CL): 2, 2.5
- Refresh cycles: 8192 refresh cycles/64ms
  — 7.8μs maximum average periodic refresh interval
- 2 variations of refresh
  — Auto refresh
  — Self refresh

Pin Configurations

/xxx indicates active low signal.

66-pin plastic TSOP(II)

X 8	X 16	Pin	Pin	X 16	X 8
VDD	VDD	1	66	VSS	VSS
DQ0	DQ0	2	65	DQ15	DQ7
VDDQ	VDDQ	3	64	VSSQ	VSSQ
NC	DQ1	4	63	DQ14	NC
DQ1	DQ2	5	62	DQ13	DQ6
VSSQ	VSSQ	6	61	VDDQ	VDDQ
NC	DQ3	7	60	DQ12	NC
DQ2	DQ4	8	59	DQ11	DQ5
VDDQ	VDDQ	9	58	VSSQ	VSSQ
NC	DQ5	10	57	DQ10	NC
DQ3	DQ6	11	56	DQ9	DQ4
VSSQ	VSSQ	12	55	VDDQ	VDDQ
NC	DQ7	13	54	DQ8	NC
NC	NC	14	53	NC	NC
VDDQ	VDDQ	15	52	VSSQ	VSSQ
NC	LDQS	16	51	UDQS	DQS
NC	NC	17	50	NC	NC
VDD	VDD	18	49	VREF	VREF
NC	NC	19	48	VSS	VSS
NC	LDM	20	47	UDM	DM
/WE	/WE	21	46	/CK	/CK
/CAS	/CAS	22	45	CK	CK
/RAS	/RAS	23	44	CKE	CKE
/CS	/CS	24	43	NC	NC
NC	NC	25	42	A12	A12
BA0	BA0	26	41	A11	A11
BA1	BA1	27	40	A9	A9
A10(AP)	A10(AP)	28	39	A8	A8
A0	A0	29	38	A7	A7
A1	A1	30	37	A6	A6
A2	A2	31	36	A5	A5
A3	A3	32	35	A4	A4
VDD	VDD	33	34	VSS	VSS

(Top view)

A0 to A12	Address input
BA0, BA1	Bank select address
DQ0 to DQ15	Data-input/output
DQS, UDQS, LDQS	Input and output data strobe
/CS	Chip select
/RAS	Row address strobe command
/CAS	Column address strobe command
/WE	Write enable
DM, UDM, LDM	Input mask
CK	Clock input
/CK	Differential clock input
CKE	Clock enable
VREF	Input reference voltage
VDD	Power for internal circuit
VSS	Ground for internal circuit
VDDQ	Power for DQ circuit
VSSQ	Ground for DQ circuit
NC	No connection

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Ordering Information

Part number	Mask version	Organization (words × bits)	Internal banks	Data rate Mbps (max.)	JEDEC speed bin (CL-tRCD-tRP)	Package
EDD2508AMTA-6B				333	DDR-333B (2.5-3-3)	66-pin Plastic TSOP (II)
EDD2508AMTA-7A	M	32M × 8	4	266	DDR-266A (2-3-3)	
EDD2508AMTA-7B				266	DDR-266B (2.5-3-3)	
EDD2516AMTA-6B				333	DDR-333B (2.5-3-3)	
EDD2516AMTA-7A		16M × 16		266	DDR-266A (2-3-3)	
EDD2516AMTA-7B				266	DDR-266B (2.5-3-3)	

Part Number

E D D 25 16 A M TA - 6B

Elpida Memory

Type
D: Monolithic Device

Product Code
D: DDR SDRAM

Density / Bank
25: 256M / 4-bank

Bit Organization
08: x8
16: x16

Voltage, Interface
A: 2.5V, SSTL_2

Die Rev.

Package
TA: TSOP (II)

Speed
6B: DDR333B (2.5-3-3)
7A: DDR266A (2-3-3)
7B: DDR266B (2.5-3-3)

CONTENTS

Electrical Specifications

- All voltages are referenced to VSS (GND).
- After power up, wait more than 200 μs and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Voltage on input pin relative to VSS	VI	–0.5 to VDD +0.5	V	
Voltage on DQ and DQS pin relative to VSS	VIO	–0.5 to VDDQ +0.5	V	
Supply voltage relative to VSS	VDD	–0.5 to +3.7	V	
Supply voltage for output relative to VSS	VDDQ	–0.5 to +3.7	V	
Short circuit output current	IOS	50	mA	
Power dissipation	PD	1.0	W	
Operating temperature	TA	0 to +70	°C	
Storage temperature	Tstg	–55 to +125	°C	

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

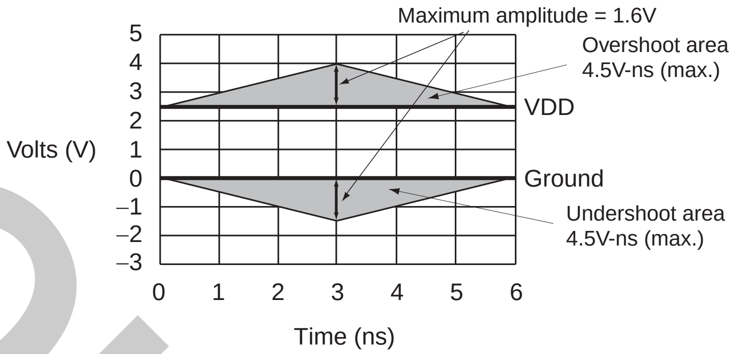
Recommended DC Operating Conditions (TA = 0 to 70°C)

Parameter	Symbol	min	typ	max	Unit	Notes
Supply voltage	VDD, VDDQ	2.3	2.5	2.7	V	1
	VSS, VSSQ	0	0	0	V	
Input reference voltage	VREF	0.49 × VDDQ	0.50 × VDDQ	0.51 × VDDQ	V	
Termination voltage	VTT	VREF – 0.04	VREF	VREF + 0.04	V	
Input high voltage	VIH (DC)	VREF + 0.15	—	VDDQ + 0.3	V	
Input low voltage	VIL (DC)	–0.3	—	VREF – 0.15	V	
Input voltage level, CK and /CK inputs	VIN (DC)	–0.3	—	VDDQ + 0.3	V	2
Input differential cross point voltage, CK and /CK inputs	VIX (DC)	0.5 × VDDQ – 0.2V	0.5 × VDDQ	0.5 × VDDQ + 0.2V	V	
Input differential voltage, CK and /CK inputs	VID (DC)	0.36	—	VDDQ + 0.6	V	3, 4

Notes: 1. VDDQ must be lower than or equal to VDD.
2. VIN (DC) specifies the allowable DC execution of each differential input.
3. VID (DC) specifies the input differential voltage required for switching.
4. VIH (CK) min assumed over VREF + 0.18V, VIL (CK) max assumed under VREF – 0.18V if measurement.

AC Overshoot/Undershoot Specification

Parameter	Specification
Maximum peak amplitude allowed for overshoot	1.6V
Maximum peak amplitude allowed for undershoot	1.6V
The area between the overshoot signal and VDD must be less than or equal to	4.5V-ns
The area between the undershoot signal and GND must be less than or equal to	4.5V-ns



DC Characteristics 1 (TA = 0 to +70°C, VDD, VDDQ = 2.5V ± 0.2V, VSS, VSSQ = 0V)

			max.				
Parameter	Symbol	Grade	× 8	× 16	Unit	Test condition	Notes
Operating current (ACT-PRE)	IDD0	-6B -7A, -7B	80 75	85 80	mA	CKE ≥ VIH, tRC = tRC (min.)	1, 2, 9
Operating current (ACT-READ-PRE)	IDD1	-6B -7A, -7B	115 100	125 115	mA	CKE ≥ VIH, BL = 4, CL = 2.5, tRC = tRC (min.)	1, 2, 5
Idle power down standby current	IDD2P		4	4	mA	CKE ≤ VIL	4
Floating idle standby current	IDD2F	-6B -7A, -7B	35 30	35 30	mA	CKE ≥ VIH, /CS ≥ VIH DQ, DQS, DM = VREF	4, 5
Quiet idle standby current	IDD2Q	-6B -7A, -7B	35 30	35 30	mA	CKE ≥ VIH, /CS ≥ VIH DQ, DQS, DM = VREF	4, 10
Active power down standby current	IDD3P	-6B -7A, -7B	25 20	25 20	mA	CKE ≤ VIL	3
Active standby current	IDD3N	-6B -7A, -7B	40 35	45 40	mA	CKE ≥ VIH, /CS ≥ VIH tRAS = tRAS (max.)	3, 5, 6
Operating current (Burst read operation)	IDD4R	-6B -7A, -7B	200 135	250 180	mA	CKE ≥ VIH, BL = 2, CL = 2.5	1, 2, 5, 6
Operating current (Burst write operation)	IDD4W	-6B -7A, -7B	175 125	200 160	mA	CKE ≥ VIH, BL = 2, CL = 2.5	1, 2, 5, 6
Auto Refresh current	IDD5	-6B -7A, -7B	145 140	145 140	mA	tRFC = tRFC (min.), Input ≤ VIL or ≥ VIH	
Self refresh current	IDD6		3	3	mA	Input ≥ VDD – 0.2 V Input ≤ 0.2 V	
Operating current (4 banks interleaving)	IDD7A	-6B -7A, -7B	300 260	330 300	mA	BL = 4	5, 6, 7

Notes: 1. These IDD data are measured under condition that DQ pins are not connected.
2. One bank operation.
3. One bank active.
4. All banks idle.
5. Command/Address transition once per one clock cycle.
6. DQ, DM and DQS transition twice per one clock cycle.
7. 4 banks active. Only one bank is running at tRC = tRC (min.)
8. The IDD data on this table are measured with regard to tCK = tCK (min.) in general.
9. Command/Address transition once every two clock cycle.
10. Command/Address stable at ≥ VIH or ≤ VIL.

DC Characteristics 2 (TA = 0 to +70°C, VDD, VDDQ = 2.5V ± 0.2V, VSS, VSSQ = 0V)

Parameter	Symbol	min.	max.	Unit	Test condition	Notes
Input leakage current	ILI	–2	2	µA	VDD ≥ VIN ≥ VSS	
Output leakage current	ILO	–5	5	µA	VDDQ ≥ VOUT ≥ VSS	
Output high current	IOH	–16.2	—	mA	VOUT = 1.95V	
Output low current	IOL	16.2	—	mA	VOUT = 0.35V	

Pin Capacitance (TA = +25°C, VDD, VDDQ = 2.5V ± 0.2V)

Parameter	Symbol	Pins	min.	Typ	max.	Unit	Notes
Input capacitance	CI1	CK, /CK	2.0	—	3.0	pF	1
	CI2	All other input pins	2.0	—	3.0	pF	1
Delta input capacitance	Cdi1	CK, /CK	—	—	0.25	pF	1
	Cdi2	All other input-only pins	—	—	0.5	pF	1
Data input/output capacitance	CI/O	DQ, DM, DQS	4.0	—	5	pF	1, 2,
Delta input/output capacitance	Cdio	DQ, DM, DQS	—	—	0.5	pF	1

Notes: 1. These parameters are measured on conditions: f = 100MHz, VOUT = VDDQ/2, ∆VOUT = 0.2V, TA = +25°C.

2. DOUT circuits are disabled.

AC Characteristics (TA = 0 to +70°C, VDD, VDDQ = 2.5V ± 0.2V, VSS, VSSQ = 0V)

		-6B		-7A		-7B			
Parameter	Symbol	min.	max.	min.	max.	min.	max	Unit	Notes
Clock cycle time (CL = 2)	tCK	7.5	12	7.5	12	10	12	ns	10
(CL = 2.5)	tCK	6	12	7.5	12	7.5	12	ns	
CK high-level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min (tCH, tCL)	—	min (tCH, tCL)	—	min (tCH, tCL)	—	tCK	
DQ output access time from CK, /CK	tAC	–0.7	0.7	–0.75	0.75	–0.75	0.75	ns	2, 11
DQS output access time from CK, /CK	tDQSCK	–0.6	0.6	–0.75	0.75	–0.75	0.75	ns	2, 11
DQS to DQ skew	tDQSQ	—	0.45	—	0.5	—	0.5	ns	3
DQ/DQS output hold time from DQS	tQH	tHP – tQHS	—	tHP – tQHS	—	tHP – tQHS	—	ns	
Data hold skew factor	tQHS	—	0.55	—	0.75	—	0.75	ns	
Data-out high-impedance time from CK, /CK	tHZ	–0.7	0.7	–0.75	0.75	–0.75	0.75	ns	5, 11
Data-out low-impedance time from CK, /CK	tLZ	–0.7	0.7	–0.75	0.75	–0.75	0.75	ns	6, 11
Read preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQ and DM input setup time	tDS	0.45	—	0.5	—	0.5	—	ns	8
DQ and DM input hold time	tDH	0.45	—	0.5	—	0.5	—	ns	8
DQ and DM input pulse width	tDIPW	1.75	—	1.75	—	1.75	—	ns	7
Write preamble setup time	tWPRES	0	—	0	—	0	—	ns	
Write preamble	tWPRE	0.25	—	0.25	—	0.25	—	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK	9
Write command to first DQS latching transition	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK	
DQS falling edge to CK setup time	tDSS	0.2	—	0.2	—	0.2	—	tCK	
DQS falling edge hold time from CK	tDSH	0.2	—	0.2	—	0.2	—	tCK	
DQS input high pulse width	tDQSH	0.35	—	0.35	—	0.35	—	tCK	
DQS input low pulse width	tDQSL	0.35	—	0.35	—	0.35	—	tCK	
Address and control input setup time	tIS	0.75	—	0.9	—	0.9	—	ns	8

Parameter	Symbol	-6B min.	-6B max.	-7A min.	-7A max.	-7B min.	-7B max	Unit	Notes
Address and control input hold time	tIH	0.75	—	0.9	—	0.9	—	ns	8
Address and control input pulse width	tIPW	2.2	—	2.2	—	2.2	—	ns	7
Mode register set command cycle time	tMRD	2	—	2	—	2	—	tCK	
Active to Precharge command period	tRAS	42	120000	45	120000	45	120000	ns	
Active to Active/Auto refresh command period	tRC	60	—	65	—	65	—	ns	
Auto refresh to Active/Auto refresh command period	tRFC	72	—	75	—	75	—	ns	
Active to Read/Write delay	tRCD	18	—	20	—	20	—	ns	
Precharge to active command period	tRP	18	—	20	—	20	—	ns	
Active to Autoprecharge delay	tRAP	tRCD min.	—	tRCD min.	—	tRCD min.	—	ns	
Active to active command period	tRRD	12	—	15	—	15	—	ns	
Write recovery time	tWR	15	—	15	—	15	—	ns	
Auto precharge write recovery and precharge time	tDAL	(tWR/tCK)+ (tRP/tCK)	—	(tWR/tCK)+ (tRP/tCK)	—	(tWR/tCK)+ (tRP/tCK)	—	tCK	13
Internal write to Read command delay	tWTR	1	—	1	—	1	—	tCK	
Average periodic refresh interval	tREF	—	7.8	—	7.8	—	7.8	μs	

Notes:
1. On all AC measurements, we assume the test conditions shown in the next page. For timing parameter definitions, see ‘Timing Waveforms’ section.
2. This parameter defines the signal transition delay from the cross point of CK and /CK. The signal transition is defined to occur when the signal level crossing VTT.
3. The timing reference level is VTT.
4. Output valid window is defined to be the period between two successive transition of data out or DQS (read) signals. The signal transition is defined to occur when the signal level crossing VTT.
5. tHZ is defined as DOUT transition delay from Low-Z to High-Z at the end of read burst operation. The timing reference is cross point of CK and /CK. This parameter is not referred to a specific DOUT voltage level, but specify when the device output stops driving.
6. tLZ is defined as DOUT transition delay from High-Z to Low-Z at the beginning of read operation. This parameter is not referred to a specific DOUT voltage level, but specify when the device output begins driving.
7. Input valid windows is defined to be the period between two successive transition of data input or DQS (write) signals. The signal transition is defined to occur when the signal level crossing VREF.
8. The timing reference level is VREF.
9. The transition from Low-Z to High-Z is defined to occur when the device output stops driving. A specific reference voltage to judge this transition is not given.
10. tCK (max.) is determined by the lock range of the DLL. Beyond this lock range, the DLL operation is not assured.
11. tCK = tCK (min) when these parameters are measured. Otherwise, absolute minimum values of these values are 10% of tCK.
12. VDD is assumed to be 2.5V ± 0.2V. VDD power supply variation per cycle expected to be less than 0.4V/400 cycle.
13. tDAL = (tWR/tCK)+(tRP/tCK)

    For each of the terms above, if not already an integer, round to the next highest integer.

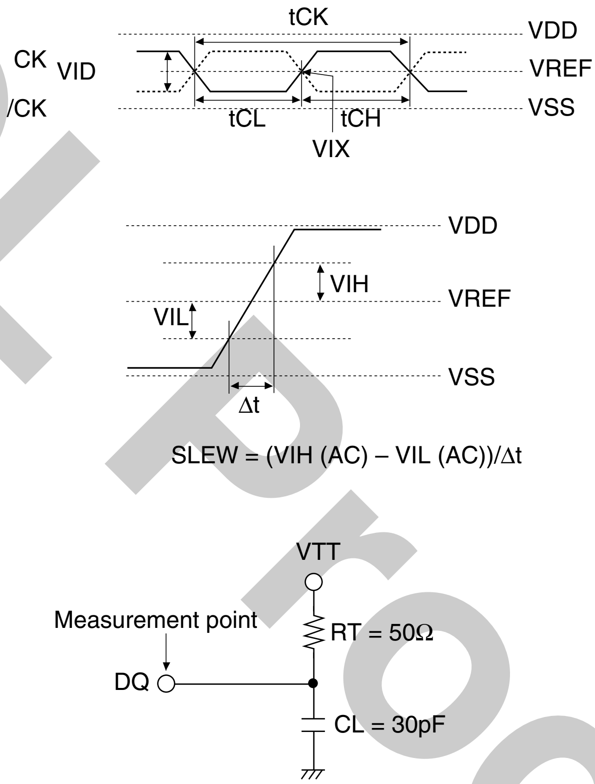
    Example: For –7A Speed at CL = 2.5, tCK = 7.5ns, tWR = 15ns and tRP= 20ns,

    tDAL = (15ns/7.5ns) + (20ns/7.5ns) = (2) + (3)

    tDAL = 5 clocks

Test Conditions

Parameter	Symbol	Value	Unit
Input reference voltage	VREF	VDDQ/2	V
Termination voltage	VTT	VREF	V
Input high voltage	VIH (AC)	VREF + 0.31	V
Input low voltage	VIL (AC)	VREF − 0.31	V
Input differential voltage, CK and /CK inputs	VID (AC)	0.7	V
Input differential cross point voltage, CK and /CK inputs	VIX (AC)	VREF	V
Input signal slew rate	SLEW	1	V/ns

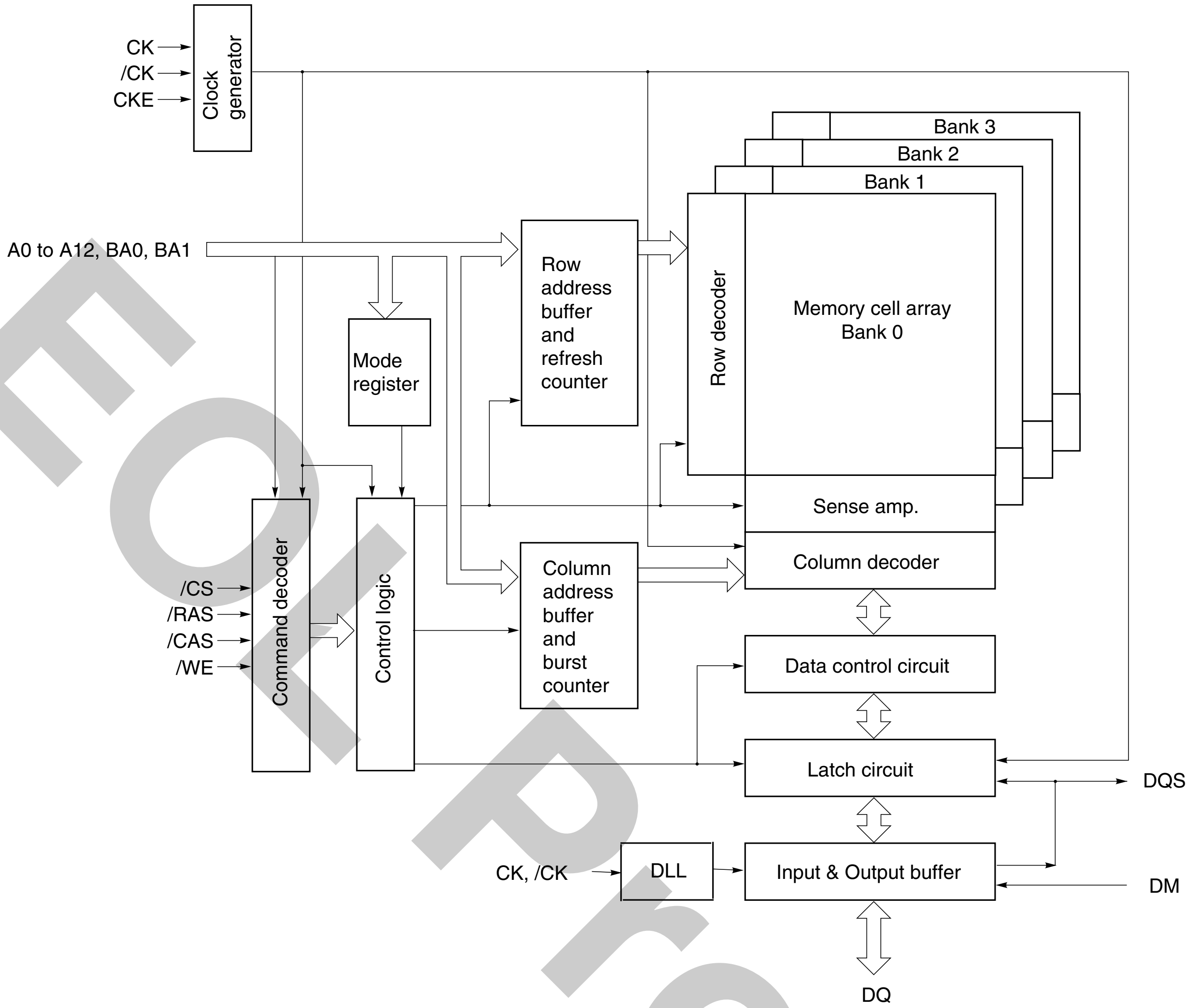


Input Waveforms and Output Load

Timing Parameter Measured in Clock Cycle

		Number of clock cycle				
tCK		6ns		7.5ns		
Parameter	Symbol	min.	max.	min.	max.	Unit
Write to pre-charge command delay (same bank)	tWPD	4 + BL/2		3 + BL/2		tCK
Read to pre-charge command delay (same bank)	tRPD	BL/2		BL/2		tCK
Write to read command delay (to input all data)	tWRD	2 + BL/2		2 + BL/2		tCK
Burst stop command to write command delay (CL = 2)	tBSTW	2		2		tCK
(CL = 2.5)	tBSTW	3		3		tCK
Burst stop command to DQ High-Z (CL = 2)	tBSTZ	2	2	2	2	tCK
(CL = 2.5)	tBSTZ	2.5	2.5	2.5	2.5	tCK
Read command to write command delay (to output all data) (CL = 2)	tRWD	2 + BL/2		2 + BL/2		tCK
(CL = 2.5)	tRWD	3 + BL/2		3 + BL/2		tCK
Pre-charge command to High-Z (CL = 2)	tHZP	2	2	2	2	tCK
(CL = 2.5)	tHZP	2.5	2.5	2.5	2.5	tCK
Write command to data in latency	tWCD	1	1	1	1	tCK
Write recovery	tWR	3		2		tCK
DM to data in latency	tDMD	0	0	0	0	tCK
Mode register set command cycle time	tMRD	2		2		tCK
Self refresh exit to non-read command	tSNR	12		10		tCK
Self refresh exit to read command	tSRD	200		200		tCK
Power down entry	tPDEN	1	1	1	1	tCK
Power down exit to command input	tPDEX	1		1		tCK

Block Diagram



Pin Function

CK, /CK (input pins)

The CK and the /CK are the master clock inputs. All inputs except DM, DQS and DQs are referred to the cross point of the CK rising edge and the /CK falling edge. When a read operation, DQS and DQs are referred to the cross point of the CK and the /CK. When a write operation, DQS and DQs are referred to the cross point of the DQS and the VREF level. DQS for write operation is referred to the cross point of the CK and the /CK. CK is the master clock input to this pin. The other input signals are referred at CK rising edge.

/CS (input pin)

When /CS is Low, commands and data can be input. When /CS is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RAS, /CAS, and /WE (input pins)

These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 to A12 (input pins)

Row address (AX0 to AX12) is determined by the A0 to the A12 level at the cross point of the CK rising edge and the /CK falling edge in a bank active command cycle. Column address (See “Address Pins Table”) is loaded via the A0 to the A8 at the cross point of the CK rising edge and the /CK falling edge in a read or a write command cycle. This column address becomes the starting address of a burst operation.

[Address Pins Table]

	Address (A0 to A12)	
Part number	Row address	Column address
EDD2508AM	AX0 to AX12	AY0 to AY9
EDD2516AM	AX0 to AX12	AY0 to AY8

A10 (AP) (input pin)

A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = High when a precharge command is issued, all banks are precharged. If A10 = Low when a precharge command is issued, only the bank that is selected by BA1/BA0 is precharged. If A10 = High when read or write command, auto-precharge function is enabled. While A10 = Low, auto-precharge function is disabled.

BA0 and BA1 (input pins)

BA0, BA1 are bank select signals (BA). The memory array is divided into bank 0, bank 1, bank 2 and bank 3. (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1
Bank 0	L	L
Bank 1	H	L
Bank 2	L	H
Bank 3	H	H

Remark: H: VIH. L: VIL.

CKE (input pin)

This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low. CKE controls power down and self-refresh. The power down and the self-refresh commands are entered when the CKE is driven Low and exited when it resumes to High. CKE must be maintained high throughout read or write access.

The CKE level must be kept for 1 CK cycle at least, that is, if CKE changes at the cross point of the CK rising edge and the /CK falling edge with proper setup time tIS, by the next CK rising edge CKE level must be kept with proper hold time tIH.

DM, UDM, LDM (input pin)

DMs are the reference signals of the data input mask function. DMs are sampled at the cross point of DQS and V_{REF}. DMs provide the byte mask function. In × 16 products, LDM controls the lower byte (DQ0 to DQ7) and UDM controls the upper byte (DQ8 to DQ15) of write data. When DM = High, the data input at the same timing are masked while the internal burst counter will be count up. LDM controls the lower byte (DQ0 to DQ7) and UDM controls the upper byte (DQ8 to DQ15) of write data.

DQ0 to DQ15 (input/output pins)

Data is input to and output from these pins.

DQS, UDQS, LDQS (input and output pin): DQS provide the read data strobes (as output) and the write data strobes (as input). In ×16 products, LDQS is the lower byte (DQ0 to DQ7) data strobe signal, UDQS is the upper byte (DQ8 to DQ15) data strobe signal.

VDD, VSS, VDDQ, VSSQ (Power supply)

VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers.

Command Operation

Command Truth Table

DDR SDRAM recognize the following commands specified by the /CS, /RAS, /CAS, /WE and address pins. All other combinations than those in the table below are illegal.

Command	Symbol	CKE n – 1	CKE n	/CS	/RAS	/CAS	/WE	BA1	BA0	AP	Address
Ignore command	DESL	H	H	H	×	×	×	×	×	×	×
No operation	NOP	H	H	L	H	H	H	×	×	×	×
Burst stop in read command	BST	H	H	L	H	H	L	×	×	×	×
Column address and read command	READ	H	H	L	H	L	H	V	V	L	V
Read with auto-precharge	READA	H	H	L	H	L	H	V	V	H	V
Column address and write command	WRIT	H	H	L	H	L	L	V	V	L	V
Write with auto-precharge	WRITA	H	H	L	H	L	L	V	V	H	V
Row address strobe and bank active	ACT	H	H	L	L	H	H	V	V	V	V
Precharge select bank	PRE	H	H	L	L	H	L	V	V	L	×
Precharge all bank	PALL	H	H	L	L	H	L	×	×	H	×
Refresh	REF	H	H	L	L	L	H	×	×	×	×
	SELF	H	L	L	L	L	H	×	×	×	×
Mode register set	MRS	H	H	L	L	L	L	L	L	L	V
	EMRS	H	H	L	L	L	L	L	H	L	V

Remark: H: VIH. L: VIL. ×: VIH or VIL V: Valid address input

Note: The CKE level must be kept for 1 CK cycle at least.

Ignore command [DESL]

When /CS is High at the cross point of the CK rising edge and the VREF level, every input are neglected and internal status is held.

No operation [NOP]

As long as this command is input at the cross point of the CK rising edge and the VREF level, address and data input are neglected and internal status is held.

Burst stop in read operation [BST]

This command stops a burst read operation, which is not applicable for a burst write operation.

Column address strobe and read command [READ]

This command starts a read operation. The start address of the burst read is determined by the column address (See “Address Pins Table” in Pin Function) and the bank select address. After the completion of the read operation, the output buffer becomes High-Z.

Read with auto-precharge [READA]

This command starts a read operation. After completion of the read operation, precharge is automatically executed.

Column address strobe and write command [WRIT]

This command starts a write operation. The start address of the burst write is determined by the column address (See “Address Pins Table” in Pin Function) and the bank select address.

Write with auto-precharge [WRITA]

This command starts a write operation. After completion of the write operation, precharge is automatically executed.

Row address strobe and bank activate [ACT]

This command activates the bank that is selected by BA0, BA1 and determines the row address (AX0 to AX12). (See Bank Select Signal Table)

Precharge selected bank [PRE]

This command starts precharge operation for the bank selected by BA0, BA1. (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1
Bank 0	L	L
Bank 1	H	L
Bank 2	L	H
Bank 3	H	H

Remark: H: VIH. L: VIL.

Precharge all banks [PALL]

This command starts a precharge operation for all banks.

Refresh [REF/SELF]

This command starts a refresh operation. There are two types of refresh operation, one is auto-refresh, and another is self-refresh. For details, refer to the CKE truth table section.

Mode register set/Extended mode register set [MRS/EMRS]

The DDR SDRAM has the two mode registers, the mode register and the extended mode register, to defines how it works. The both mode registers are set through the address pins (the A0 to the A12, BA0 to BA1) in the mode register set cycle. For details, refer to "Mode register and extended mode register set".

CKE Truth Table

		CKE							
Current state	Command	n – 1	n	/CS	/RAS	/CAS	/WE	Address	Notes
Idle	Auto-refresh command (REF)	H	H	L	L	L	H	×	2
Idle	Self-refresh entry (SELF)	H	L	L	L	L	H	×	2
Idle	Power down entry (PDEN)	H	L	L	H	H	H	×	
		H	L	H	×	×	×	×	
Self refresh	Self refresh exit (SELFX)	L	H	L	H	H	H	×	
		L	H	H	×	×	×	×	
Power down	Power down exit (PDEX)	L	H	L	H	H	H	×	
		L	H	H	×	×	×	×	

Remark: H: VIH. L: VIL. ×: VIH or VIL.

Notes: 1. All the banks must be in IDLE before executing this command.

2. The CKE level must be kept for 1 CK cycle at least.

Function Truth Table

The following tables show the operations that are performed when each command is issued in each state of the DDR SDRAM.

Function Truth Table

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Next state
Precharging*[1]	H	×	×	×	×	DESL	NOP	Idle
	L	H	H	H	×	NOP	NOP	Idle
	L	H	H	L	×	BST	ILLEGAL*[11]	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*[11]	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[11]	—
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]	—
	L	L	H	L	BA, A10	PRE, PALL	NOP	Idle
	L	L	L	×	×		ILLEGAL	—
Idle*[2]	H	×	×	×	×	DESL	NOP	Idle
	L	H	H	H	×	NOP	NOP	Idle
	L	H	H	L	×	BST	ILLEGAL*[11]	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*[11]	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[11]	—
	L	L	H	H	BA, RA	ACT	Activating	Active
	L	L	H	L	BA, A10	PRE, PALL	NOP	Idle
	L	L	L	H	×	REF, SELF	Refresh/ Self refresh*[12]	Idle/ Self refresh
	L	L	L	L	MODE	MRS	Mode register set*[12]	Idle
Refresh (auto-refresh)*[3]	H	×	×	×	×	DESL	NOP	Idle
	L	H	H	H	×	NOP	NOP	Idle
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	×	×		ILLEGAL	—
	L	L	×	×	×		ILLEGAL	—
Activating*[4]	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	ILLEGAL*[11]	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*[11]	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[11]	—
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]	—
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*[11]	—
	L	L	L	×	×		ILLEGAL	—

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Next state
Active*[5]	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	ILLEGAL	Active
	L	H	L	H	BA, CA, A10	READ/READA	Starting read operation	Read/READA
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Starting write operation	Write recovering/ precharging
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]	—
	L	L	H	L	BA, A10	PRE, PALL	Pre-charge	Idle
	L	L	L	×	×		ILLEGAL	—
Read*[6]	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	BST	Active
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst read operation to start new read	Active
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[13]	—
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]	—
	L	L	H	L	BA, A10	PRE, PALL	Interrupting burst read operation to start pre-charge	Precharging
	L	L	L	×	×		ILLEGAL	—
Read with auto-pre-charge*[7]	H	×	×	×	×	DESL	NOP	Precharging
	L	H	H	H	×	NOP	NOP	Precharging
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*[14]	—
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*[14]	—
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11, 14]	—
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*[11, 14]	—
	L	L	L	×	×		ILLEGAL	—
Write*[8]	H	×	×	×	×	DESL	NOP	Write recovering
	L	H	H	H	×	NOP	NOP	Write recovering
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst write operation to start read operation.	Read/ReadA
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Interrupting burst write operation to start new write operation.	Write/WriteA
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]	—
	L	L	H	L	BA, A10	PRE, PALL	Interrupting write operation to start pre-charge.	Idle
	L	L	L	×	×		ILLEGAL	—

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation	Next state
Write recovering*[9]	H	×	×	×	×	DESL	NOP	Active
	L	H	H	H	×	NOP	NOP	Active
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	Starting read operation.	Read/ReadA
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Starting new write operation.	Write/WriteA
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11]	—
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL*[11]	—
	L	L	L	×	×		ILLEGAL	—
Write with auto-pre-charge*[10]	H	×	×	×	×	DESL	NOP	Precharging
	L	H	H	H	×	NOP	NOP	Precharging
	L	H	H	L	×	BST	ILLEGAL	—
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*[14]	—
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL*[14]	—
	L	L	H	H	BA, RA	ACT	ILLEGAL*[11, 14]	—
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*[11, 14]	—
	L	L	L	×	×		ILLEGAL	—

Remark: H: VIH. L: VIL. ×: VIH or VIL

Notes:
1. The DDR SDRAM is in "Precharging" state for tRP after precharge command is issued.
2. The DDR SDRAM reaches "IDLE" state tRP after precharge command is issued.
3. The DDR SDRAM is in "Refresh" state for tRFC after auto-refresh command is issued.
4. The DDR SDRAM is in "Activating" state for tRCD after ACT command is issued.
5. The DDR SDRAM is in "Active" state after "Activating" is completed.
6. The DDR SDRAM is in "READ" state until burst data have been output and DQ output circuits are turned off.
7. The DDR SDRAM is in "READ with auto-precharge" from READA command until burst data has been output and DQ output circuits are turned off.
8. The DDR SDRAM is in "WRITE" state from WRIT command to the last burst data are input.
9. The DDR SDRAM is in "Write recovering" for tWR after the last data are input.
10. The DDR SDRAM is in "Write with auto-precharge" until tWR after the last data has been input.
11. This command may be issued for other banks, depending on the state of the banks.
12. All banks must be in "IDLE".
13. Before executing a write command to stop the preceding burst read operation, BST command must be issued.

14. The DDR SDRAM supports the concurrent auto-precharge feature, a read with auto-precharge enabled,or a write with auto-precharge enabled, may be followed by any column command to other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply. (E.g. Conflict between READ data and WRITE data must be avoided.)

The minimum delay from a read or write command with auto precharge enabled, to a command to a different bank, is summarized below.

From command	To command (different bank, non-interrupting command)	Minimum delay (Concurrent AP supported)	Units
Read w/AP	Read or Read w/AP	BL/2	tCK
	Write or Write w/AP	CL(rounded up)+ (BL/2)	tCK
	Precharge or Activate	1	tCK
Write w/AP	Read or Read w/AP	1 + (BL/2) + tWTR	tCK
	Write or Write w/AP	BL/2	tCK
	Precharge or Activate	1	tCK

Command Truth Table for CKE

Current State	CKE n – 1	CKE n	/CS	/RAS	/CAS	/WE	Address	Operation	Notes
Self refresh	H	×	×	×	×	×	×	INVALID, CK (n-1) would exit self refresh	
	L	H	H	×	×	×	×	Self refresh recovery	
	L	H	L	H	H	×	×	Self refresh recovery	
	L	H	L	H	L	×	×	ILLEGAL	
	L	H	L	L	×	×	×	ILLEGAL	
	L	L	×	×	×	×	×	Maintain self refresh	
Self refresh recovery	H	H	H	×	×	×	×	Idle after tRC	
	H	H	L	H	H	×	×	Idle after tRC	
	H	H	L	H	L	×	×	ILLEGAL	
	H	H	L	L	×	×	×	ILLEGAL	
	H	L	H	×	×	×	×	ILLEGAL	
	H	L	L	H	H	×	×	ILLEGAL	
	H	L	L	H	L	×	×	ILLEGAL	
	H	L	L	L	×	×	×	ILLEGAL	
Power down	H	×	×	×	×	×		INVALID, CK (n – 1) would exit power down	
	L	H	H	×	×	×	×	EXIT power down → Idle	
	L	H	L	H	H	H	×		
	L	L	×	×	×	×	×	Maintain power down mode	
All banks idle	H	H	H	×	×	×		Refer to operations in Function Truth Table	
	H	H	L	H	×	×		Refer to operations in Function Truth Table	
	H	H	L	L	H	×		Refer to operations in Function Truth Table	
	H	H	L	L	L	H	×	CBR (auto) refresh	
	H	H	L	L	L	L	OPCODE	Refer to operations in Function Truth Table	
	H	L	H	×	×	×		Refer to operations in Function Truth Table	
	H	L	L	H	×	×		Refer to operations in Function Truth Table	
	H	L	L	L	H	×		Refer to operations in Function Truth Table	
	H	L	L	L	L	H	×	Self refresh	1
	H	L	L	L	L	L	OPCODE	Refer to operations in Function Truth Table	
	L	×	×	×	×	×	×	Power down	1
Row active	H	×	×	×	×	×	×	Refer to operations in Function Truth Table	
	L	×	×	×	×	×	×	Power down	1

Remark: H: VIH. L: VIL. ×: VIH or VIL

Note: Self refresh can be entered only from the all banks idle state. Power down can be entered only from all banks idle or row active state.

Auto-refresh command [REF]

This command executes auto-refresh. The banks and the ROW addresses to be refreshed are internally determined by the internal refresh controller. The average refresh cycle is 7.8 μs. The output buffer becomes High-Z after auto-refresh start. Precharge has been completed automatically after the auto-refresh. The ACT or MRS command can be issued tRFC after the last auto-refresh command.

Self-refresh entry [SELF]

This command starts self-refresh. The self-refresh operation continues as long as CKE is held Low. During the self-refresh operation, all ROW addresses are repeated refreshing by the internal refresh controller. A self-refresh is terminated by a self-refresh exit command.

Power down mode entry [PDEN]

tPDEN (= 1 cycle) after the cycle when [PDEN] is issued. The DDR SDRAM enters into power-down mode. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. No internal refresh operation occurs during the power down mode. [PDEN] do not disable DLL.

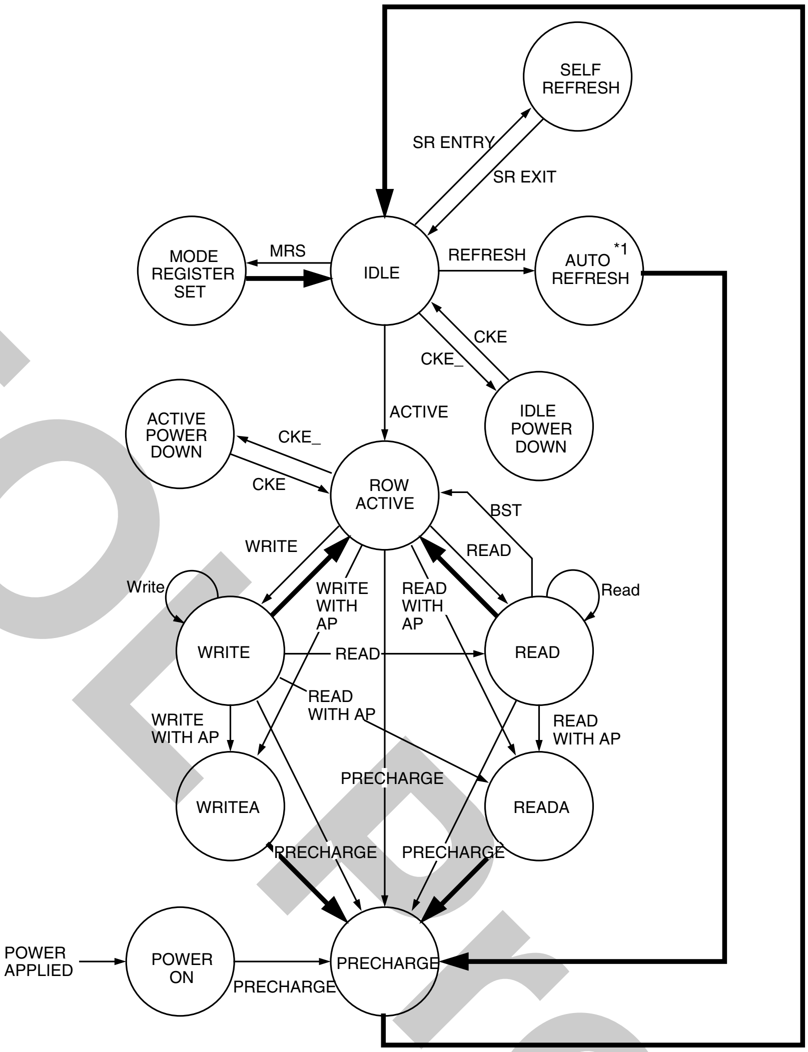
Self-refresh exit [SELFX]

This command is executed to exit from self-refresh mode. To issue non-read commands, tSNR has to be satisfied. ((tSNR =)10 cycles for tCK = 7.5 ns or 12 cycles for tCK = 6.0 ns after [SELFX]) To issue read command, tSRD has to be satisfied to adjust DOUT timing by DLL. (200 cycles after [SELFX]) After the exit, input auto-refresh command within 7.8 μs.

Power down exit [PDEX]

The DDR SDRAM can exit from power down mode tPDEX (1 cycle min.) after the cycle when [PDEX] is issued.

Simplified State Diagram



Automatic transition after completion of command.

Transition resulting from command input.

Note: 1. After the auto-refresh operation, precharge operation is performed automatically and enter the IDLE state.

Operation of the DDR SDRAM

Power-up Sequence

The following sequence is recommended for Power-up.

(1) Apply power and attempt to maintain CKE at an LVCMOS low state (all other inputs may be undefined).
Apply VDD before or at the same time as VDDQ.
Apply VDDQ before or at the same time as VTT and VREF.

(2) Start clock and maintain stable condition for a minimum of 200 µs.

(3) After the minimum 200 µs of stable power and clock (CK, /CK), apply NOP and take CKE high.

(4) Issue precharge all command for the device.

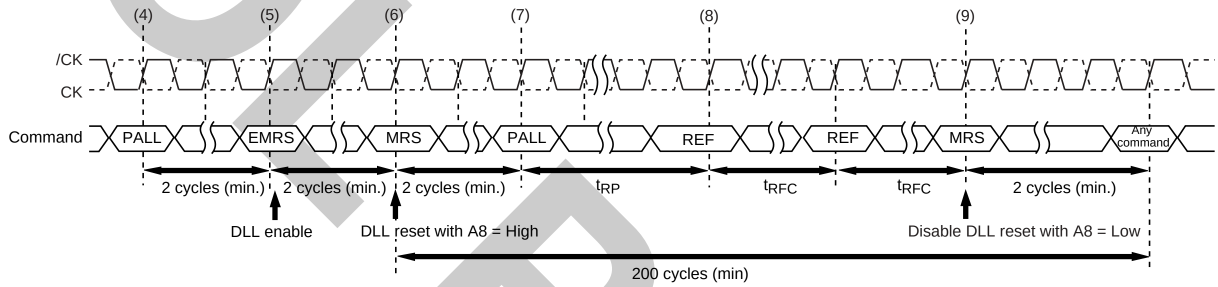
(5) Issue EMRS to enable DLL.

(6) Issue a mode register set command (MRS) for "DLL reset" with bit A8 set to high (An additional 200 cycles of clock input is required to lock the DLL after every DLL reset).

(7) Issue precharge all command for the device.

(8) Issue 2 or more auto-refresh commands.

(9) Issue a mode register set command to initialize device operation with bit A8 set to low in order to avoid resetting the DLL.



Power-up Sequence after CKE Goes High

Mode Register and Extended Mode Register Set

There are two mode registers, the mode register and the extended mode register so as to define the operating mode. Parameters are set to both through the A0 to the A12 and BA0, BA1 pins by the mode register set command [MRS] or the extended mode register set command [EMRS]. The mode register and the extended mode register are set by inputting signal via the A0 to the A12 and BA0, BA1 during mode register set cycles. BA0 and BA1 determine which one of the mode register or the extended mode register are set. Prior to a read or a write operation, the mode register must be set.
Remind that no other parameters shown in the table bellow are allowed to input to the registers.

BA0	BA1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	DR	0	LMODE			BT	BL		

MRS

A8	DLL Reset
0	No
1	Yes

A6	A5	A4	CAS Latency
0	1	0	2
1	1	0	2.5

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length	
			BT=0	BT=1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8

Mode Register Set [MRS] (BA0 = 0, BA1 = 0)

BA0	BA1	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	DLL

EMRS

A0	DLL Control
0	DLL Enable
1	DLL Disable

Extended Mode Register Set [EMRS] (BA0 = 1, BA1 = 0)

Burst Operation

The burst type (BT) and the first three bits of the column address determine the order of a data out.

Burst length = 2

Starting Ad.	Addressing(decimal)	
A0	Sequence	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

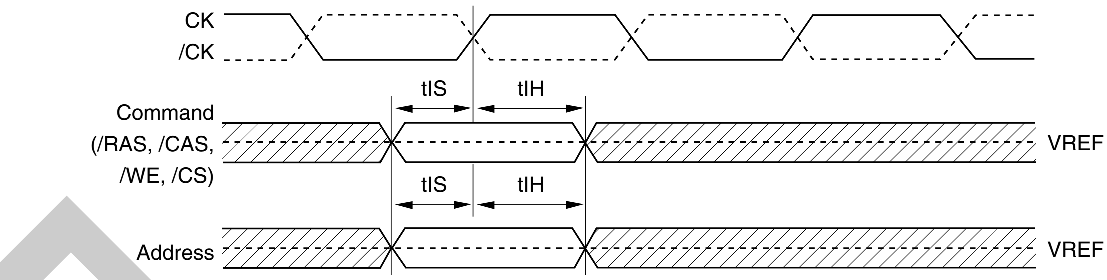
Starting Ad.		Addressing(decimal)	
A1	A0	Sequence	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

Burst length = 8

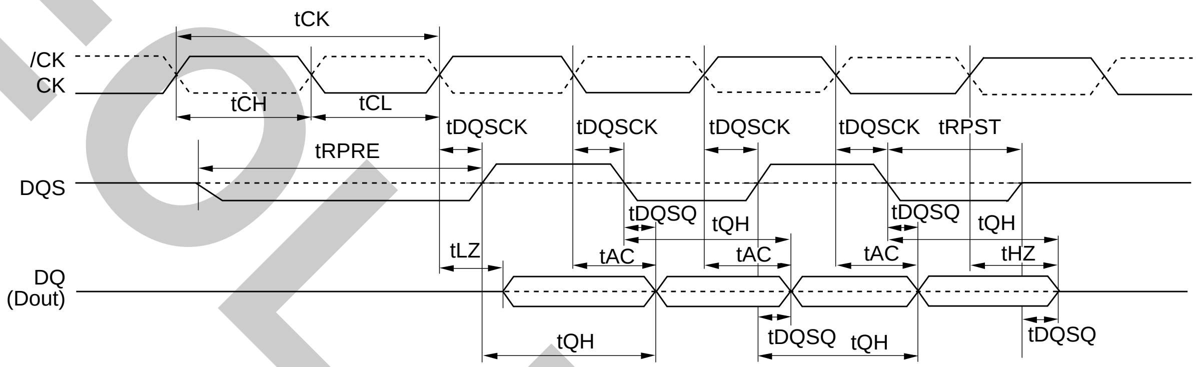
Starting Ad.			Addressing(decimal)	
A2	A1	A0	Sequence	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0,

Timing Waveforms

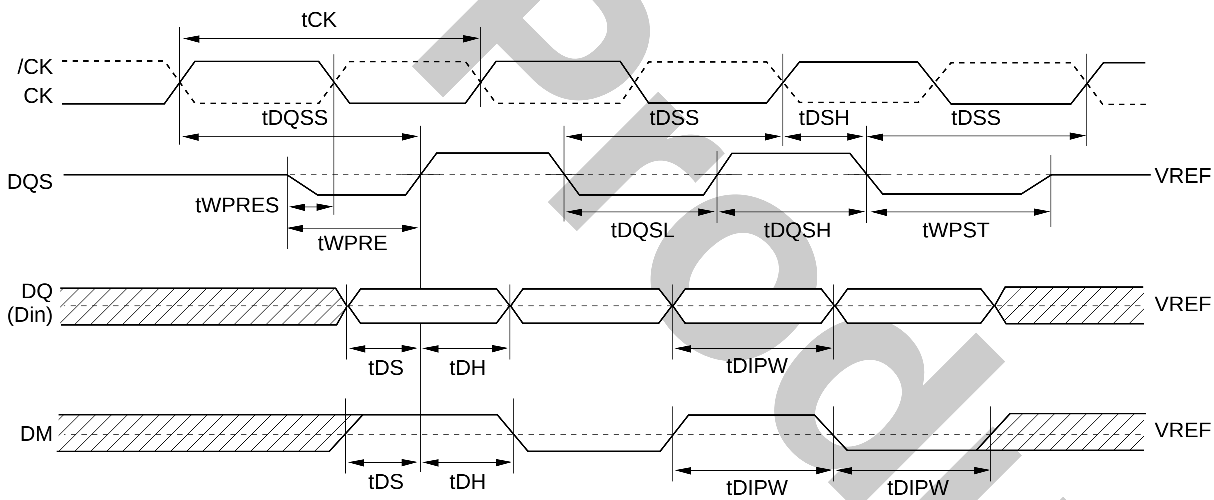
Command and Addresses Input Timing Definition



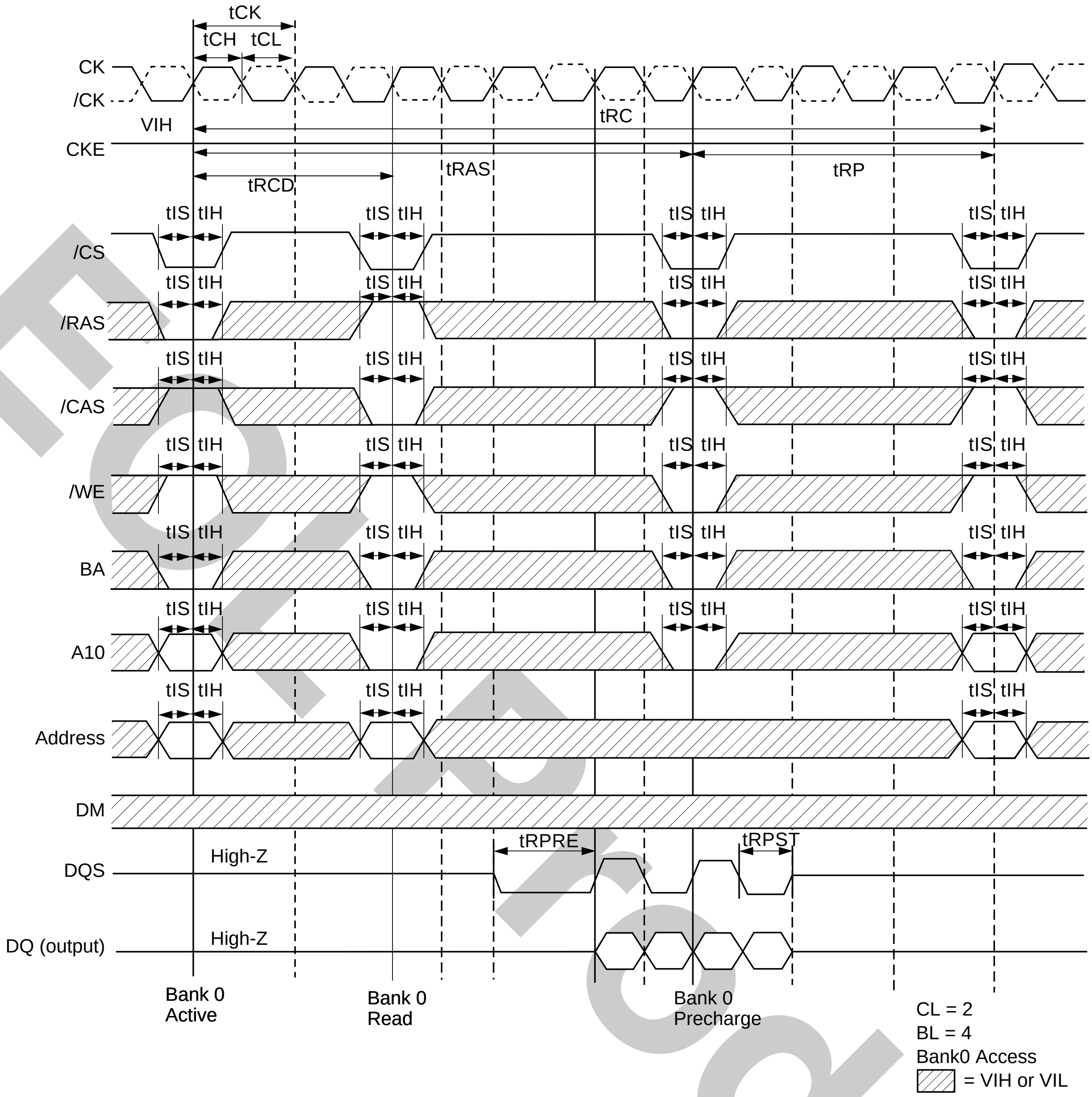
Read Timing Definition



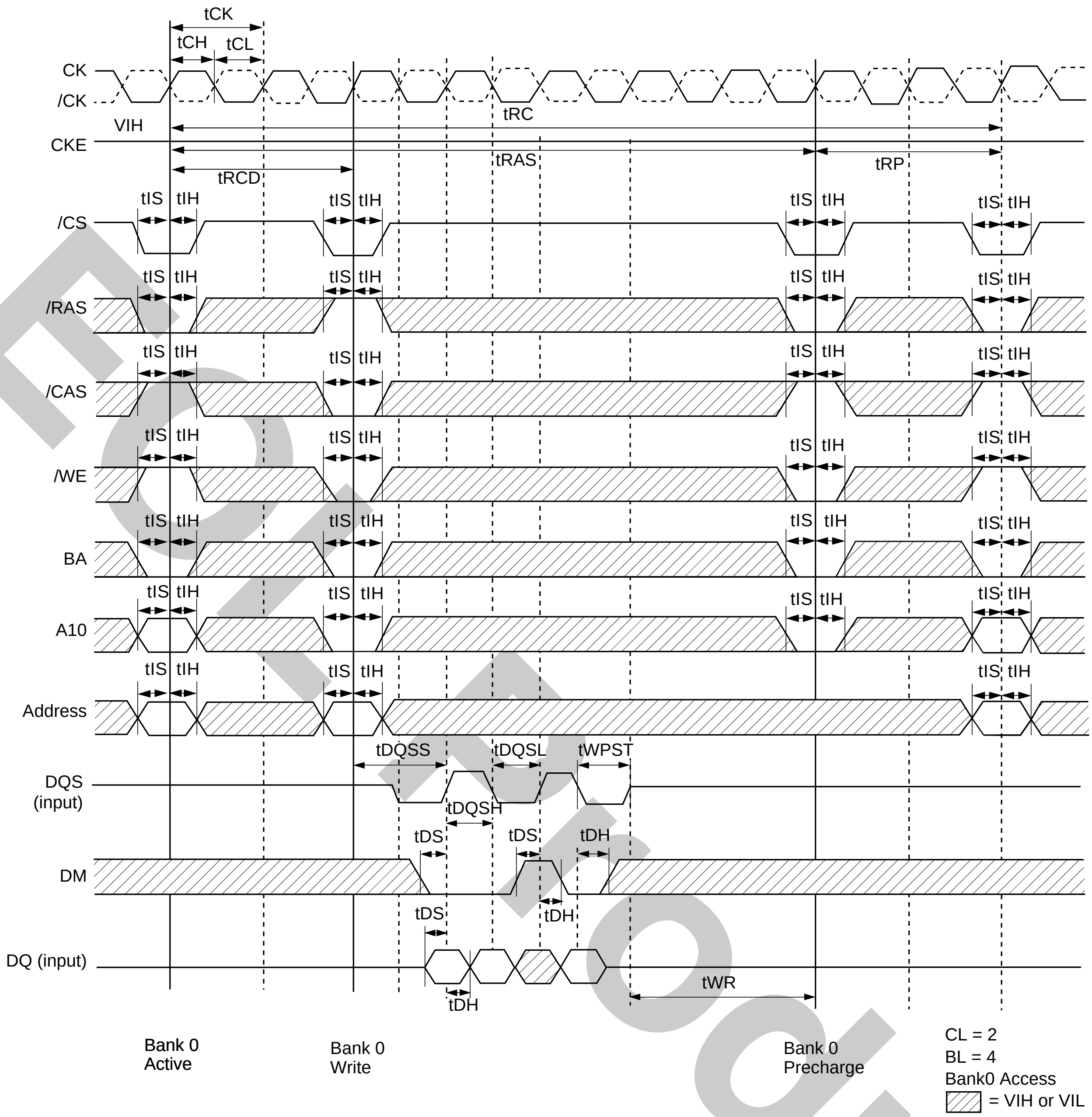
Write Timing Definition



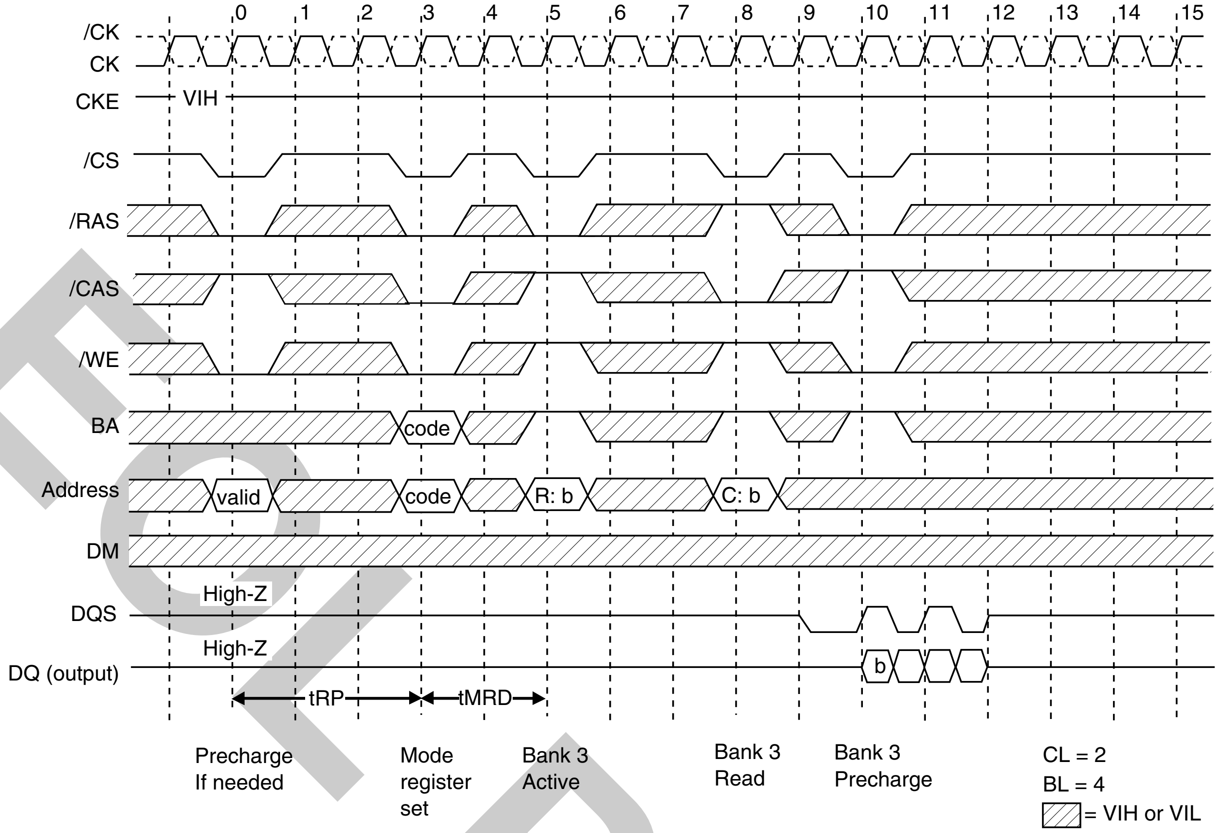
Read Cycle


tCK
tCH tCL
CK
/CK
VIH
tRC
CKE
tRAS
tRP
tRCD
tIS tIH
/CS
/RAS
/CAS
/WE
BA
A10
Address
DM
tRPRE
tRPST
DQS
High-Z
DQ (output)
High-Z
Bank 0
Active
Bank 0
Read
Bank 0
Precharge
CL = 2
BL = 4
Bank0 Access
= VIH or VIL

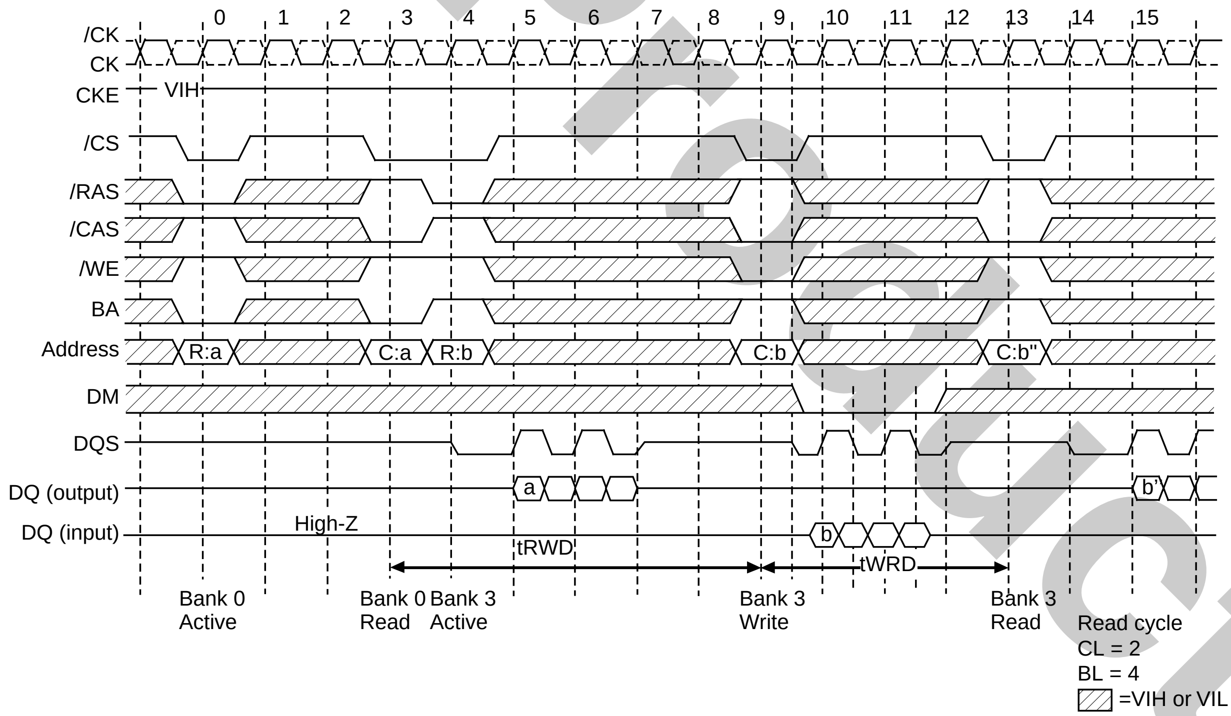
Write Cycle


tCK
tCH
tCL
CK
/CK
VIH
tRC
CKE
tRAS
tRP
tRCD
tIS
tIH
/CS
/RAS
/CAS
/WE
BA
A10
Address
tDQSS
tDQSL
tWPST
DQS
(input)
tDQSH
tDS
tDH
DM
DQ (input)
tWR
Bank 0
Active
Bank 0
Write
Bank 0
Precharge
CL = 2
BL = 4
Bank0 Access
= VIH or VIL

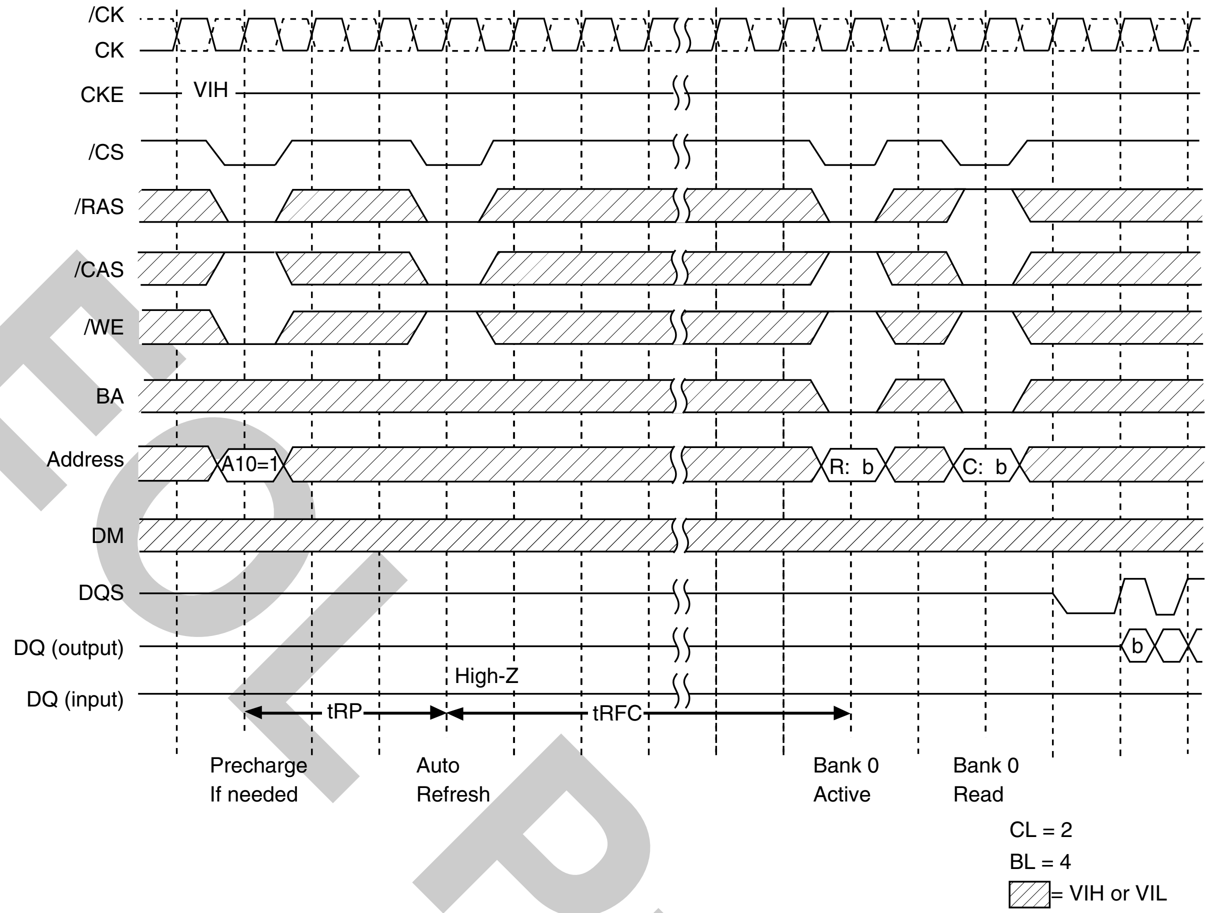
Mode Register Set Cycle



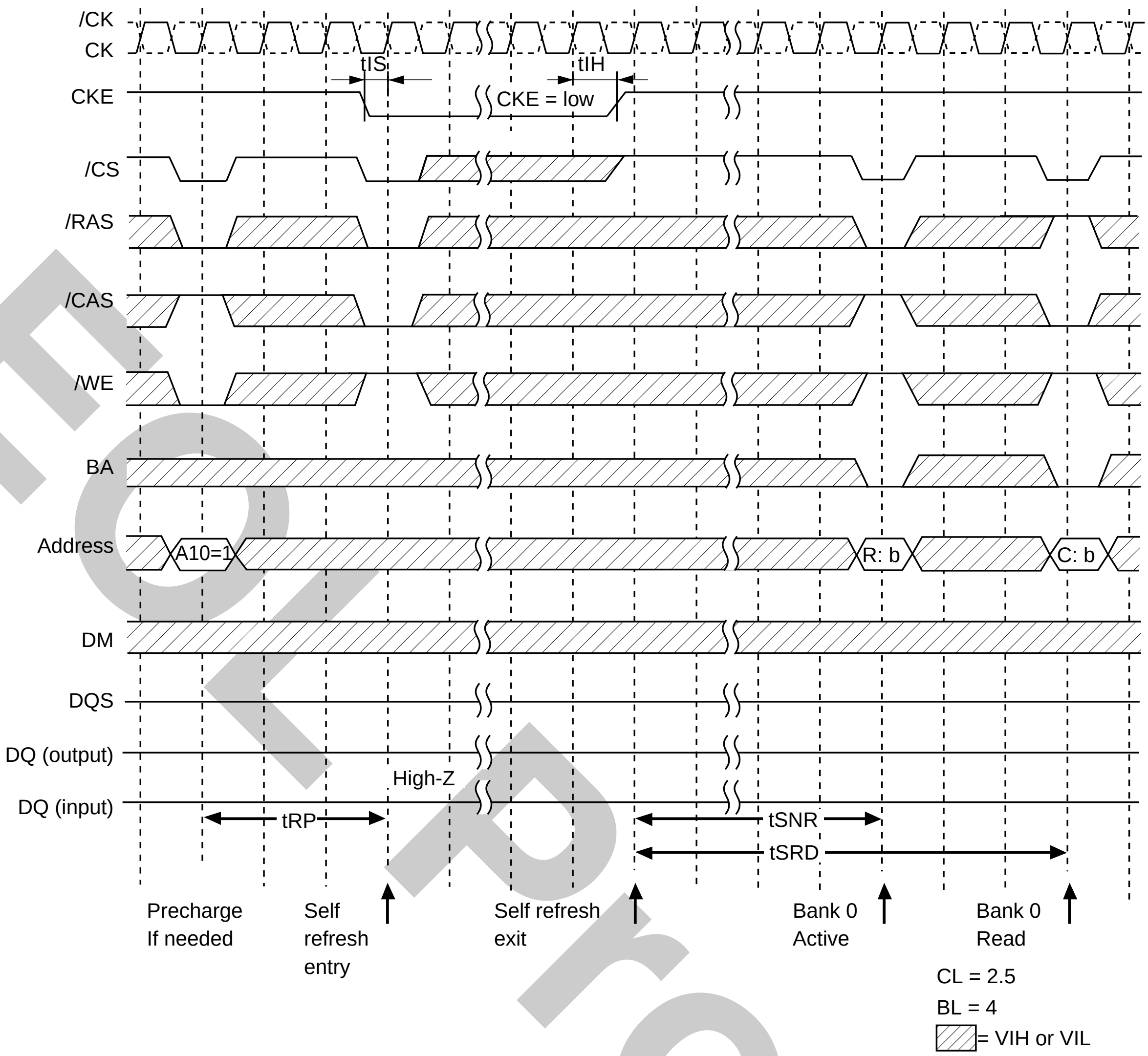
Read/Write Cycle



Auto Refresh Cycle



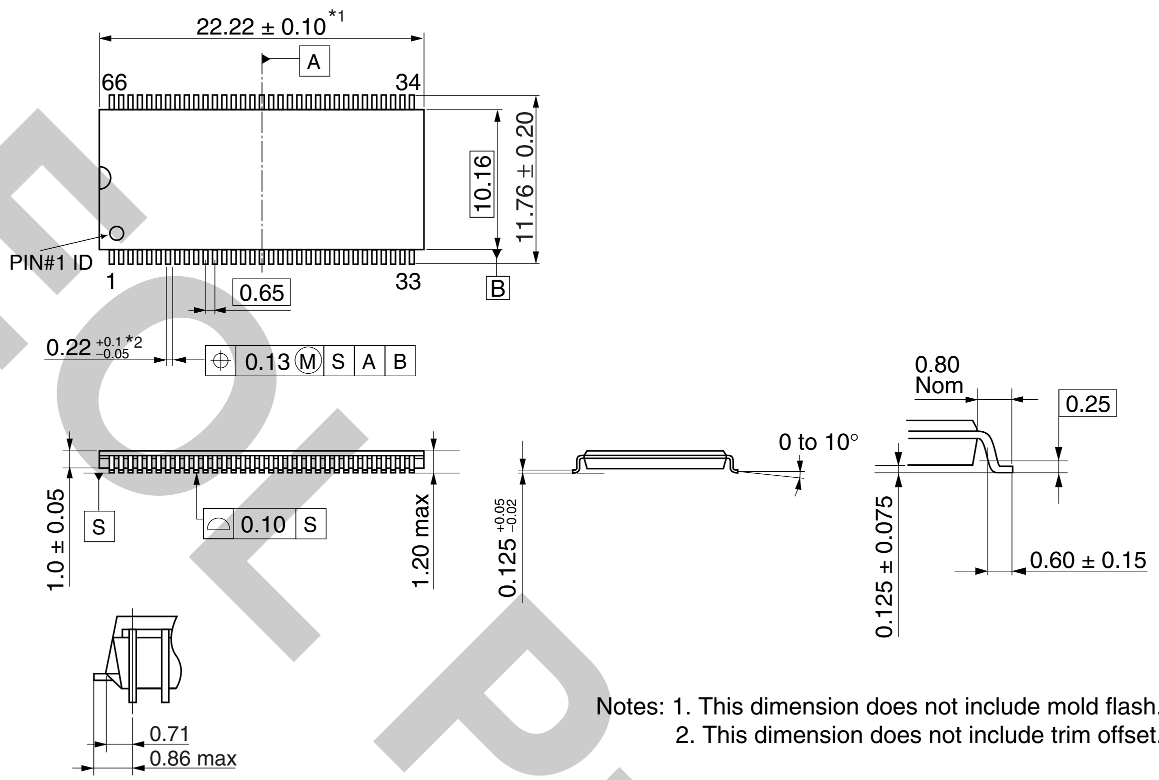
Self Refresh Cycle



Package Drawing

66-pin Plastic TSOP (II)

Unit: mm



Notes: 1. This dimension does not include mold flash.
2. This dimension does not include trim offset.

ECA-TS2-0097-01

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the EDD2508AM, EDD2516AM.

Type of Surface Mount Device

EDD2508AMTA, EDD2516AMTA: 66-pin Plastic TSOP (II)

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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[Product usage]
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[Usage environment]
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