

Silicon PNP Power Transistors

2SB512

DESCRIPTION

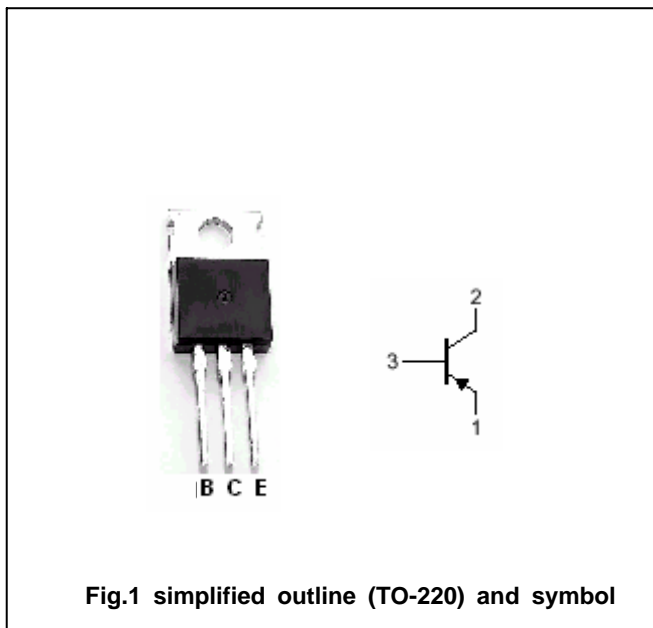
- With TO-220 package
- Low collector saturation voltage

APPLICATIONS

- For low frequency power amplifier applications

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector;connected to mounting base
3	Base



Absolute maximum ratings(Ta=25)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V _{CBO}	Collector-base voltage	Open emitter	-60	V
V _{CEO}	Collector-emitter voltage	Open base	-60	V
V _{EBO}	Emitter-base voltage	Open collector	-5	V
I _C	Collector current		-3	A
P _C	Collector power dissipation	T _C =25	25	W
T _j	Junction temperature		150	
T _{stg}	Storage temperature		-55~150	

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CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-10mA, I _B =0	-60			V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =-1mA, I _E =0	-60			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =-1mA, I _C =0	-6			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-2A; I _B =-0.2A			-1.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =-2A; I _B =-0.2A			-1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =-40V; I _E =0			-1.0	μA
I _{EBO}	Emitter cut-off current	V _{EB} =-4V; I _C =0			-1.0	μA
h _{FE}	DC current gain	I _C =-0.5A; V _{CE} =-5V	60		320	
f _T	Transition frequency	I _C =-0.5A; V _{CE} =-10V	3			MHz

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PACKAGE OUTLINE

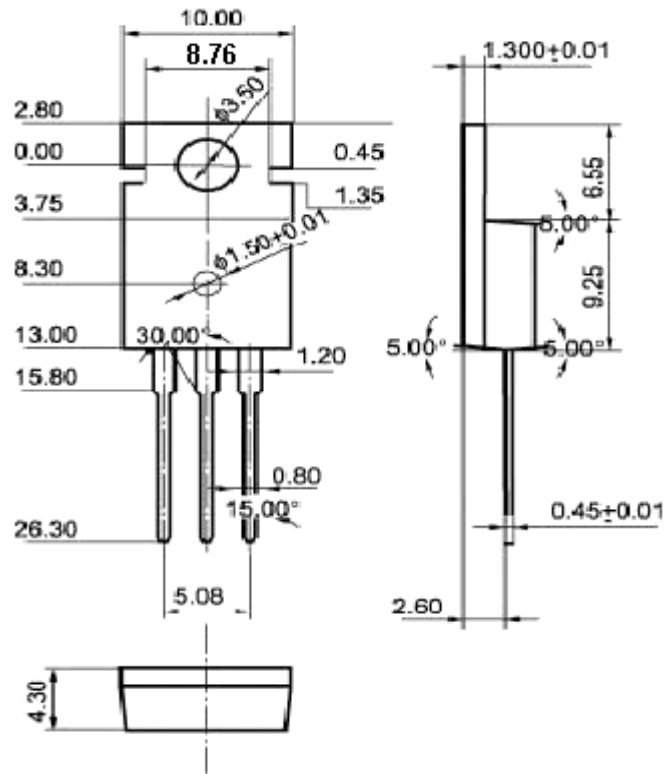


Fig.2 Outline dimensions(unindicated tolerance: ± 0.10 mm)