RQJ0306FQDQS

Silicon P Channel MOS FET
Power Switching

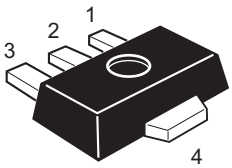
REJ03G1780-0100
Rev.1.00
Mar 16, 2009

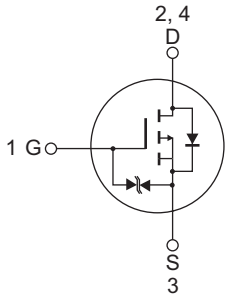
Features

- Low gate drive
  V_{DSS} : –30 V and 2.5 V gate drive
- Low drive current
- High speed switching
- Small traditional power package (UPAK)

Outline

RENESAS package code: PLZZ0004CA-A
(Package name: UPAK®)





1. Gate
2. Drain
3. Source
4. Drain

Notes: Marking is "FQ".

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	–30	V
Gate to source voltage	V_{GSS}	+8 / –12	V
Drain current	I_D	–4	A
Drain peak current	$I_{D(pulse)}$ Note1	–16	A
Body - drain diode reverse drain current	I_{DR}	4	A
Channel dissipation	Pch Note2	1.5	W
Thermal resistance	Rth(ch-a) Note2	83	°C /W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Notes: 1. PW ≤ 10 µs, Duty cycle ≤ 1%
2. When using the glass epoxy board (FR-4 40 × 40 × 1 mm)

Electrical Characteristics

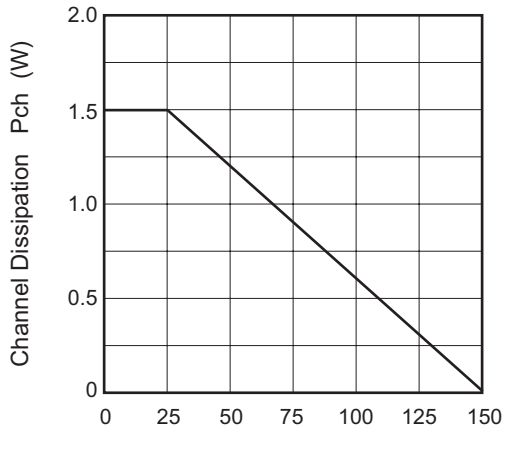
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	–30	—	—	V	I_D = –10 mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	+8	—	—	V	I_G = +100 µA, V_{DS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	–12	—	—	V	I_G = –100 µA, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	+10	µA	V_{GS} = +6 V, V_{DS} = 0
Gate to source leak current	I_{GSS}	—	—	–10	µA	V_{GS} = –10 V, V_{DS} = 0
Drain to source leak current	I_{DSS}	—	—	–1	µA	V_{DS} = –30 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	–0.4	—	–1.4	V	V_{DS} = –10 V, I_D = -1 mA
Drain to source on state resistance	$R_{DS(on)}$	—	75	95	mΩ	I_D = –2.0 A, V_{GS} = –4.5 V [Note3]
Drain to source on state resistance	$R_{DS(on)}$	—	120	165	mΩ	I_D = –2.0 A, V_{GS} = –2.5 V [Note3]
Forward transfer admittance	$\|y_{fs}\|$	4.5	6.0	—	S	I_D = –2.0 A, V_{DS} = –10 V [Note3]
Input capacitance	Ciss	—	510	—	pF	V_{DS} = –10 V, V_{GS} = 0, f = 1 MHz
Output capacitance	Coss	—	100	—	pF	
Reverse transfer capacitance	Crss	—	58	—	pF	
Turn - on delay time	$t_{d(on)}$	—	18	—	ns	I_D = –1.5 A, V_{GS} = –4.5 V, R_L = 6.7 Ω, R_g = 4.7 Ω
Rise time	t_r	—	48	—	ns	
Turn - off delay time	$t_{d(off)}$	—	47	—	ns	
Fall time	t_f	—	13	—	ns	
Total gate charge	Qg	—	4.8	—	nC	V_{DD} = –10 V, V_{GS} = –4.5 V, I_D = –3.0 A
Gate to Source charge	Qgs	—	0.8	—	nC	
Gate to drain charge	Qgd	—	1.8	—	nC	
Body - drain diode forward voltage	V_{DF}	—	–0.9	–1.3	V	I_F = –4.0 A, V_{GS} = 0 [Note3]

Notes: 3. Pulse test

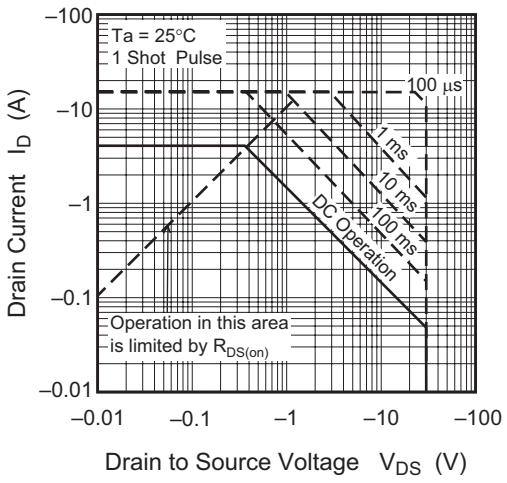
Main Characteristics

Maximum Channel Power Dissipation Curve

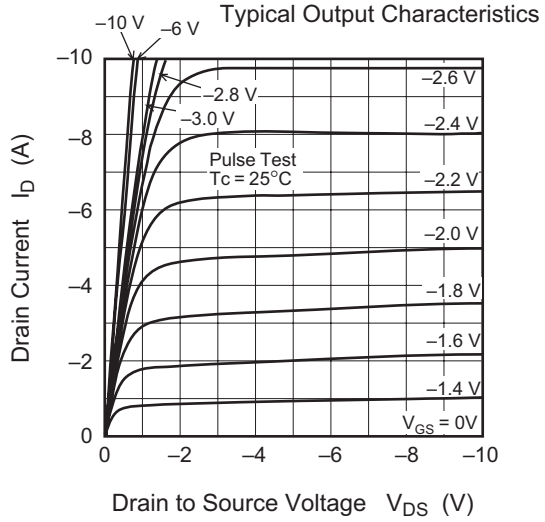


*When using the glass epoxy board (FR-4: 40 × 40 × 1 mm)

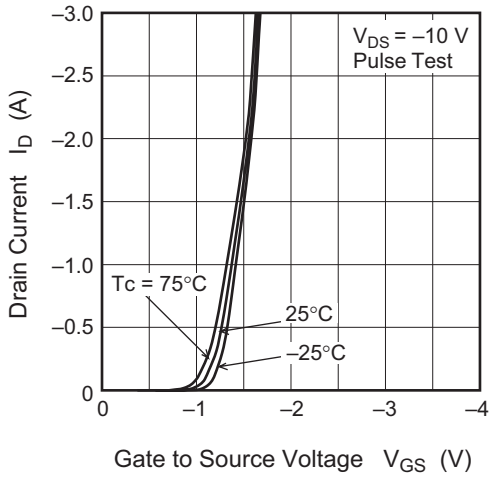
Maximum Safe Operation Area



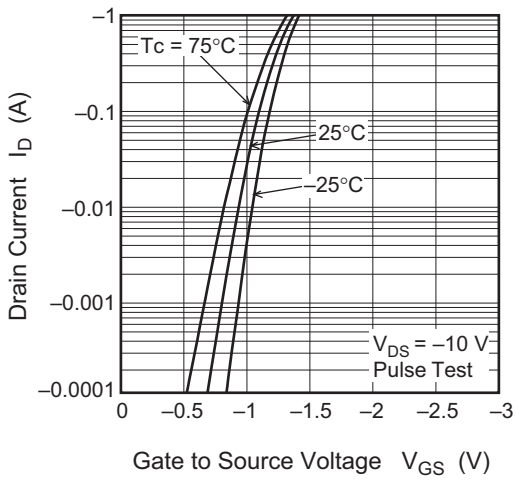
Typical Output Characteristics



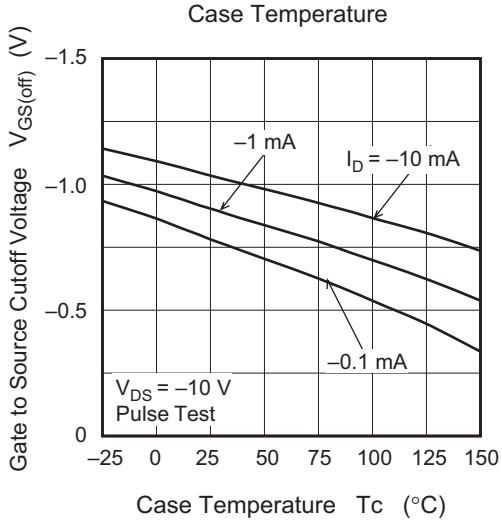
Typical Transfer Characteristics (1)



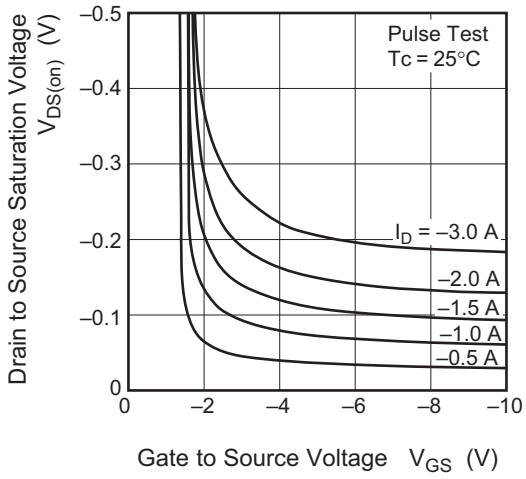
Typical Transfer Characteristics (2)



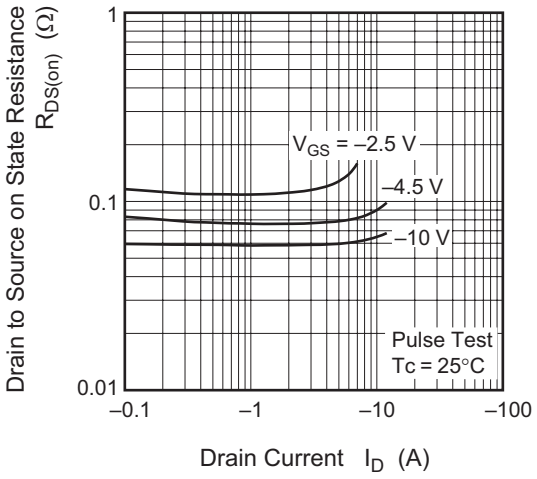
Gate to Source Cutoff Voltage vs. Case Temperature



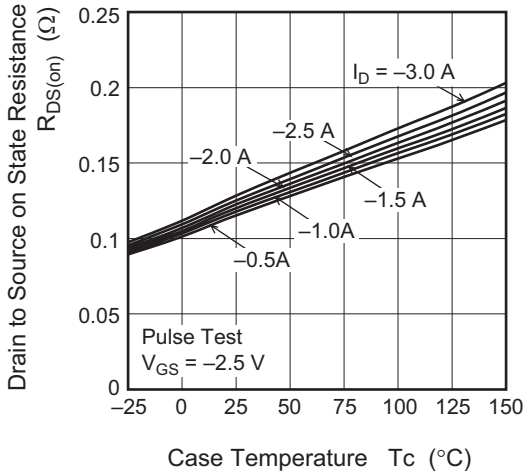
Drain to Source Saturation Voltage vs. Gate to Source Voltage



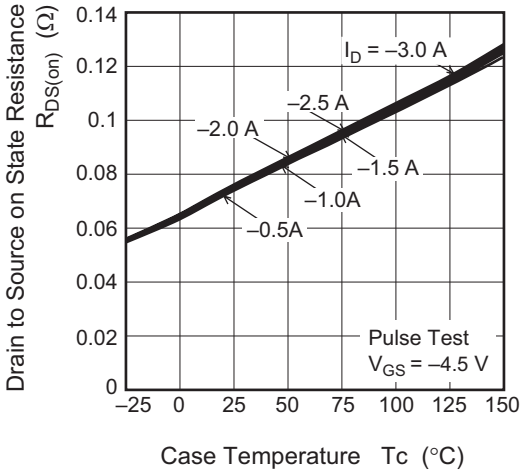
Static Drain to Source on State Resistance vs. Drain Current



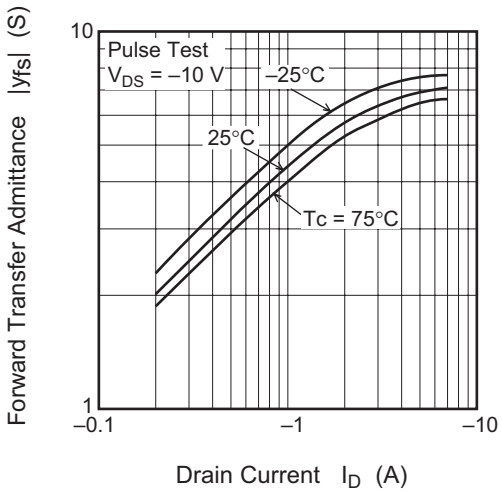
Static Drain to Source on State Resistance vs. Case Temperature (1)



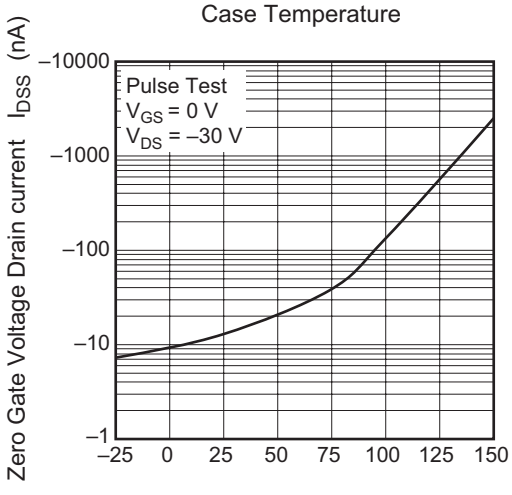
Static Drain to Source on State Resistance vs. Case Temperature (2)



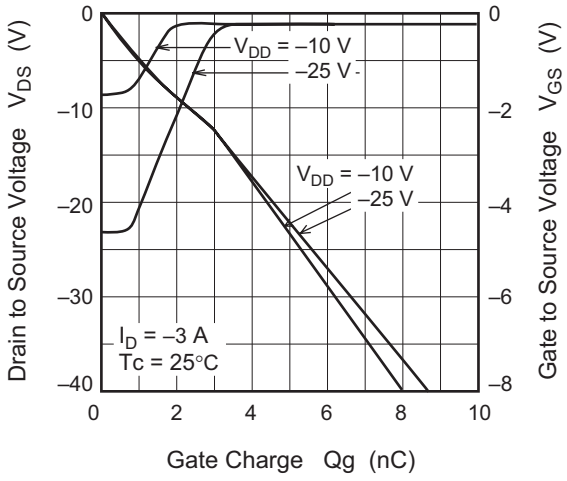
Forward Transfer Admittance vs. Drain Current



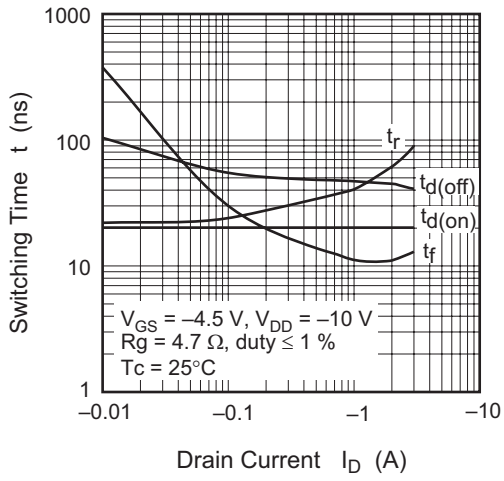
Zero Gate Voltage Drain current vs. Case Temperature



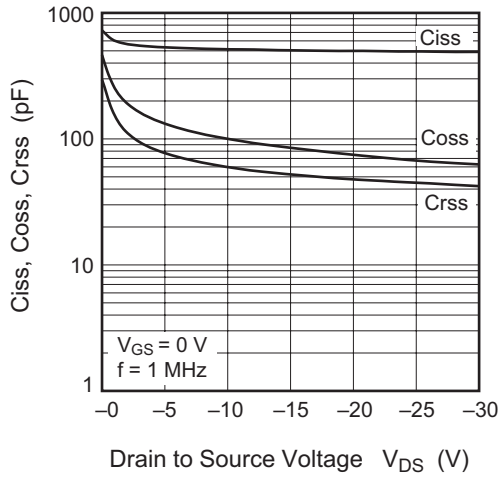
Dynamic Input Characteristics



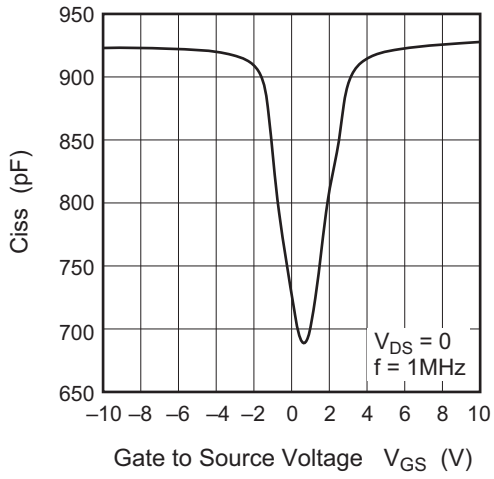
Switching Characteristics



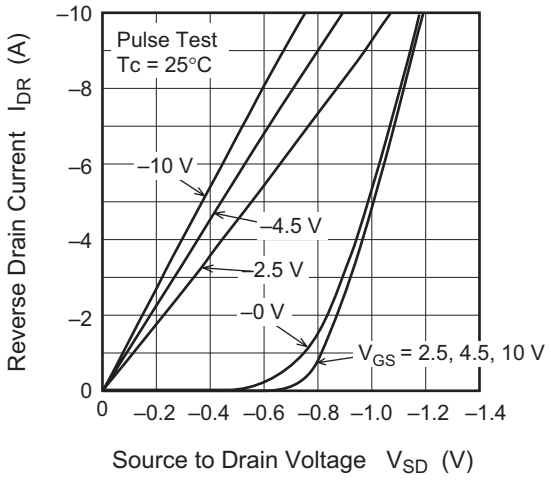
Typical Capacitance vs.
Drain to Source Voltage



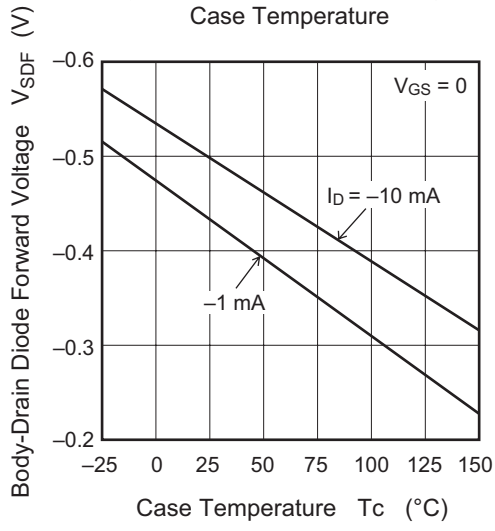
Input Capacitance vs.
Gate to Source Voltage



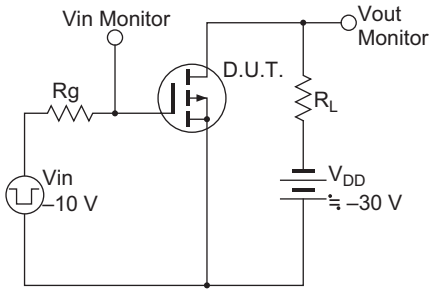
Reverse Drain Current vs.
Source to Drain Voltage



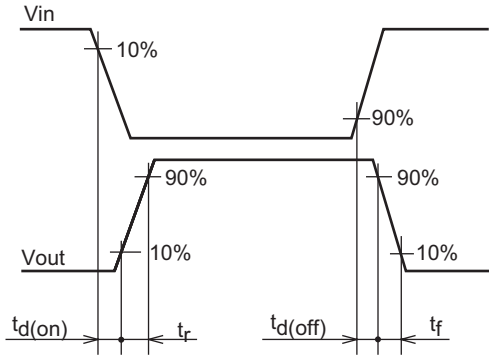
Body-Drain Diode Forward Voltage vs.
Case Temperature



Switching Time Test Circuit



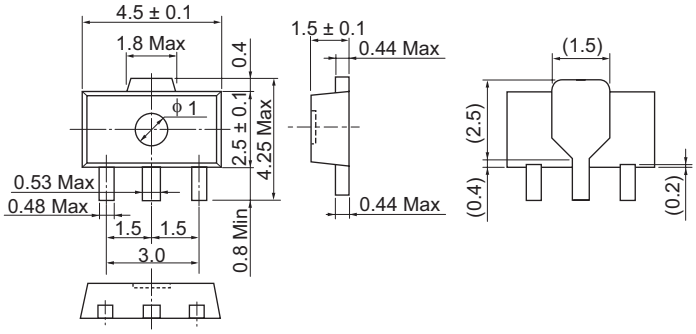
Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
UPAK	SC-62	PLZZ0004CA-A	UPAK / UPAKV	0.050g

Unit: mm



Ordering Information

Part No.	Quantity	Shipping Container
RQJ0306FQDQSTL-E	1000 pcs.	ϕ178 mm reel, 12 mm Emboss taping

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

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Colophon .7.2