

10-18GHz Low Noise, Variable Gain Amplifier

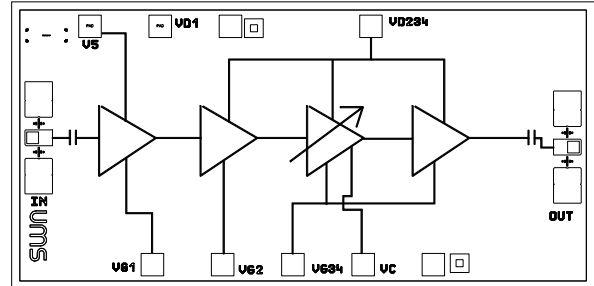
GaAs Monolithic Microwave IC

Description

The CHA2291 is a high gain four-stage monolithic low noise amplifier with variable gain. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.

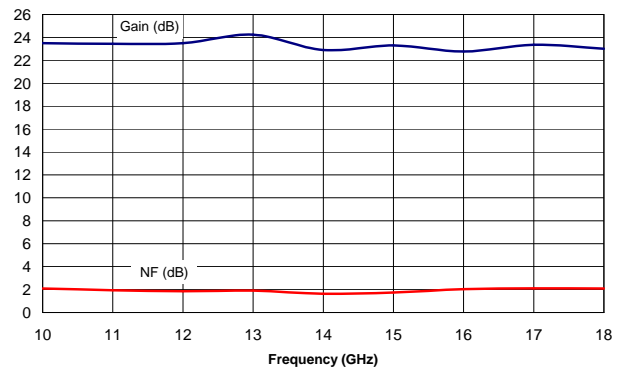
The circuit is manufactured with a pHEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.



Main Features

- Frequency range: 10-18GHz
- 2.2dB Noise Figure.
- 23dB gain
- Gain control range: 25dB
- DC power consumption: 180mA @ 5V
- Chip size: 2.49 X 1.23 X 0.10 mm



Typical on wafer measurements : Gain & NF

Main Characteristics

Tamb. = 25°C

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------|--------------------------------------|-----|-----|-----|------|
| Fop | Operating frequency range | 10 | | 18 | GHz |
| G | Small signal gain | 20 | 23 | | dB |
| NF | Noise figure | | 2.2 | 3 | dB |
| Gctrl | Gain control range with Vc variation | | 25 | | dB |
| Id | Bias current | | 180 | | mA |

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

Electrical Characteristics for Broadband OperationT_{amb} = +25°C, V₅=V_{d2,3,4}= 5V

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------|--|------|-------------------|-------|--------|
| Fop | Operating frequency range | 10 | | 18 | GHz |
| G | Small signal gain (1) | 20 | 23 | | dB |
| ΔG | Small signal gain flatness (1) | | ±1 | | dB |
| Is | Reverse isolation (1) | | 60 | | dB |
| NF | Noise figure with V _c =1.2V (1) | | 2.2 | 3 | dB |
| Gctrl | Gain control range versus V _c | 20 | 25 | | dB |
| P1dB | Output power at 1dB compression with V _c =1.2V | | 10 | | dBm |
| VSWRin | Input VSWR (1) | | | 3.0:1 | |
| VSWRout | Output VSWR (1) | | | 2.5:1 | |
| Vd | DC voltage V ₅ = V _{d2,3,4} V _c | -1.5 | 5 [-0.7, +1.2] | +1.3 | V V |
| Id1 | Bias current (2) with V _c =1.2V | | 25 | | mA |
| Id | Bias current total (3) with V _c =1.2V | | 180 | | mA |

(1) These values are representative of on-wafer measurements that are made without bonding wires at RF ports.

(2) For optimum noise figure, the bias current Id1 should be adjusted to 25mA with Vg1 voltage.

(3) With Id1=25mA, adjust Vg2,3,4 voltage for a total drain current around 180mA.

Absolute Maximum RatingsT_{amb.} = 25°C (1)

| Symbol | Parameter | Values | Unit |
|--------|--|--------------|------|
| Vd | Maximum Drain bias voltage | +5.2 | V |
| Id | Maximum drain bias current | 250 | mA |
| Vg | Gate bias voltage | -2.5 to +0.4 | V |
| Vc | Maximum Control bias voltage | +1.5 | V |
| Vdg | Maximum drain to gate voltage (V _d - V _g) | +5.0 | V |
| Pin | Maximum input power overdrive (2) | +15 | dBm |
| Tch | Maximum channel temperature | +175 | °C |
| Ta | Operating temperature range | -40 to +85 | °C |
| Tstg | Storage temperature range | -55 to +125 | °C |

(1) Operation of this device above any of these parameters may cause permanent damage.

(2) Duration < 1s.

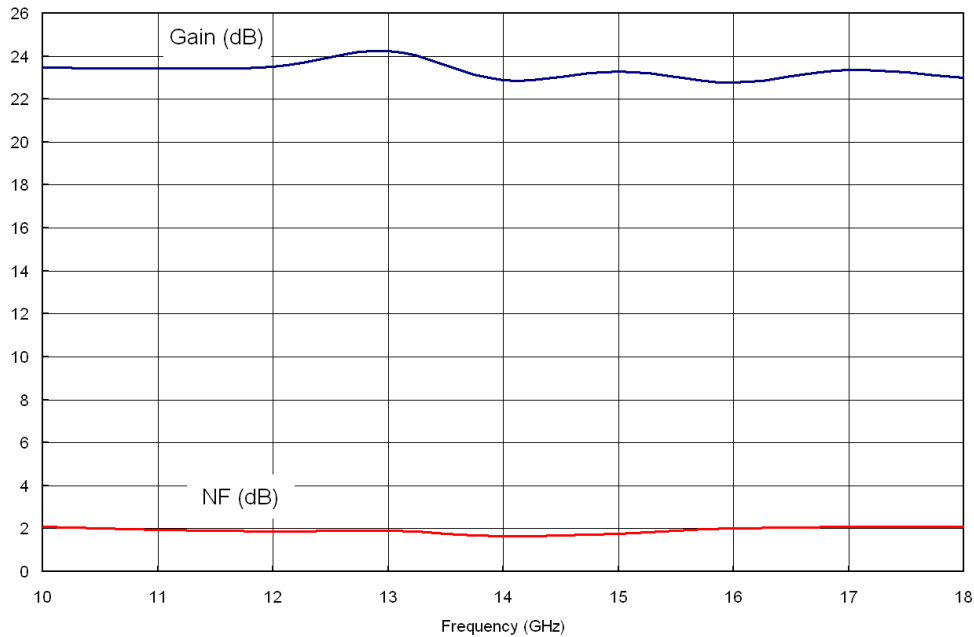
Ref. : DSCHA22917165 - 14 Jun 07

2/8

Specifications subject to change without notice

Typical on wafer Measurements

Bias Conditions: $V_5=V_{d2,3,4}=5V$, V_{g1} for $I_{d1}=25mA$, $V_{g2}=V_{g3,4}=-0.5V$, $V_c=+1.2V$

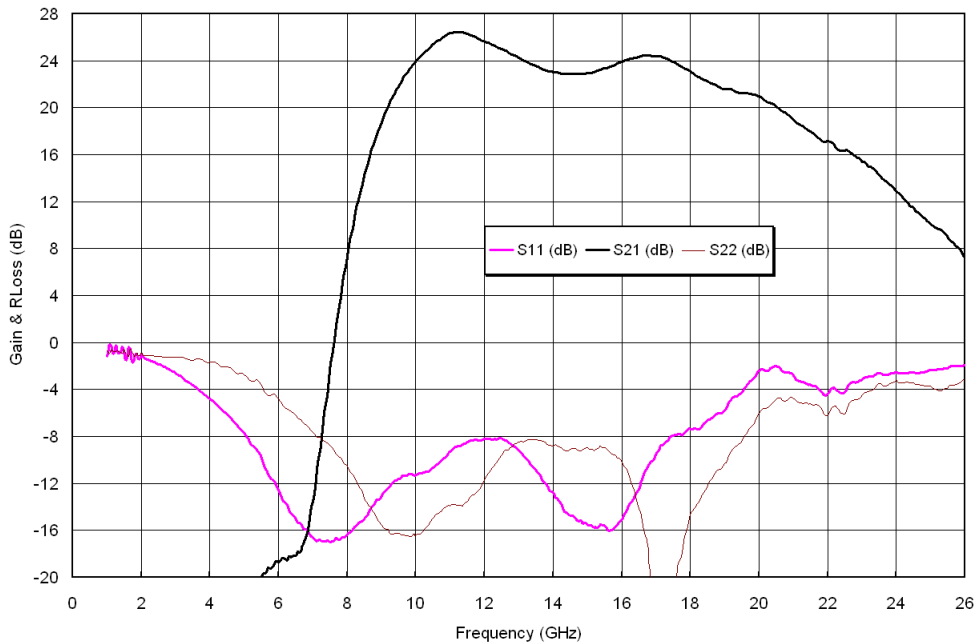


Gain & Noise Figure versus frequency

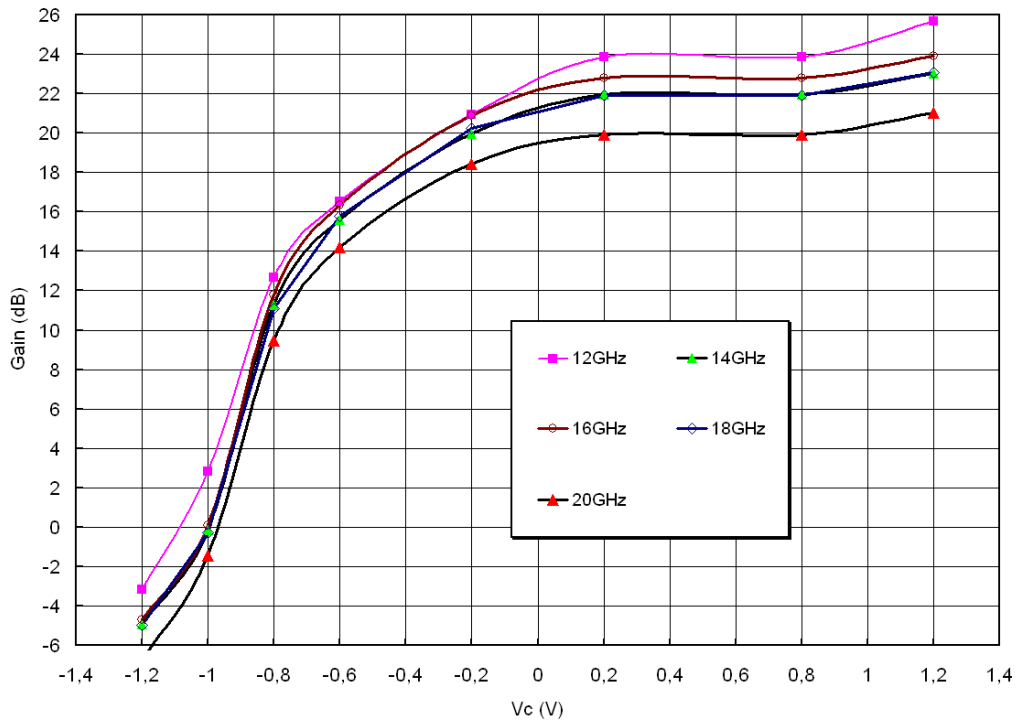
In jig Measurements

All these measurements include the jig losses (about 0.5dB on gain, 0.2dB on noise figure and 0.3dB on output power)

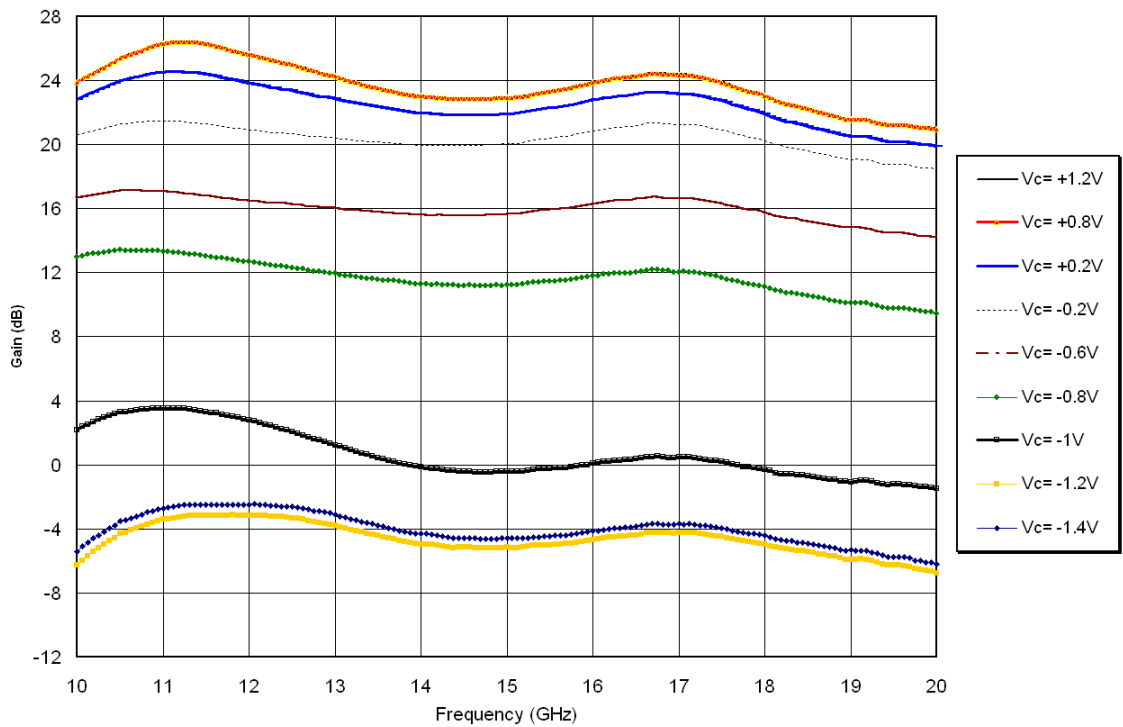
Bias Conditions: $V_5=V_{d2,3,4}=5V$, V_{g1} for $I_{d1}=25mA$, $V_{g2}=V_{g3,4}=-0.5V$, $V_c=+1.2V$



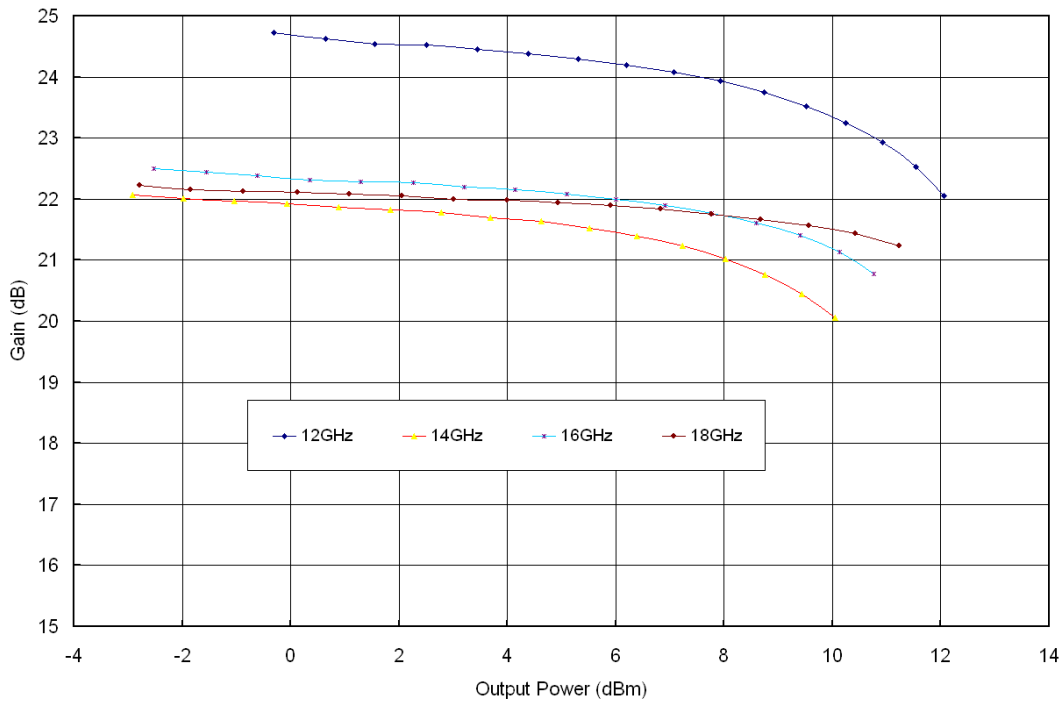
Gain, Return Loss & Noise Figure versus frequency



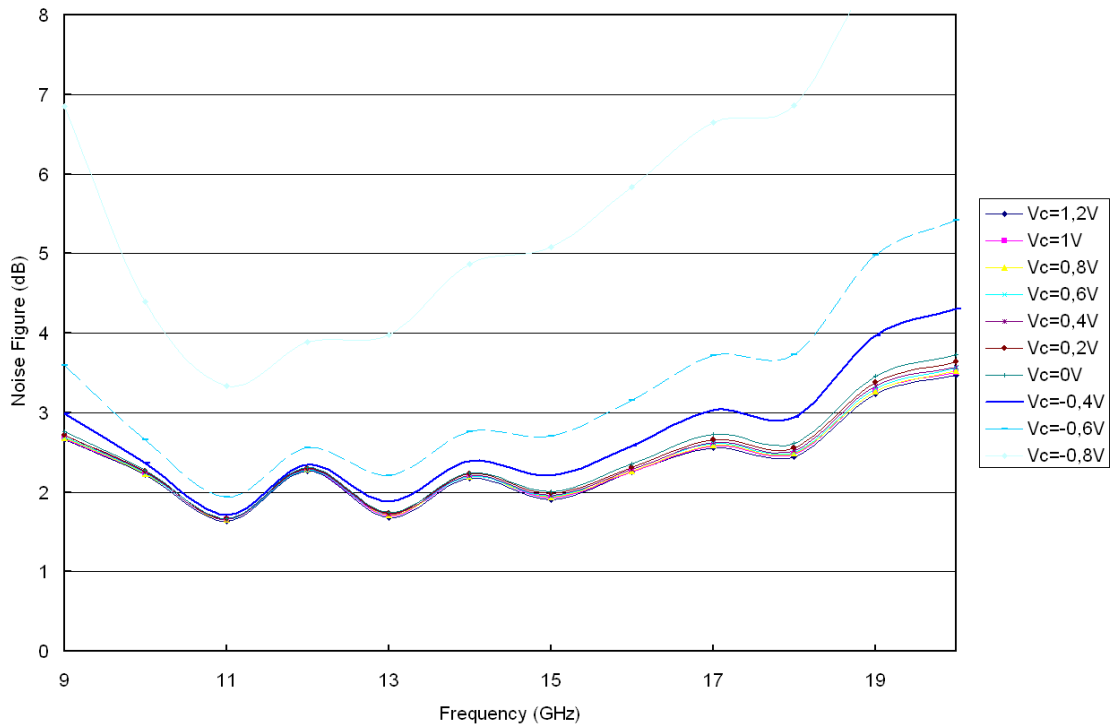
Gain versus Vc



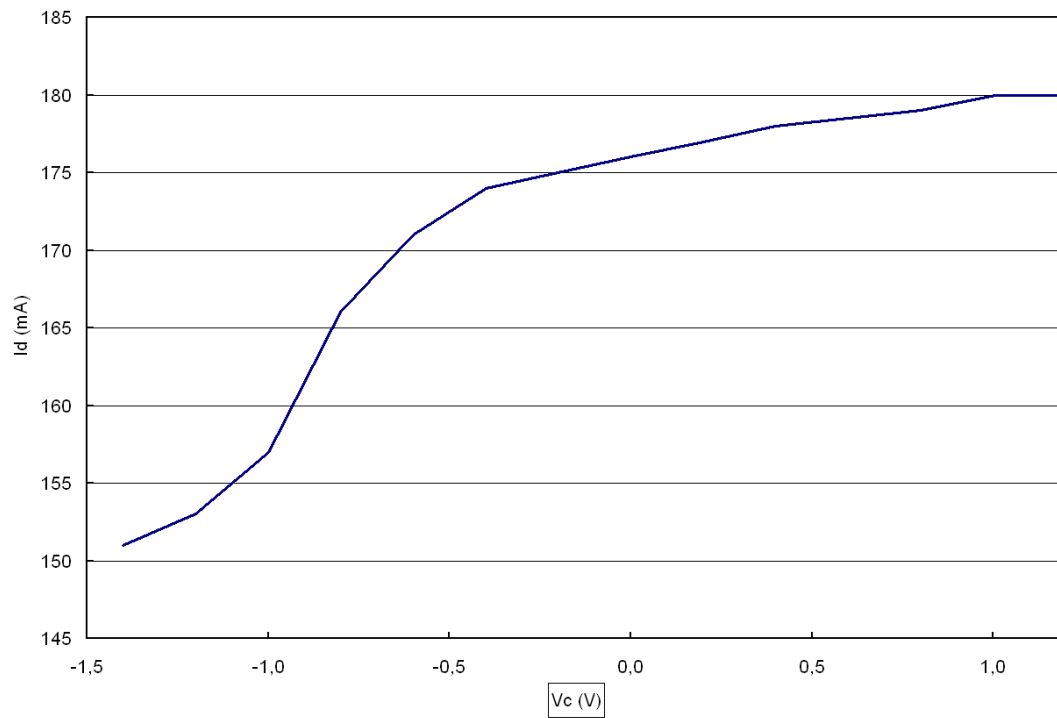
Gain versus Frequency and Vc



Gain versus Output power

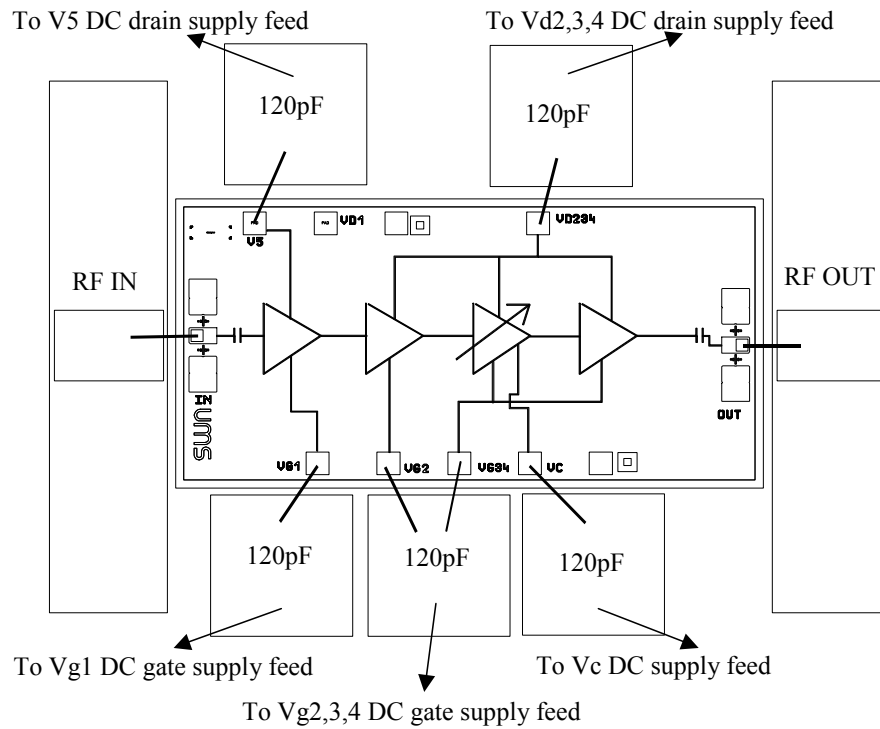


Noise figure versus Frequency and Vc

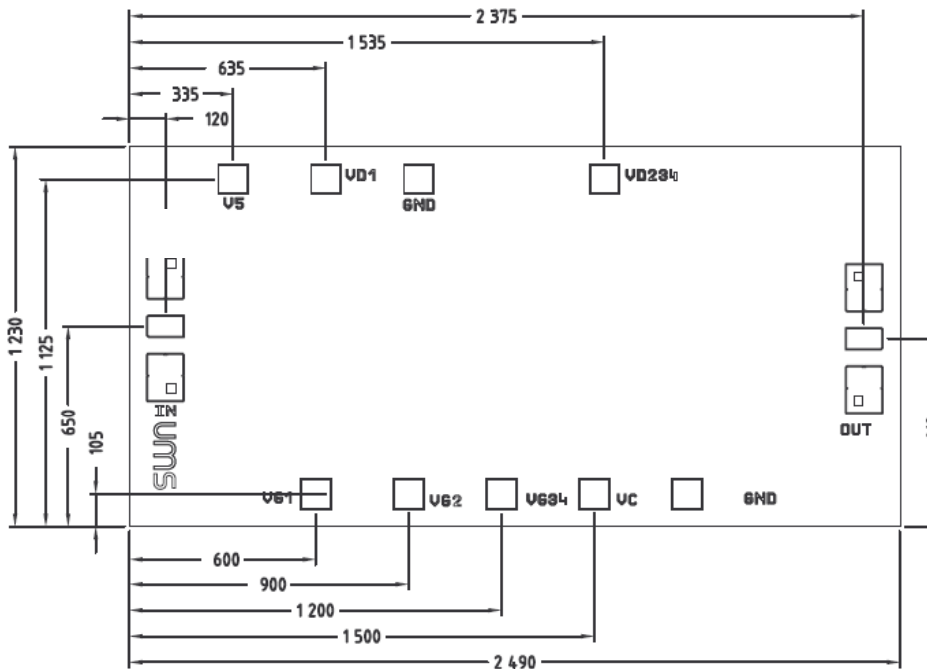


I_d versus V_c (I_d tuned to 180mA with $V_c=+1.2$ V; $V_d=5$ V)

Chip Assembly and Mechanical Data



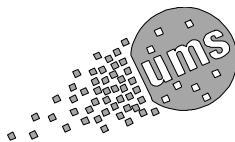
Note: Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended
Bond Pad: 100 x 100 µm



UNITS : µm
Tol : ±35µm

Bonding pad positions

(Chip thickness : 100µm. All dimensions are in micrometers)



Ordering Information

Chip form : CHA2291-99F/00

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.** Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**