TOSHIBA CMOS Digital Integrated Circuit   Silicon Monolithic

TC74VCXR162500FT

Low-Voltage 18-Bit Universal Bus Transceiver with 3.6-V Tolerant Inputs and Outputs

The TC74VCXR162500FT is a high-performance CMOS 18-bit universal bus transceiver. Designed for use in 1.8-V, 2.5-V or 3.3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

It is also designed with overvoltage tolerant inputs and outputs up to 3.6 V.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CKAB}}$ and $\overline{\text{CKBA}}$) inputs.

For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if $\overline{\text{CKAB}}$ is held at a high or low logic level. If LEAB is low, the A bus data is stored in the latch/flip-flop on the high-to-low transition of $\overline{\text{CKAB}}$.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CKBA}}$.

When the $\overline{\text{OE}}$ input is high, the outputs are in a high-impedance state. This device is designed to be used with 3-state memory address drivers, etc.

The 26-Ω series resistor helps reducing output overshoot and undershoot without external resistor.

All inputs are equipped with protection circuits against static discharge.
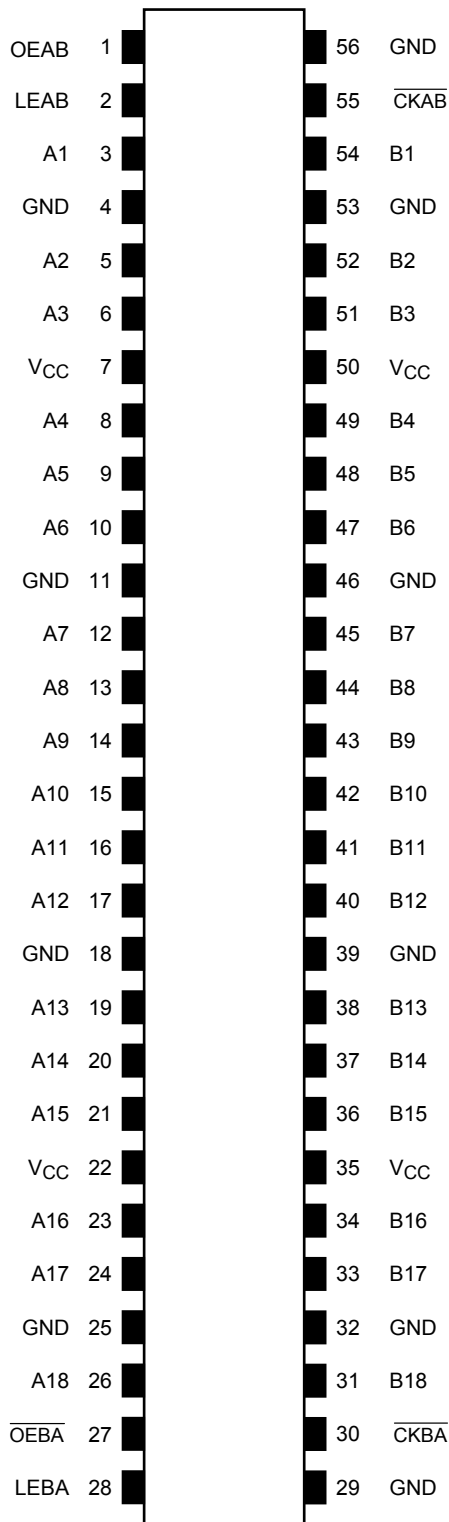

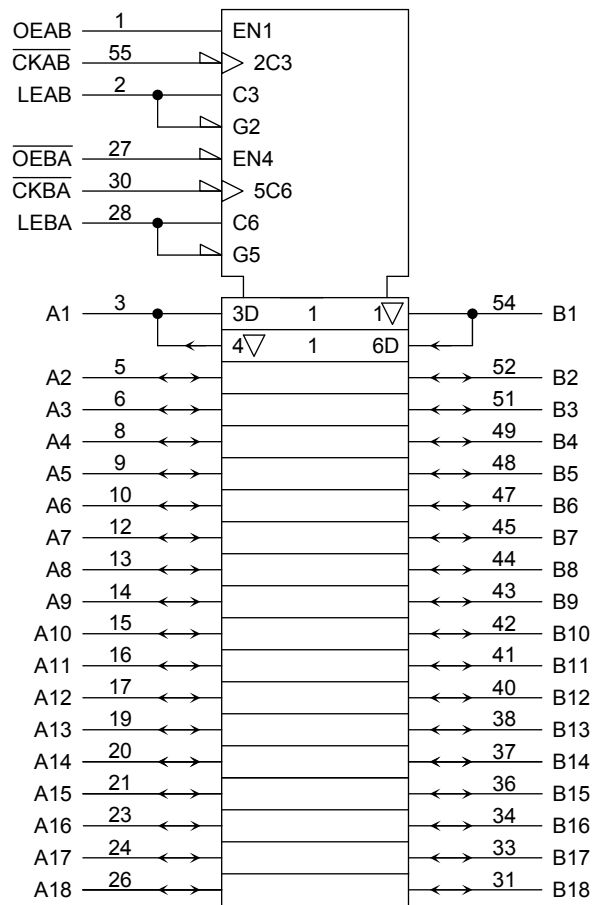TSSOP56-P-0061-0.50A
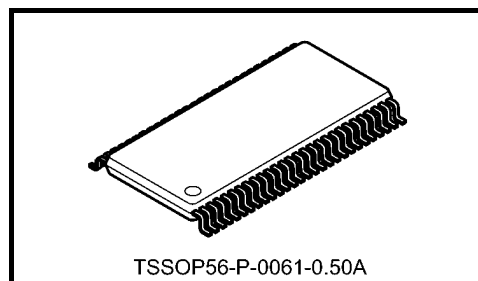
Weight: 0.25 g (typ.)

Features (Note)

- 26-Ω series resistors on outputs
- Low-voltage operation: V_{CC} = 1.8 to 3.6 V
- High-speed operation: t_{pd} = 3.8 ns (max) (V_{CC} = 3.0 to 3.6 V)
  - : t_{pd} = 4.9 ns (max) (V_{CC} = 2.3 to 2.7 V)
  - : t_{pd} = 9.8 ns (max) (V_{CC} = 1.8 V)
- Output current: I_{OH}/I_{OL} = ±12 mA (min) (V_{CC} = 3.0 V)
  - : I_{OH}/I_{OL} = ±8 mA (min) (V_{CC} = 2.3 V)
  - : I_{OH}/I_{OL} = ±4 mA (min) (V_{CC} = 1.8 V)
- Latch-up performance: −300 mA
- ESD performance: Machine model ≥ ±200 V
  - Human body model ≥ ±2000 V
- Package: TSSOP
- Bidirectional interface between 2.5 V and 3.3 V signals.
- 3.6-V tolerant function and power-down protection provided on all inputs and outputs

Note: Do not apply a signal to any bus pins when it is in the output mode. Damage may result.
All floating (high impedance) bus pins must have their input level fixed by means of pull-up or pull-down resistors.

Pin Assignment (top view)

Pin	Name		Pin	Name
1	OEAB		56	GND
2	LEAB		55	$\overline{\text{CKAB}}$
3	A1		54	B1
4	GND		53	GND
5	A2		52	B2
6	A3		51	B3
7	V$_{CC}$		50	V$_{CC}$
8	A4		49	B4
9	A5		48	B5
10	A6		47	B6
11	GND		46	GND
12	A7		45	B7
13	A8		44	B8
14	A9		43	B9
15	A10		42	B10
16	A11		41	B11
17	A12		40	B12
18	GND		39	GND
19	A13		38	B13
20	A14		37	B14
21	A15		36	B15
22	V$_{CC}$		35	V$_{CC}$
23	A16		34	B16
24	A17		33	B17
25	GND		32	GND
26	A18		31	B18
27	$\overline{\text{OEBA}}$		30	$\overline{\text{CKBA}}$
28	LEBA		29	GND

IEC Logic Symbol

Signal	Pin	Label
OEAB	1	EN1
$\overline{\text{CKAB}}$	55	2C3
LEAB	2	C3
		G2
$\overline{\text{OEBA}}$	27	EN4
$\overline{\text{CKBA}}$	30	5C6
LEBA	28	C6
		G5

A	Pin			Pin	B
A1	3	3D 1 1▽	4▽ 1 6D	54	B1
A2	5			52	B2
A3	6			51	B3
A4	8			49	B4
A5	9			48	B5
A6	10			47	B6
A7	12			45	B7
A8	13			44	B8
A9	14			43	B9
A10	15			42	B10
A11	16			41	B11
A12	17			40	B12
A13	19			38	B13
A14	20			37	B14
A15	21			36	B15
A16	23			34	B16
A17	24			33	B17
A18	26			31	B18

TOSHIBA

Truth Table (A bus → B bus)

| Inputs | | | | Outputs |
OEAB	LEAB	$\overline{\text{CKAB}}$	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↘	L	L
H	L	↘	H	H
H	L	H	X	B0 (Note)
H	L	L	X	B0 (Note)

Note: Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CKAB}}$ was low or high before LEAB went low.

Truth Table (B bus → A bus)

| Inputs | | | | Outputs |
$\overline{\text{OEBA}}$	LEBA	$\overline{\text{CKBA}}$	B	A
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↘	L	L
L	L	↘	H	H
L	L	H	X	A0 (Note)
L	L	L	X	A0 (Note)

Note: Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CKBA}}$ was low or high before LEBA went low.

System Diagram

To 17 other channels
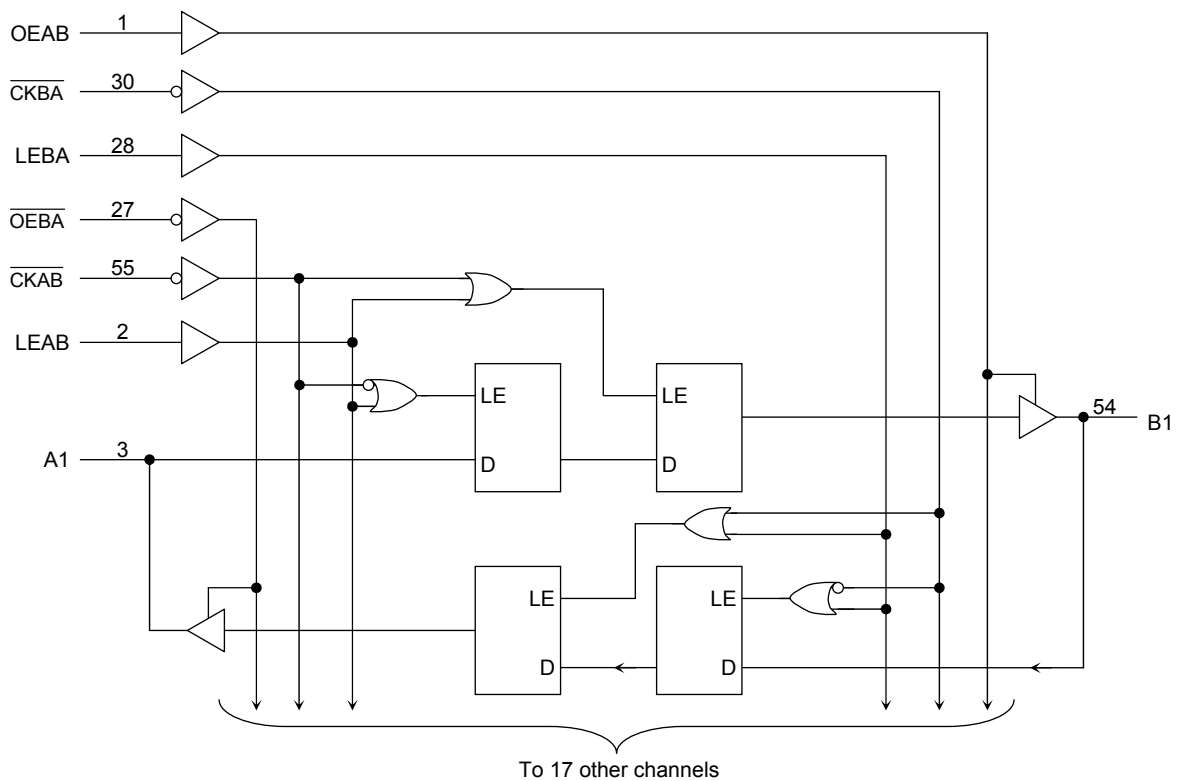
Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to 4.6	V
DC input voltage (OEAB, $\overline{OEBA}$, LEAB, LEBA, $\overline{CKAB}$, $\overline{CKBA}$)	V_{IN}	−0.5 to 4.6	V
DC bus I/O voltage	$V_{I/O}$	−0.5 to 4.6 (Note 2)	V
		−0.5 to V_{CC} + 0.5 (Note 3)	
Input diode current	I_{IK}	−50	mA
Output diode current	I_{OK}	±50 (Note 4)	mA
DC output current	I_{OUT}	±50	mA
Power dissipation	P_D	400	mW
DC V_{CC}/ground current per supply pin	I_{CC}/I_{GND}	±100	mA
Storage temperature	T_{stg}	−65 to 150	°C

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: OFF state

Note 3: High or low state. I_{OUT} absolute maximum rating must be observed.

Note 4: V_{OUT} < GND, V_{OUT} > V_{CC}

Operating Ranges (Note 1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	1.8 to 3.6 1.2 to 3.6 (Note 2)	V
Input voltage (OEAB, $\overline{OEBA}$, LEAB, LEBA, CKAB, CKBA)	V_{IN}	−0.3 to 3.6	V
Bus I/O voltage	$V_{I/O}$	0 to 3.6 (Note 3) 0 to V_{CC} (Note 4)	V
Output current	I_{OH}/I_{OL}	±12 (Note 5) ±8 (Note 6) ±4 (Note 7)	mA
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 10 (Note 8)	ns/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either VCC or GND.

Note 2: Data retention only

Note 3: OFF state

Note 4: High or low state

Note 5: V_{CC} = 3.0 to 3.6 V

Note 6: V_{CC} = 2.3 to 2.7 V

Note 7: V_{CC} = 1.8 V

Note 8: V_{IN} = 0.8 to 2.0 V, V_{CC} = 3.0 V

Electrical Characteristics

DC Characteristics (Ta = −40 to 85°C, 2.7 V < V$_{CC}$ ≦ 3.6 V)

Characteristics		Symbol	Test Condition		V$_{CC}$ (V)	Min	Max	Unit
Input voltage	H-level	V$_{IH}$	—		2.7 to 3.6	2.0	—	V
	L-level	V$_{IL}$	—		2.7 to 3.6	—	0.8	
Output voltage	H-level	V$_{OH}$	V$_{IN}$ = V$_{IH}$ or V$_{IL}$	I$_{OH}$ = −100 μA	2.7 to 3.6	V$_{CC}$ − 0.2	—	V
				I$_{OH}$ = −6 mA	2.7	2.2	—	
				I$_{OH}$ = −8 mA	3.0	2.4	—	
				I$_{OH}$ = −12 mA	3.0	2.2	—	
	L-level	V$_{OL}$	V$_{IN}$ = V$_{IH}$ or V$_{IL}$	I$_{OL}$ = 100 μA	2.7 to 3.6	—	0.2	
				I$_{OL}$ = 6 mA	2.7	—	0.4	
				I$_{OL}$ = 8 mA	3.0	—	0.55	
				I$_{OL}$ = 12 mA	3.0	—	0.8	
Input leakage current		I$_{IN}$	V$_{IN}$ = 0 to 3.6 V		2.7 to 3.6	—	±5.0	μA
3-state output OFF state current		I$_{OZ}$	V$_{IN}$ = V$_{IH}$ or V$_{IL}$ V$_{OUT}$ = 0 to 3.6 V		2.7 to 3.6	—	±10.0	μA
Power-off leakage current		I$_{OFF}$	V$_{IN}$, V$_{OUT}$ = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I$_{CC}$	V$_{IN}$ = V$_{CC}$ or GND		2.7 to 3.6	—	20.0	μA
			V$_{CC}$ ≦ (V$_{IN}$, V$_{OUT}$) ≦ 3.6 V		2.7 to 3.6	—	±20.0	
Increase in I$_{CC}$ per input		ΔI$_{CC}$	V$_{IH}$ = V$_{CC}$ − 0.6 V		2.7 to 3.6	—	750	

DC Characteristics (Ta = −40 to 85°C, 2.3 V ≦ V$_{CC}$ ≦ 2.7 V)

Characteristics		Symbol	Test Condition		V$_{CC}$ (V)	Min	Max	Unit
Input voltage	H-level	V$_{IH}$	—		2.3 to 2.7	1.6	—	V
	L-level	V$_{IL}$	—		2.3 to 2.7	—	0.7	
Output voltage	H-level	V$_{OH}$	V$_{IN}$ = V$_{IH}$ or V$_{IL}$	I$_{OH}$ = −100 μA	2.3 to 2.7	V$_{CC}$ − 0.2	—	V
				I$_{OH}$ = −4 mA	2.3	2.0	—	
				I$_{OH}$ = −6 mA	2.3	1.8	—	
				I$_{OH}$ = −8 mA	2.3	1.7	—	
	L-level	V$_{OL}$	V$_{IN}$ = V$_{IH}$ or V$_{IL}$	I$_{OL}$ = 100 μA	2.3 to 2.7	—	0.2	
				I$_{OL}$ = 6 mA	2.3	—	0.4	
				I$_{OL}$ = 8 mA	2.3	—	0.6	
Input leakage current		I$_{IN}$	V$_{IN}$ = 0 to 3.6 V		2.3 to 2.7	—	±5.0	μA
3-state output OFF state current		I$_{OZ}$	V$_{IN}$ = V$_{IH}$ or V$_{IL}$ V$_{OUT}$ = 0 to 3.6 V		2.3 to 2.7	—	±10.0	μA
Power-off leakage current		I$_{OFF}$	V$_{IN}$, V$_{OUT}$ = 0 to 3.6 V		0	—	10.0	μA
Quiescent supply current		I$_{CC}$	V$_{IN}$ = V$_{CC}$ or GND		2.3 to 2.7	—	20.0	μA
			V$_{CC}$ ≦ (V$_{IN}$, V$_{OUT}$) ≦ 3.6 V		2.3 to 2.7	—	±20.0	

DC Characteristics (Ta = −40 to 85°C, 1.8 V ≦ V_{CC} < 2.3 V)

Characteristics		Symbol	Test Condition		V_{CC} (V)	Min	Max	Unit
Input voltage	H-level	V_{IH}	—		1.8 to 2.3	0.7 × V_{CC}	—	V
	L-level	V_{IL}	—		1.8 to 2.3	—	0.2 × V_{CC}	
Output voltage	H-level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100$ μA	1.8	V_{CC} − 0.2	—	V
				$I_{OH} = -4$ mA	1.8	1.4	—	
	L-level	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 100$ μA	1.8	—	0.2	
				$I_{OL} = 4$ mA	1.8	—	0.3	
Input leakage current		I_{IN}	$V_{IN} = 0$ to 3.6 V		1.8	—	±5.0	μA
3-state output OFF state current		I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = 0$ to 3.6 V		1.8	—	±10.0	μA
Power-off leakage current		I_{OFF}	$V_{IN}, V_{OUT} = 0$ to 3.6 V		0	—	10.0	μA
Quiescent supply current		I_{CC}	$V_{IN} = V_{CC}$ or GND		1.8	—	20.0	μA
			$V_{CC} ≦ (V_{IN}, V_{OUT}) ≦ 3.6$ V		1.8	—	±20.0	

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AC Characteristics (Ta = −40 to 85°C, input: $t_r = t_f$ = 2.0 ns, C_L = 30 pF, R_L = 500 Ω) (Note 1)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit
Maximum clock frequency	f_{max}	Figure 1, Figure 3	1.8	100	—	MHz
			2.5 ± 0.2	200	—	
			3.3 ± 0.3	250	—	
Propagation delay time (An, Bn-Bn, An)	t_{pLH} t_{pHL}	Figure 1, Figure 2	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	4.9	
			3.3 ± 0.3	0.6	3.8	
Propagation delay time ($\overline{CKAB}$, $\overline{CLKBA}$ -Bn, An)	t_{pLH} t_{pHL}	Figure 1, Figure 3	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	6.7	
			3.3 ± 0.3	0.6	5.1	
Propagation delay time (LEAB, LEBA-Bn, An)	t_{pLH} t_{pHL}	Figure 1, Figure 4	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	6.3	
			3.3 ± 0.3	0.6	4.7	
Output enable time (OEAB, $\overline{OEBA}$ -Bn, An)	t_{pZL} t_{pZH}	Figure 1, Figure 5, Figure 6	1.8	1.5	9.8	ns
			2.5 ± 0.2	0.8	5.9	
			3.3 ± 0.3	0.6	4.3	
Output disable time (OEAB, $\overline{OEBA}$ -Bn, An)	t_{pLZ} t_{pHZ}	Figure 1, Figure 5, Figure 6	1.8	1.5	8.8	ns
			2.5 ± 0.2	0.8	4.9	
			3.3 ± 0.3	0.6	4.3	
Minimum pulse width	$t_{W (H)}$ $t_{W (L)}$	Figure 1, Figure 3, Figure 4	1.8	4.0	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum setup time	t_s	Figure 1, Figure 3, Figure 4	1.8	2.5	—	ns
			2.5 ± 0.2	1.5	—	
			3.3 ± 0.3	1.5	—	
Minimum hold time	t_h	Figure 1, Figure 3, Figure 4	1.8	1.0	—	ns
			2.5 ± 0.2	1.0	—	
			3.3 ± 0.3	1.0	—	
Output to output skew	t_{osLH} t_{osHL}	(Note 2)	1.8	—	0.5	ns
			2.5 ± 0.2	—	0.5	
			3.3 ± 0.3	—	0.5	

Note 1: For C_L = 50 pF, add approximately 300 ps to the AC maximum specification.

Note 2: Parameter guaranteed by design.
 (t_{osLH} = |t_{pLHm} − t_{pLHn}|, t_{osHL} = |t_{pHLm} − t_{pHLn}|)

Dynamic Switching Characteristics
(Ta = 25°C, input: t_r = t_f = 2.0 ns, C_L = 30 pF, R_L = 500 Ω)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Typ.	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	V_{IH} = 1.8 V, V_{IL} = 0 V	(Note)	1.8	0.15	V
		V_{IH} = 2.5 V, V_{IL} = 0 V	(Note)	2.5	0.25	
		V_{IH} = 3.3 V, V_{IL} = 0 V	(Note)	3.3	0.35	
Quiet output minimum dynamic V_{OL}	V_{OLV}	V_{IH} = 1.8 V, V_{IL} = 0 V	(Note)	1.8	−0.15	V
		V_{IH} = 2.5 V, V_{IL} = 0 V	(Note)	2.5	−0.25	
		V_{IH} = 3.3 V, V_{IL} = 0 V	(Note)	3.3	−0.35	
Quiet output minimum dynamic V_{OH}	V_{OHV}	V_{IH} = 1.8 V, V_{IL} = 0 V	(Note)	1.8	1.55	V
		V_{IH} = 2.5 V, V_{IL} = 0 V	(Note)	2.5	2.05	
		V_{IH} = 3.3 V, V_{IL} = 0 V	(Note)	3.3	2.65	

Note: Parameter guaranteed by design.

Capacitive Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition		V_{CC} (V)	Typ.	Unit
Input capacitance	C_{IN}	—		1.8, 2.5, 3.3	6	pF
Bus I/O capacitance	$C_{I/O}$	—		1.8, 2.5, 3.3	7	pF
Power dissipation capacitance	C_{PD}	f_{IN} = 10 MHz	(Note)	1.8, 2.5, 3.3	20	pF

Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/18 \text{ (per bit)}$$

AC Test Circuit

Figure 1
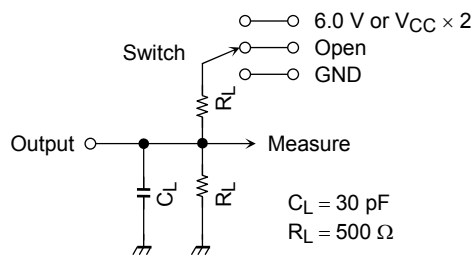
Parameter	Switch	
t_{pLH}, t_{pHL}	Open	
t_{pLZ}, t_{pZL}	6.0 V $V_{CC} \times 2$	@V_{CC} = 3.3 ± 0.3 V @V_{CC} = 2.5 ± 0.2 V @V_{CC} = 1.8 V
t_{pHZ}, t_{pZH}	GND	

AC Waveform
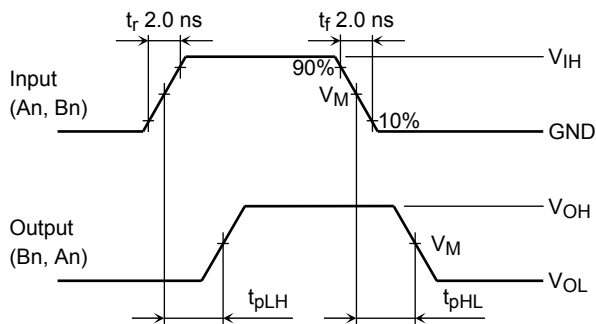
Figure 2 t_{pLH}, t_{pHL}

Symbol	V_{CC}		
	3.3 ± 0.3 V	2.5 ± 0.2 V	1.8 V
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_M	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_X	V_{OL} + 0.3 V	V_{OL} + 0.15 V	V_{OL} + 0.15 V
V_Y	V_{OH} − 0.3 V	V_{OH} − 0.15 V	V_{OH} − 0.15 V
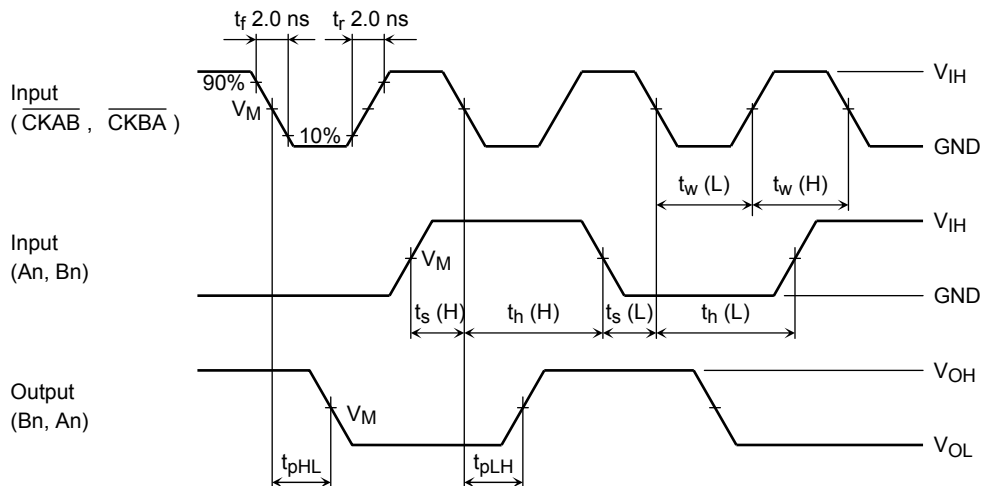
Figure 3 t_{pLH}, t_{pHL}, t_w, t_s, t_h
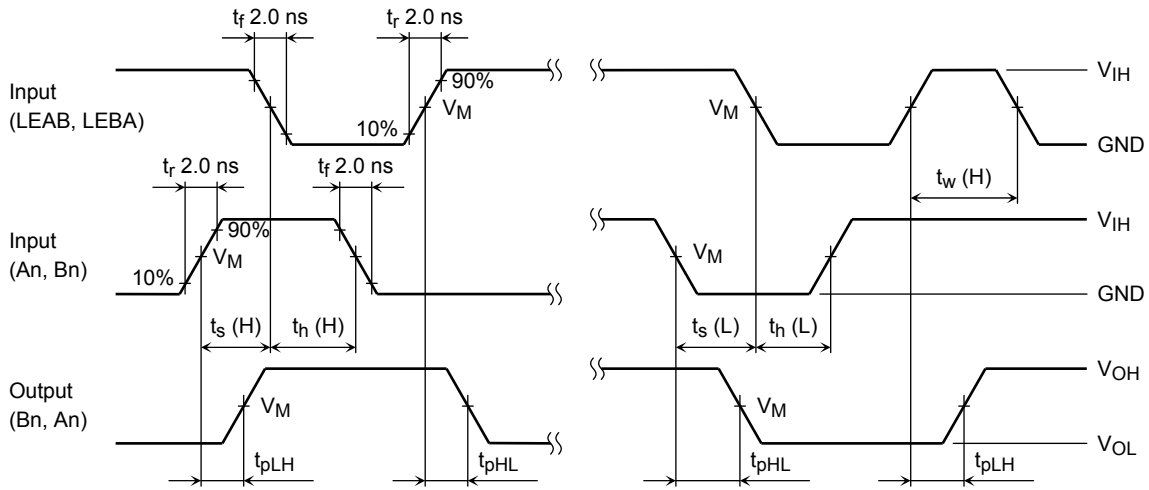
Figure 4 t_{pLH}, t_{pHL}, t_w, t_s, t_h
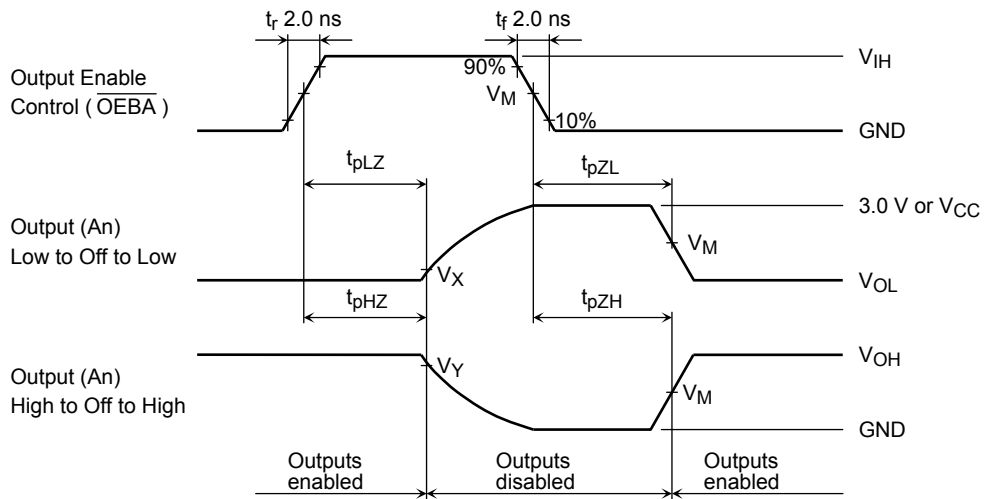
Figure 5 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}
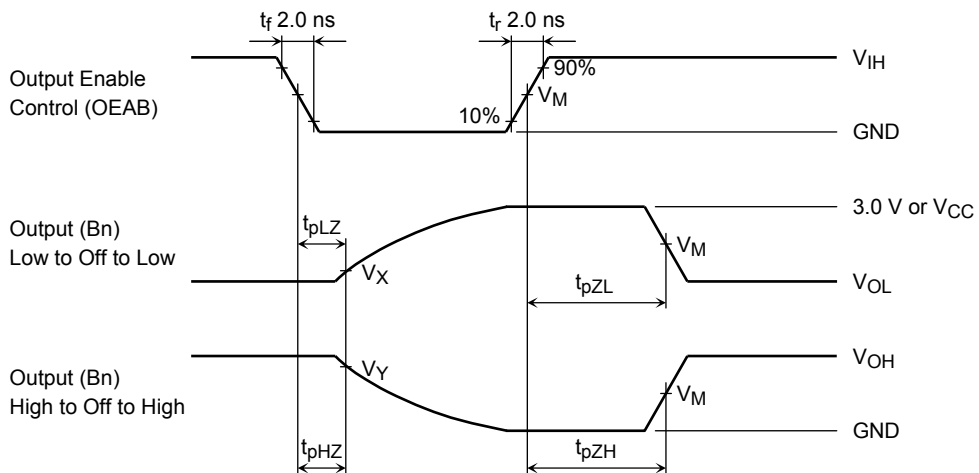
Figure 6 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

Package Dimensions

TSSOP56-P-0061-0.50A   Unit: mm

56   29

6.1±0.1
8.1±0.2

1   28

0.25TYP   0.5   0.2 $^{+0.07}_{-0.06}$ ⊕ 0.1 Ⓜ

14.3MAX

14.0±0.1

0.125 $^{+0.03}_{-0.01}$ 0~10°   0.25

(0.5)

0.45~0.75

1.2MAX

�\0.1

0.1±0.05   1.0±0.05
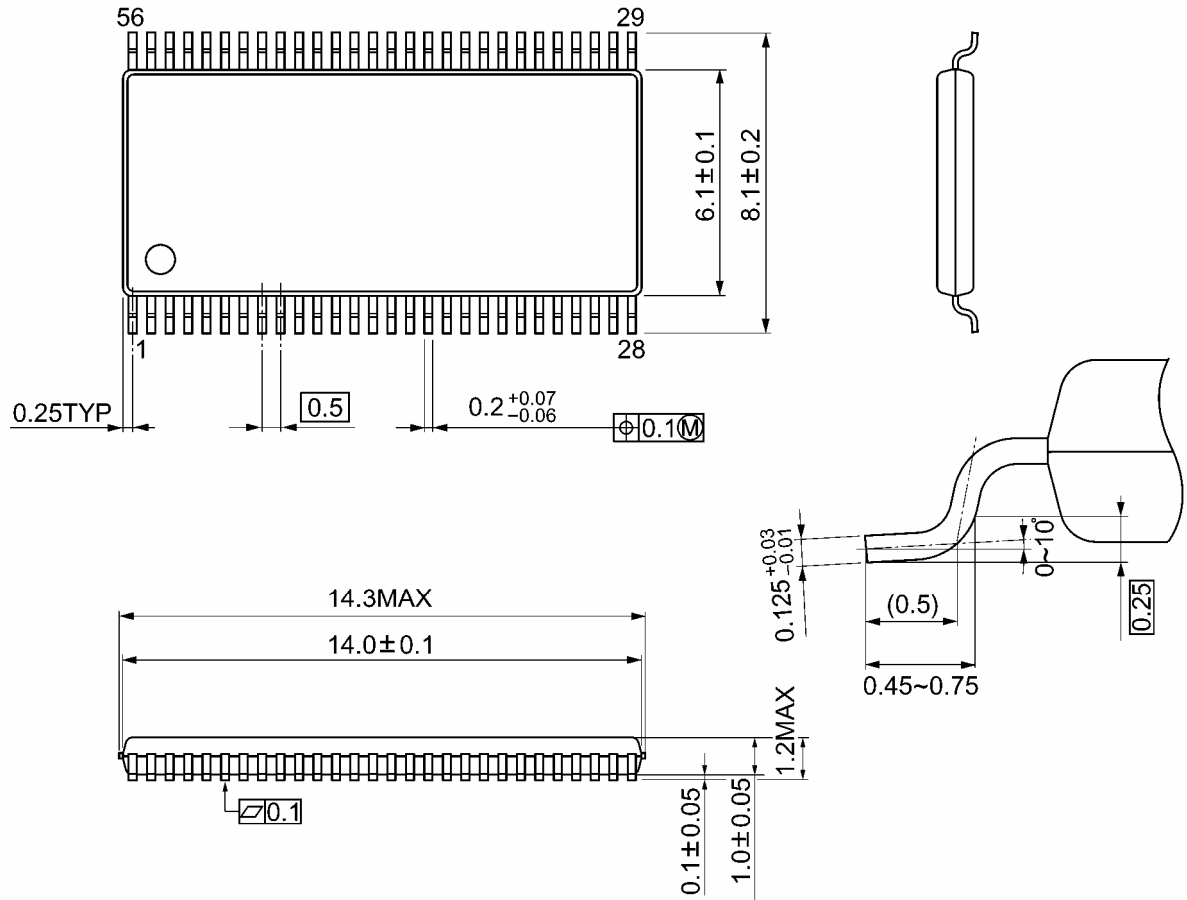
Weight: 0.25 g (typ.)

RESTRICTIONS ON PRODUCT USE

2007-10-19