BLF574

HF / VHF power LDMOS transistor

Rev. 01 — 8 December 2008 | Preliminary data sheet

1. Product profile

1.1 General description

A 500 W to 600 W LDMOS power transistor for broadcast applications and industrial applications in the HF to 500 MHz band.

Table 1. Application information

Mode of operation	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW	225	50	500	26.5	70
	108	50	600	27.5	73

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

- Typical CW performance at frequency of 225 MHz, a supply voltage of 50 V and an I_{Dq} of 1000 mA:
  - Average output power = 500 W
  - Power gain = 26.5 dB
  - Efficiency = 70 %
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (10 MHz to 500 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

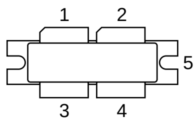
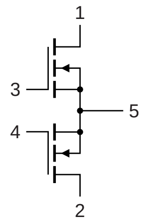
1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

founded by Philips

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF574	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
V_{GS}	gate-source voltage		–0.5	+11	V
I_D	drain current		-	56	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 400 W	0.23	K/W

[1] $R_{th(j-c)}$ is measured under RF conditions.

6. Characteristics

Table 6. DC characteristics

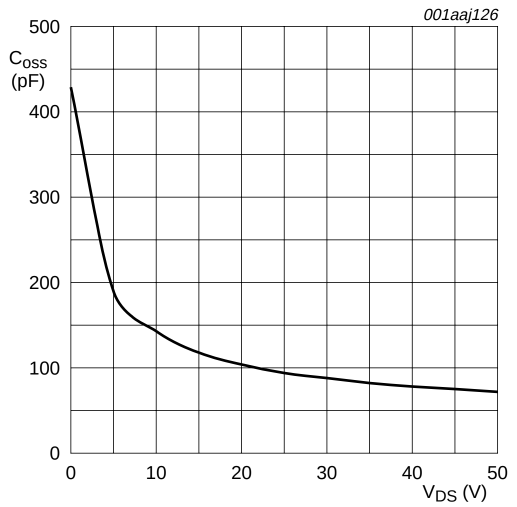
T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 2.5 mA	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 250 mA	1.25	1.7	2.25	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 500 mA	1.35	1.85	2.35	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	29	37.5	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 12.5 A	-	17	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 8.33 A	-	0.14	-	Ω
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	1.5	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	204	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	72	-	pF

Table 7. RF characteristics

Mode of operation: CW; f = 225 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 1000 mA for total device; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 400 W	25	26.5	28	dB
RL_{in}	input return loss	P_L = 400 W	13	20	-	dB
η_D	drain efficiency	P_L = 400 W	66	70	-	%



V_{GS} = 0 V; f = 1 MHz.

Fig 1. Output capacitance as a function of drain-source voltage; typical values per section

6.1 Ruggedness in class-AB operation

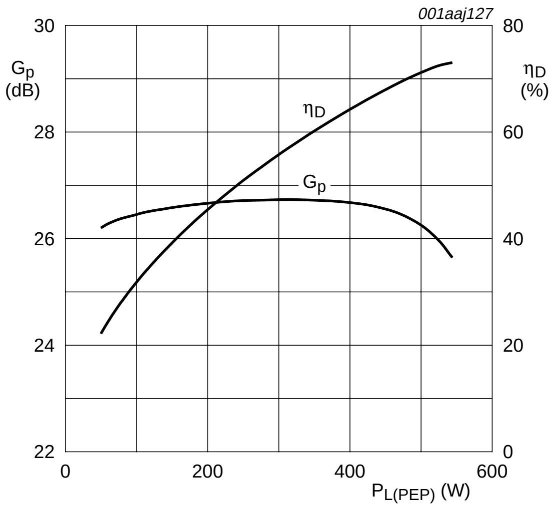
The BLF574 is capable of withstanding a load mismatch corresponding to VSWR = 13 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 1000 mA; P_L = 400 W; f = 225 MHz.

7. Application information

7.1 RF performance

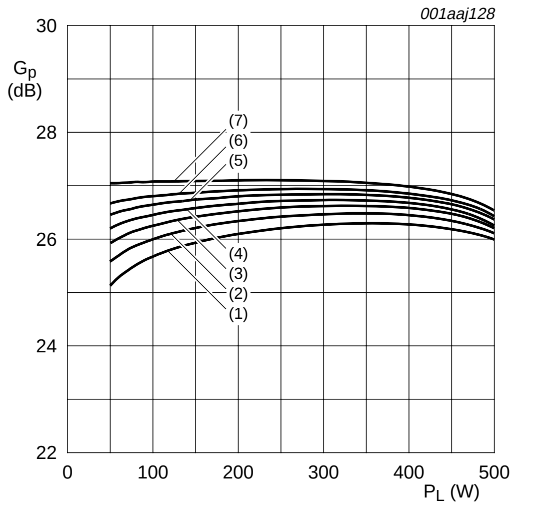
RF performance in a 500 W application circuit at 225 MHz.

7.1.1 1-Tone CW



V_{DS} = 50 V; I_{Dq} = 1000 mA; f = 225 MHz.

Fig 2. Power gain and drain efficiency as functions of load power; typical values



V_{DS} = 50 V; f = 225 MHz.

(1) I_{Dq} = 400 mA

(2) I_{Dq} = 600 mA

(3) I_{Dq} = 800 mA

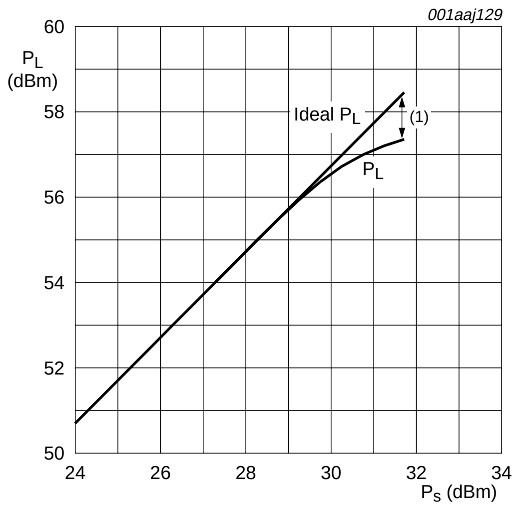
(4) I_{Dq} = 1000 mA

(5) I_{Dq} = 1200 mA

(6) I_{Dq} = 1400 mA

(7) I_{Dq} = 1800 mA

Fig 3. Power gain as function of load power; typical values

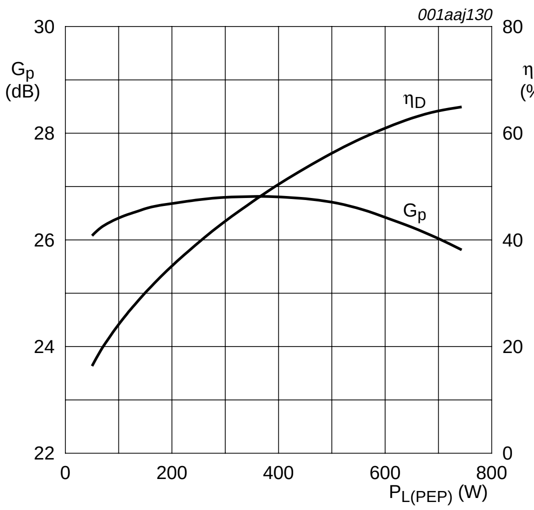


V_{DS} = 50 V; I_{Dq} = 1000 mA; f = 225 MHz.

(1) $P_{L(1dB)}$ = 57.32 dBm (540 W)

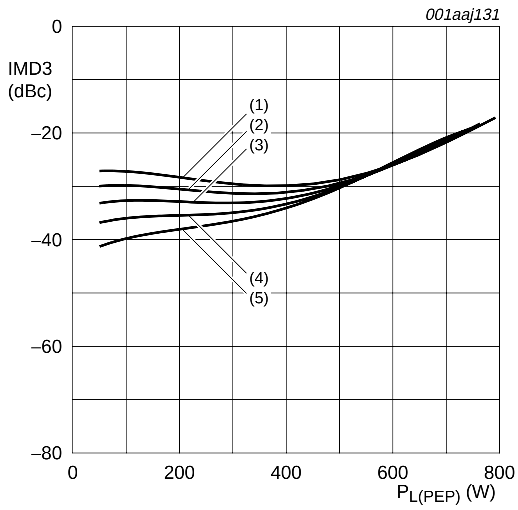
Fig 4. Load power as function of source power; typical values

7.1.2 2-Tone CW



V_{DS} = 50 V; I_{Dq} = 1000 mA; f_1 = 224.95 MHz; f_2 = 225.05 MHz.

Fig 5. Power gain and drain efficiency as functions of peak envelope load power; typical values



V_{DS} = 50 V; f_1 = 224.95 MHz; f_2 = 225.05 MHz.

(1) I_{Dq} = 600 mA

(2) I_{Dq} = 800 mA

(3) I_{Dq} = 1000 mA

(4) I_{Dq} = 1200 mA

(5) I_{Dq} = 1400 mA

Fig 6. Third order intermodulation distortion as a function of peak envelope load power; typical values

7.1.3 Application circuit

Table 8. List of components

For application circuit, see Figure 7.

Printed-Circuit Board (PCB): Rogers 5880; ε_r = 2.2 F/m; height = 0.79 mm; Cu (top/bottom metallization); thickness copper plating = 35 µm.

Component	Description	Value		Remarks
C1, C2, C23, C24	multilayer ceramic chip capacitor	100 pF	[1]	
C3	multilayer ceramic chip capacitor	24 pF	[1]	
C4,C5	multilayer ceramic chip capacitor	39 pF	[1]	
C6, C9	multilayer ceramic chip capacitor	4.7 µF		TDK4532X7R1E475Mt020U
C7, C8, C10, C11	multilayer ceramic chip capacitor	1 nF	[1]	
C12, C16	electrolytic capacitor	220 µF; 63 V		
C13, C15	multilayer ceramic chip capacitor	62 pF	[1]	
C14	multilayer ceramic chip capacitor	15 pF	[1]	
C17, C19	multilayer ceramic chip capacitor	47 pF	[1]	
C18	multilayer ceramic chip capacitor	33 pF	[1]	
C20, C22	multilayer ceramic chip capacitor	10 pF	[1]	
C21	multilayer ceramic chip capacitor	18 pF	[1]	
L1, L2, L3, L4	3 turns 1 mm copper wire	D = 3 mm; length = 3 mm		
L5, L6	stripline	-		(L × W) 125 mm × 7 mm
L7, L8, L9, L10	stripline	-		(L × W) 8 mm × 15 mm
L11, L12	stripline	-		(L × W) 132 mm × 7 mm
R1, R2	metal film resistor	10 Ω; 0.6 W		
R3, R4	metal film resistor	3 Ω; 0.6 W		
T1, T2, T3, T4	semi rigid coax	50 Ω; 120 mm		EZ-141-AL-TP-M17

[1] American Technical Ceramics type 100B or capacitor of same quality.

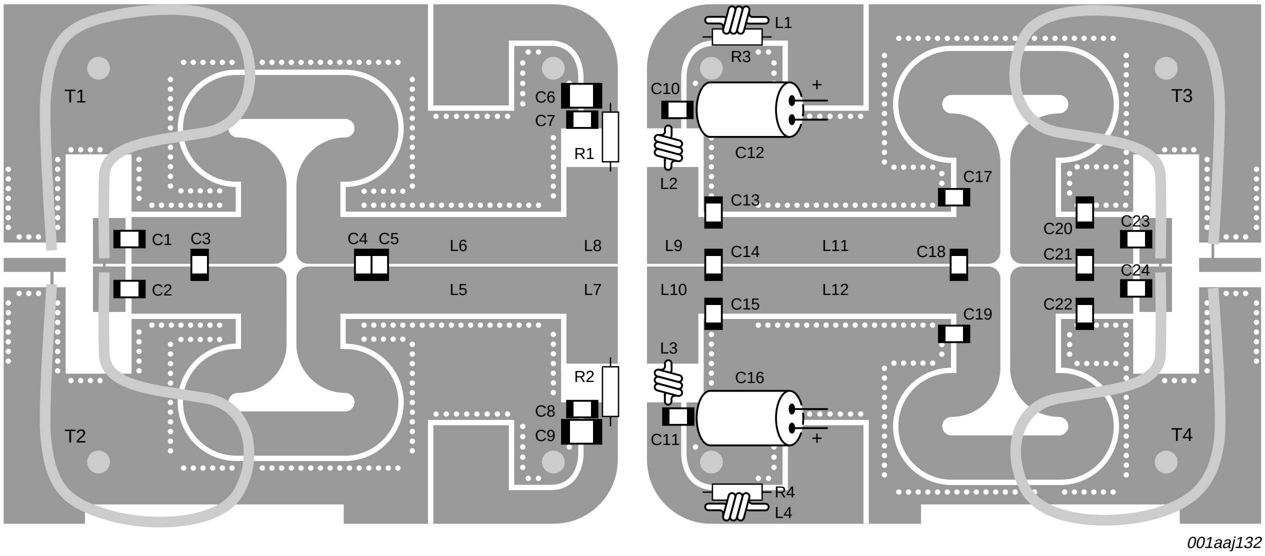
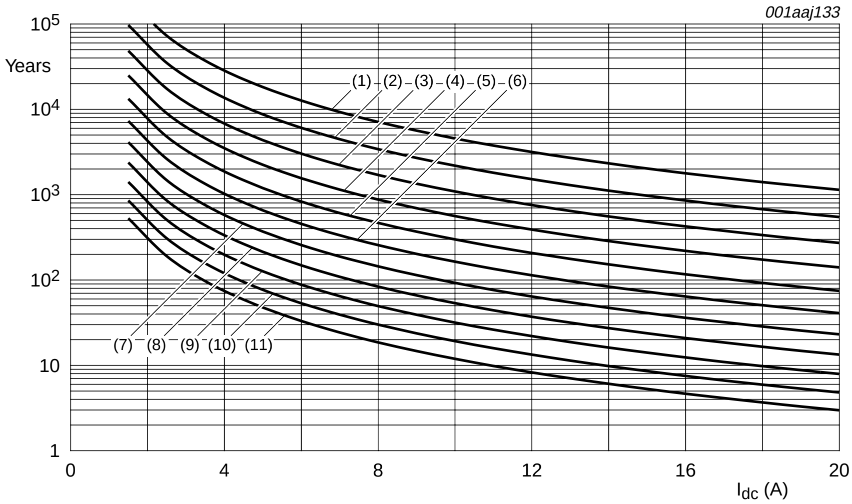


Fig 7. Component layout for class-AB application circuit

7.2 Reliability



TTF (0.1 % failure fraction).

(1) T_j = 100 °C

(2) T_j = 110 °C

(3) T_j = 120 °C

(4) T_j = 130 °C

(5) T_j = 140 °C

(6) T_j = 150 °C

(7) T_j = 160 °C

(8) T_j = 170 °C

(9) T_j = 180 °C

(10) T_j = 190 °C

(11) T_j = 200 °C

Fig 8. BLF574 electromigration (I_D, total device)

8. Test information

8.1 Impedance information

Table 9. Typical impedance

Simulated Z_S and Z_L test circuit impedances.

f MHz	Z_S Ω	Z_L Ω
225	3.2 + j2.5	7.5 + j4.0

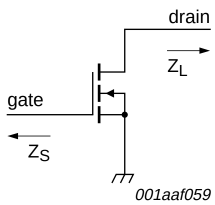
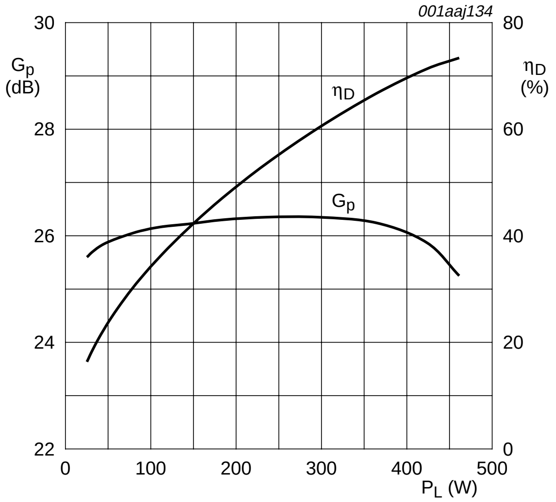


Fig 9. Definition of transistor impedance

8.2 RF performance

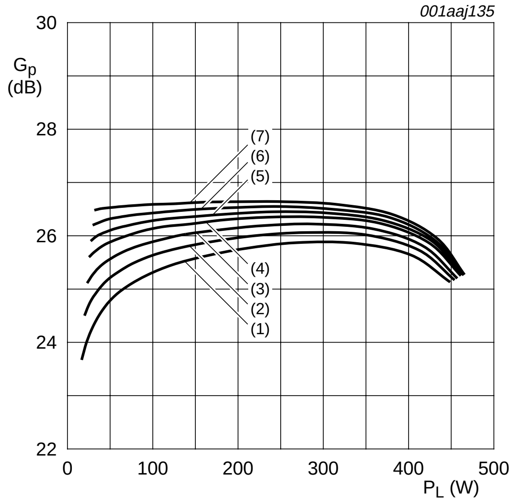
The following figures are measured in a class-AB production test circuit.

8.2.1 1-Tone CW



V_{DS} = 50 V; I_{Dq} = 1000 mA; f = 225 MHz.

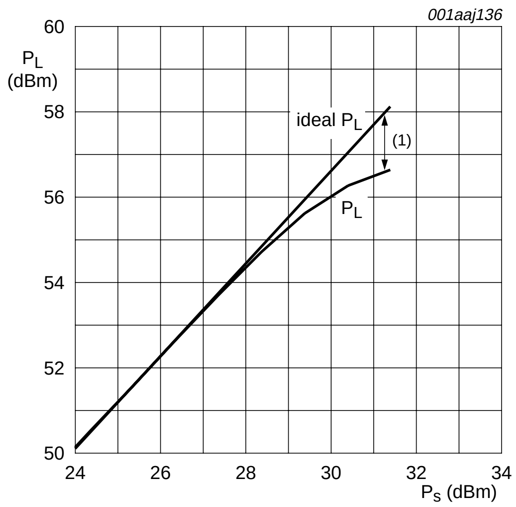
Fig 10. Power gain and drain efficiency as functions of load power; typical values



V_{DS} = 50 V; f = 225 MHz.

(1) I_{Dq} = 400 mA
(2) I_{Dq} = 600 mA
(3) I_{Dq} = 800 mA
(4) I_{Dq} = 1000 mA
(5) I_{Dq} = 1200 mA
(6) I_{Dq} = 1400 mA
(7) I_{Dq} = 1800 mA

Fig 11. Power gain as function of load power; typical values

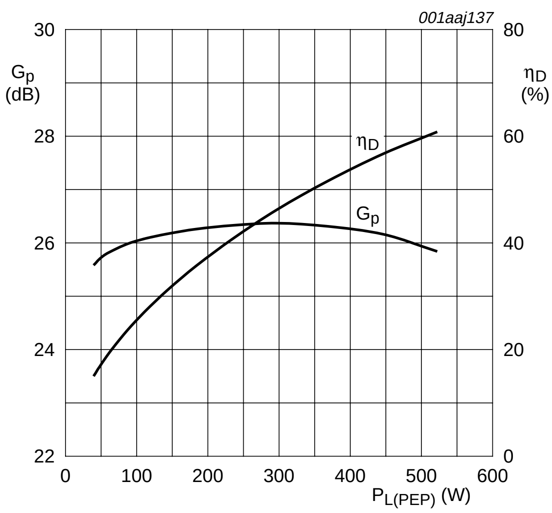


V_{DS} = 50 V; I_{Dq} = 1000 mA; f = 225 MHz.

(1) $P_{L(1dB)}$ = 56.43 dBm (440 W)

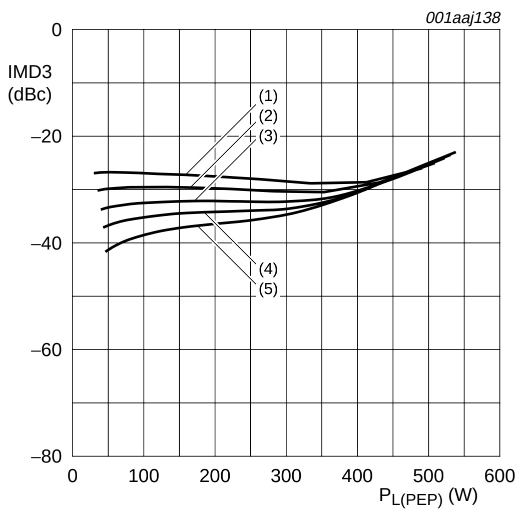
Fig 12. Load power as function of source power; typical values

8.2.2 2-Tone CW



V_{DS} = 50 V; I_{Dq} = 1000 mA; f_1 = 224.95 MHz; f_2 = 225.05 MHz.

Fig 13. Power gain and drain efficiency as functions of peak envelope load power; typical values



V_{DS} = 50 V; f_1 = 224.95 MHz; f_2 = 225.05 MHz.

(1) I_{Dq} = 600 mA

(2) I_{Dq} = 800 mA

(3) I_{Dq} = 1000 mA

(4) I_{Dq} = 1200 mA

(5) I_{Dq} = 1400 mA

Fig 14. Third order intermodulation distortion as a function of peak envelope load power; typical values

8.2.3 Test circuit

Table 10. List of components

For production test circuit, see Figure 15 and Figure 16.
Printed-Circuit Board (PCB): Rogers 5880; ε_r = 2.2 F/m; height = 0.79 mm; Cu (top/bottom metallization); thickness copper plating = 35 µm.

Component	Description	Value		Remarks
C1, C2, C20, C21	multilayer ceramic chip capacitor	100 pF	[1]	
C3	multilayer ceramic chip capacitor	24 pF	[1]	
C4,C5	multilayer ceramic chip capacitor	39 pF	[1]	
C6, C7, C10, C11	multilayer ceramic chip capacitor	1 nf	[1]	
C8, C9	multilayer ceramic chip capacitor	4.7 µF	[1]	TDK4532X7R1E475Mt020U
C12, C13	electrolytic capacitor	220 µF; 63 V		
C14, C15	multilayer ceramic chip capacitor	47 pf	[1]	
C16	multilayer ceramic chip capacitor	33 pF	[1]	
C17	multilayer ceramic chip capacitor	18 pF	[1]	
C18, C19	multilayer ceramic chip capacitor	10 pF	[1]	
C22	multilayer ceramic chip capacitor	15 pF	[1]	
C23, C24	multilayer ceramic chip capacitor	62 pF	[1]	
L1, L2, L3, L4	3 turns 1 mm copper wire	D = 3 mm; length = 2 mm		
L5, L6	stripline	-		(L × W) 125 mm × 7 mm
L7, L8, L9, L10	stripline	-		(L × W) 8 mm × 15 mm
L11, L12	stripline	-		(L × W) 132 mm × 7 mm
R1, R2	metal film resistor	10 Ω; 0.6 W		
R3, R4	metal film resistor	3 Ω; 0.6 W		
T1, T2, T3, T4	semi rigid coax	50 Ω; 120 mm		EZ-141-AL-TP-M17

[1] American Technical Ceramics type 100B or capacitor of same quality.

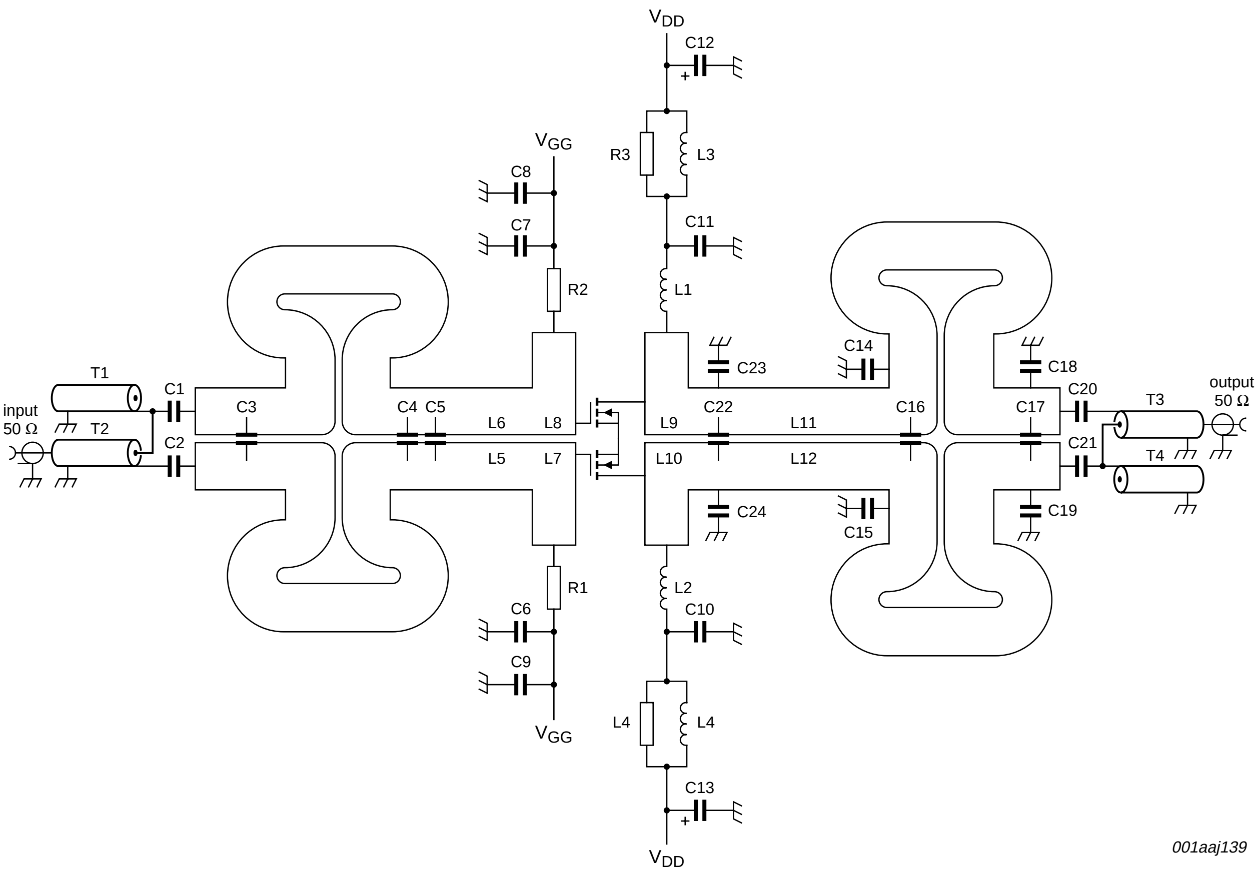


Fig 15. Class-AB common-source production test circuit

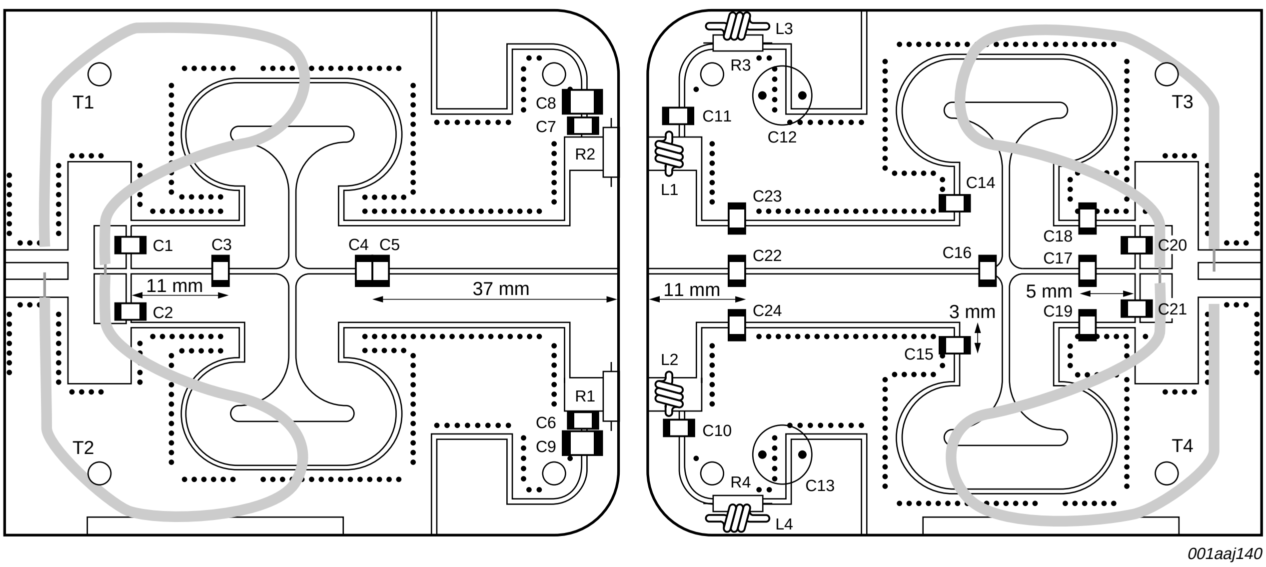
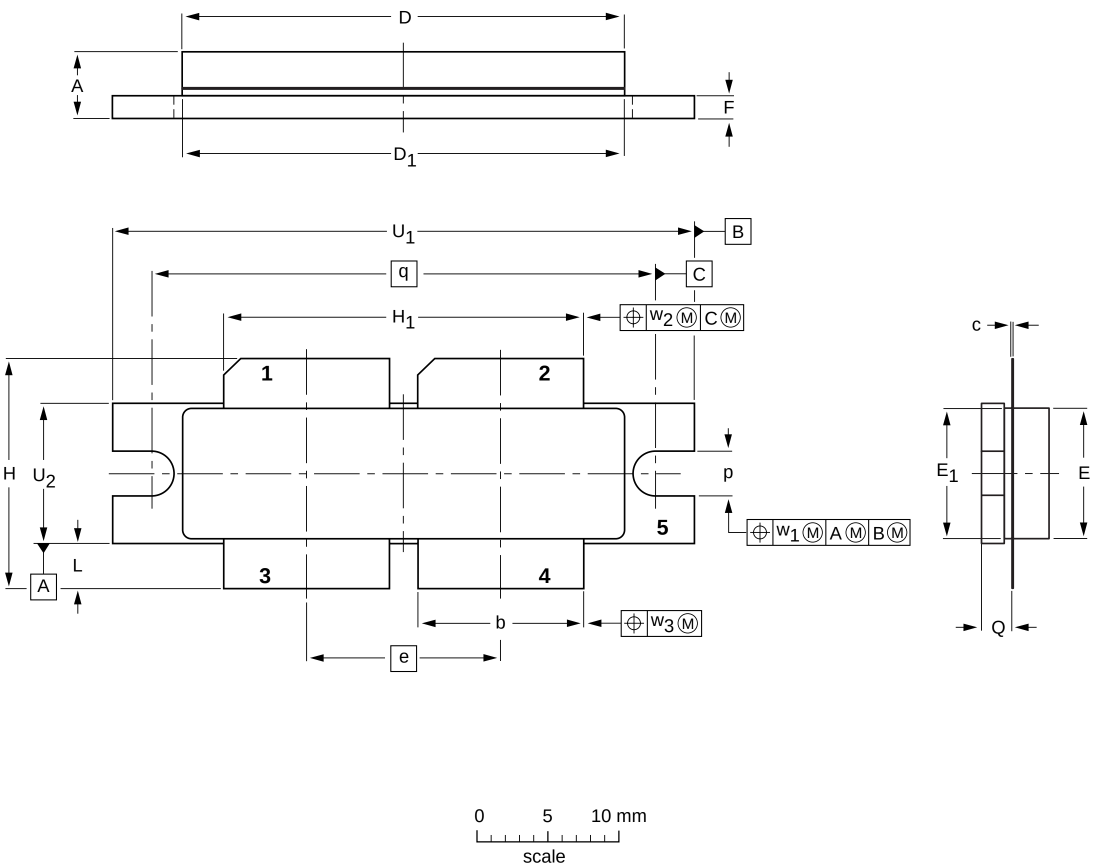


Fig 16. Component layout for class-AB production test circuit

9. Package outline

Flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.33 3.96	11.81 11.56	0.15 0.08	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.73 2.72	3.30 3.05	2.31 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.210 0.156	0.465 0.455	0.006 0.003	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.147 0.107	0.130 0.120	0.091 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~99-12-28~~ 00-03-03

Fig 17. Package outline SOT539A

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
EDGE	Enhanced Data rates for GSM Evolution
GSM	Global System for Mobile communications
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
TTF	Time To Failure
VHF	Very High Frequency
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF574_1	20081208	Preliminary data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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14. Contents

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