# UNISONIC TECHNOLOGIES CO., LTD

100V N-Channel MOSFET

■ DESCRIPTION

The UTC 100V N-Channel enhancement mode power field effect transistors (MOSFET) are produced by UTC's planar stripe, DMOS technology which has been tailored especially in the avalanche and commutation mode to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse. They are suited for low voltage applications such as audio amplifier, high efficiency switching DC/DC converters, and DC motor control.

■ FEATURES

* $R_{DS(ON)}$ = 0.1Ω @V_{GS} = 10 V
* Ultra low gate charge (typical 19nC)
* Low reverse transfer Capacitance (C_{RSS} = typical 32pF)
* Fast switching capability
* Avalanche energy Specified
* Improved dv/dt capability, high ruggedness
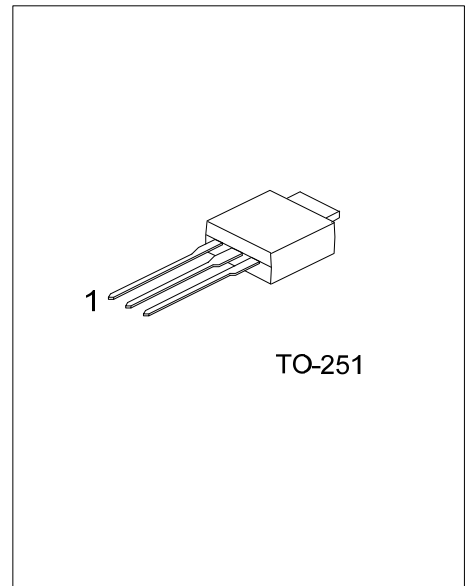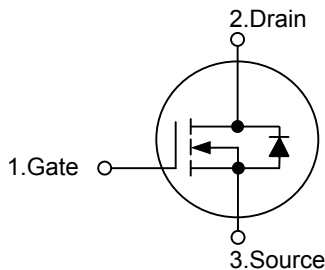
TO-251

Lead-free: 19N10L
Halogen-free: 19N10G

■ SYMBOL

2.Drain

1.Gate

3.Source

■ ORDERING INFORMATION

Ordering Number			Package	Pin Assignment			Packing
Normal	Lead Free	Halogen Free		1	2	3	
19N10-TM3-T	19N10L-TM3-T	19N10G-TM3-T	TO-251	G	D	S	Tube

19N10L-TM3-T

(1)Packing Type   (1) T: Tube

(2)Package Type   (2) TM3: TO-251

(3)Lead Plating   (3) G: Halogen Free, L: Lead Free,
                           Blank: Pb/Sn

■ **ABSOLUTE MAXIMUM RATINGS** (T$_C$=25℃, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V$_{DSS}$	100	V
Gate-Source Voltage	V$_{GSS}$	± 25	V
Continuous Drain Current	I$_D$	15.6	A
Pulsed Drain Current (Note 2)	I$_{DM}$	62.4	A
Avalanche Current (Note 2)	I$_{AR}$	15.6	A
Single Pulsed Avalanche Energy (Note 3)	E$_{AS}$	220	mJ
Repetitive Avalanche Energy (Note 2)	E$_{AR}$	5.0	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	6.0	V/ns
Power Dissipation	P$_D$	50	W
Derate above 25°C		0.4	W/°C
Junction Temperature	T$_J$	+150	℃
Storage Temperature	T$_{STG}$	-55 ~ +150	℃

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. Pulse width limited by T$_{J(MAX)}$
3. L=1.35mH, I$_{AS}$=15.6A, V$_{DD}$=25V, R$_G$=25 Ω, Starting T$_J$=25°C
4. I$_{SD}$≤19A, di/dt ≤ 300A/μs, V$_{DD}$≤BV$_{DSS}$, Starting T$_J$=25°C

■ **THERMAL DATA**

PARAMETER	SYMBOL	RATINGS	UNIT
Junction-to-Ambient	θ$_{JA}$	110	℃/W
Junction-to-Case	θ$_{JC}$	2.5	℃/W

■ **ELECTRICAL CHARACTERISTICS** (T$_J$=25°C, unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS							
Drain-Source Breakdown Voltage		BV$_{DSS}$	V$_{GS}$=0V, I$_D$=250μA	100			V
Breakdown Voltage Temperature Coefficient		ΔBV$_{DSS}$ / ΔT$_J$	I$_D$=250μA, Referenced to 25°C		0.1		V/°C
Drain-Source Leakage Current		I$_{DSS}$	V$_{DS}$=100V, V$_{GS}$=0V			1	μA
Gate-Source Leakage Current	Forward	I$_{GSS}$	V$_{GS}$=25V, V$_{DS}$=0V			100	nA
	Reverse		V$_{GS}$=-25V, V$_{DS}$=0V			-100	
ON CHARACTERISTICS							
Gate Threshold Voltage		V$_{GS(TH)}$	V$_{DS}$=V$_{GS}$, I$_D$=250μA	2.0		4.0	V
Static Drain-Source On-Resistance		R$_{DS(ON)}$	V$_{GS}$=10V, I$_D$=7.8A		0.078	0.1	Ω
Forward Transconductance		g$_{FS}$	V$_{DS}$=40V, I$_D$=7.8A (Note 1)		11		S
DYNAMIC PARAMETERS							
Input Capacitance		C$_{ISS}$	V$_{DS}$=25V, V$_{GS}$=0V, f=1.0 MHz		600	780	pF
Output Capacitance		C$_{OSS}$			165	215	pF
Reverse Transfer Capacitance		C$_{RSS}$			32	40	pF
SWITCHING PARAMETERS							
Total Gate Charge		Q$_G$	V$_{DS}$=80V, I$_D$=19A, V$_{GS}$=10V (Note 1, 2)		19	25	nC
Gate Source Charge		Q$_{GS}$			3.9		nC
Gate Drain Charge		Q$_{GD}$			9.0		nC
Turn-ON Delay Time		t$_{D(ON)}$	V$_{DD}$=50V, I$_D$=19A, R$_G$=25Ω (Note 1, 2)		7.5	25	ns
Turn-ON Rise Time		t$_R$			150	310	ns
Turn-OFF Delay Time		t$_{D(OFF)}$			20	50	ns
Turn-OFF Fall-Time		t$_F$			65	140	ns

■ **ELECTRICAL CHARACTERISTICS (Cont.)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=15.6A			1.5	V
Maximum Body-Diode Continuous Current	I_S				15.6	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}				62.4	A
Body Diode Reverse Recovery Time	t_{RR}	V_{GS}= 0V, I_S=19A,		78		ns
Body Diode Reverse Recovery Charge	Q_{RR}	dI_F/dt=100A/µs (Note 1)		200		nC

Note: 1. Pulse Test : Pulse width ≤300µs, Duty cycle ≤ 2%
　　　 2. Essentially independent of operating temperature

■ **TEST CIRCUITS AND WAVEFORMS**
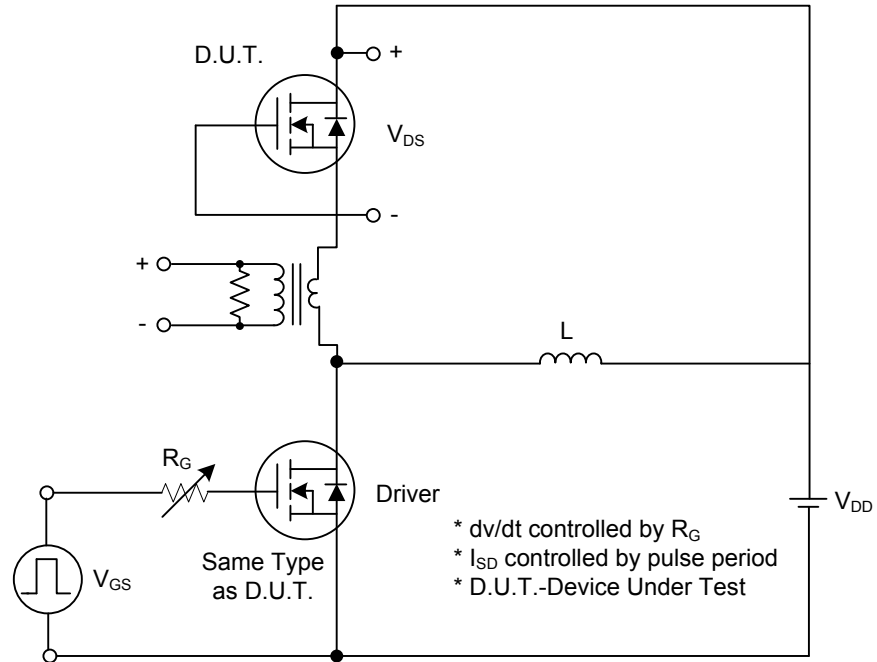
Fig. 1A Peak Diode Recovery dv/dt Test Circuit
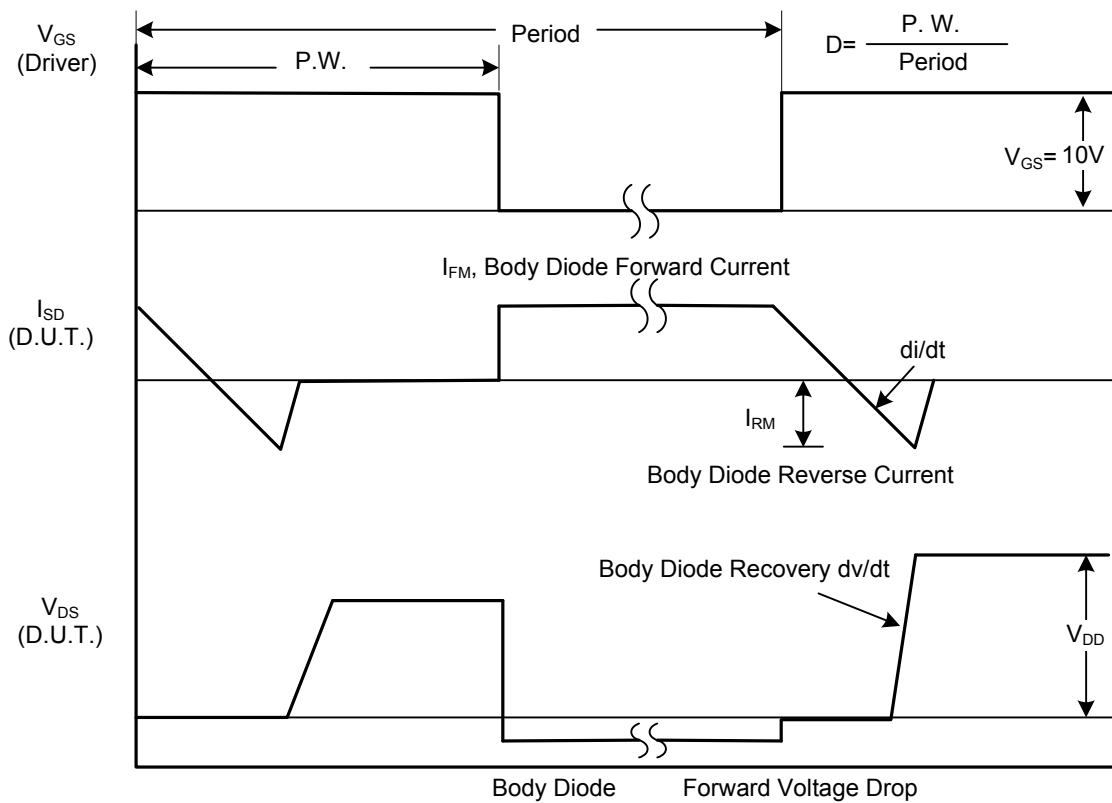
Fig. 1B Peak Diode Recovery dv/dt Waveforms

■ **TEST CIRCUITS AND WAVEFORMS (Cont.)**
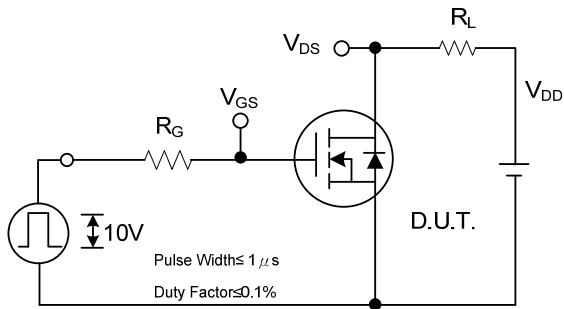
Fig. 2A Switching Test Circuit
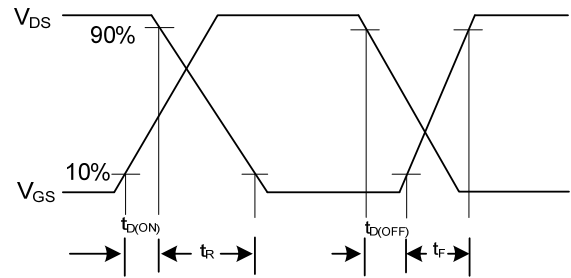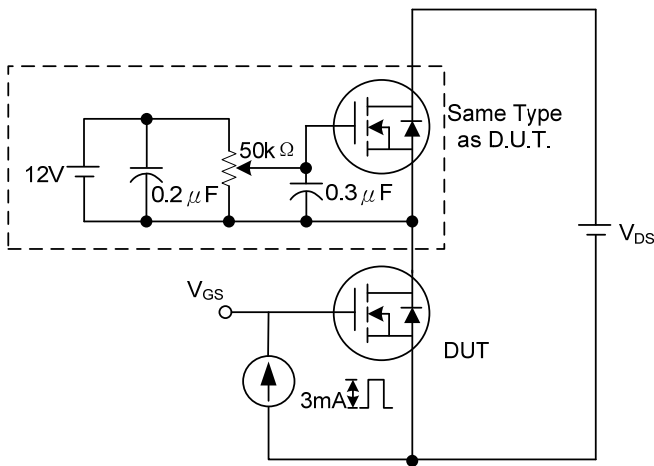

Fig. 2B Switching Waveforms
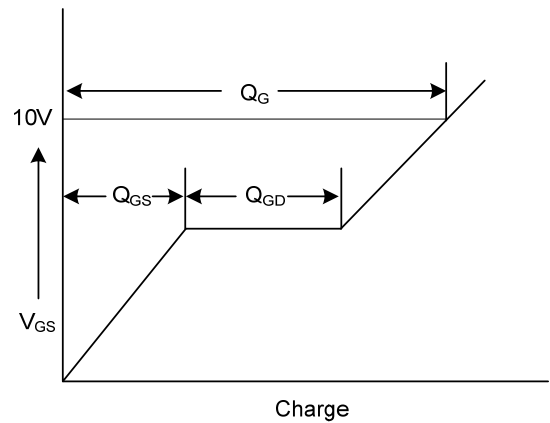

Fig. 3A Gate Charge Test Circuit

Fig. 3B Gate Charge Waveform
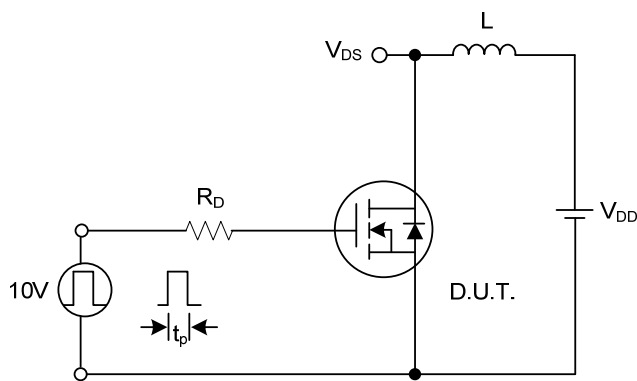
Fig. 4A Unclamped Inductive Switching Test Circuit
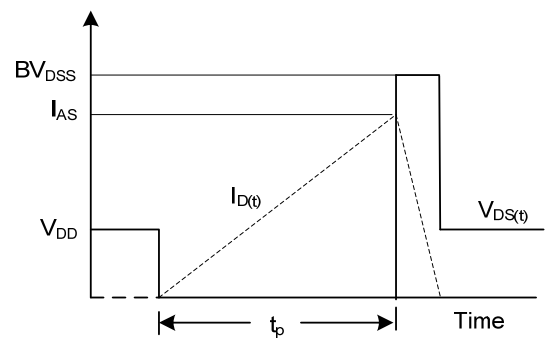
Fig. 4B Unclamped Inductive Switching Waveforms

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