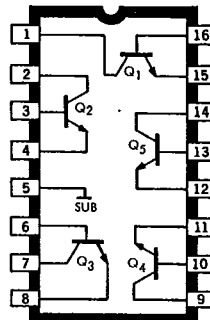


## ULN-2083A AND ULS-2083H TRANSISTOR ARRAYS (Five Independent NPN Transistors)

DESIGNED for use in general purpose, medium current (to 100 mA) switching and differential amplifier applications, the ULN-2083A and ULS-2083H transistor arrays each consist of five NPN transistors on a single monolithic chip. Two transistors are matched at low currents (1 mA) making them ideal for use in balanced mixer circuits, push-pull amplifiers, and other circuit functions requiring close thermal and offset matching.

A separate substrate connection permits maximum circuit design flexibility. In order to maintain isolation between transistors and provide normal transistor action, the substrate must be connected to a voltage which is more negative than any collector voltage. The substrate terminal (pin 5) should therefore be maintained at either d-c ground or suitably bypassed to a-c ground to avoid undesired coupling between transistors.

Two package configurations are available. The Type ULN-2083A is supplied in a 16-lead dual in-line plastic package for operation over the temperature range of  $-20^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . This package is sim-



Dwg. No. A-10,232

ilar to JEDEC style MO-001AC. The Type ULS-2083H is electrically identical to the ULN-2083A but is supplied in a hermetic dual in-line package for operation over the temperature range of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . This package conforms to the dimensional requirements of Military Specification MIL-M-38510 and can meet all of the applicable environmental requirements of Military Standard MIL-STD-883.

### ABSOLUTE MAXIMUM RATINGS at $+25^{\circ}\text{C}$ Free-Air Temperature

Power Dissipation, $P_D$ (any one transistor) .....	500 mW
(total package) .....	750 mW*
Operating Temperature Range, $T_A$ (ULN-2083A) .....	$-20^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
(ULS-2083H) .....	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Storage Temperature Range, $T_S$ .....	$-55^{\circ}\text{C}$ to $+150^{\circ}\text{C}$

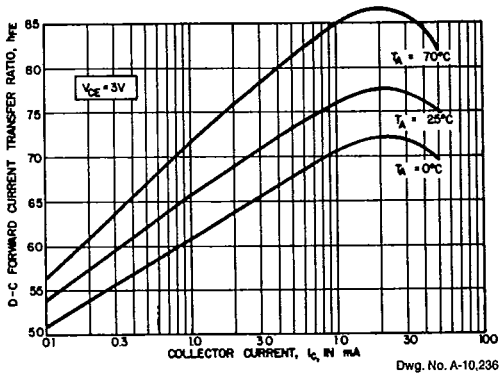
\*Derate at the rate of 6.67 mW/ $^{\circ}\text{C}$  above  $25^{\circ}\text{C}$ .

### ELECTRICAL CHARACTERISTICS at $T_A = +25^{\circ}\text{C}$ Free-Air Temperature

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Collector-Base Breakdown Voltage	$BV_{CBO}$	$I_C = 100 \mu\text{A}$	20	60	—	V
Collector-Emitter Breakdown Voltage	$BV_{CEO}$	$I_C = 1 \text{ mA}$	15	24	—	V
Collector-Substrate Breakdown Voltage	$BV_{CISO}$	$I_C = 100 \mu\text{A}$	20	60	—	V
Emitter-Base Breakdown Voltage	$BV_{EBO}$	$I_E = 500 \mu\text{A}$	5.0	6.9	—	V
Collector Cutoff Current	$I_{CEO}$	$V_{CE} = 10 \text{ V}$	—	—	10	$\mu\text{A}$
	$I_{CBO}$	$V_{CB} = 10 \text{ V}$	—	—	1.0	$\mu\text{A}$
Base Emitter Voltage	$V_{BE}$	$V_{CE} = 3 \text{ V}, I_C = 10 \text{ mA}$	650	740	850	mV
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_C = 50 \text{ mA}, I_B = 5 \text{ mA}$	—	400	700	mV
D-C Forward Current Transfer Ratio	$h_{FE}$	$V_{CE} = 3 \text{ V}, I_C = 10 \text{ mA}$	40	76	—	
		$V_{CE} = 3 \text{ V}, I_C = 50 \text{ mA}$	40	75	—	
Differential Input Offset Voltage*	$V_{IO}$	$V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$	—	1.2	5.0	mV
Differential Input Offset Current	$I_{IO}$	$V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$	www.DataSheet4U.com			$\mu\text{A}$

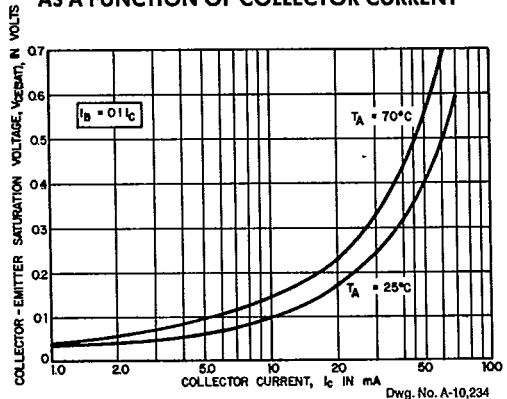
\*Applies only to transistors  $Q_1$  and  $Q_2$  when connected as a differential pair.

**D-C FORWARD CURRENT TRANSFER RATIO AS A FUNCTION OF COLLECTOR CURRENT**



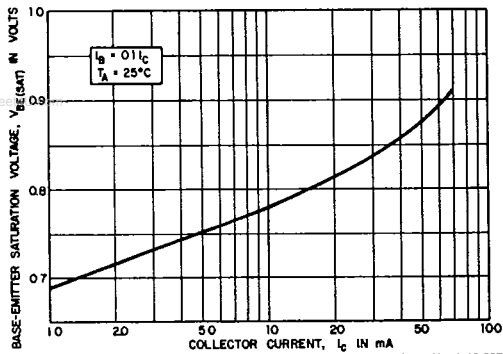
Dwg. No. A-10,236

**COLLECTOR-EMITTER SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT**



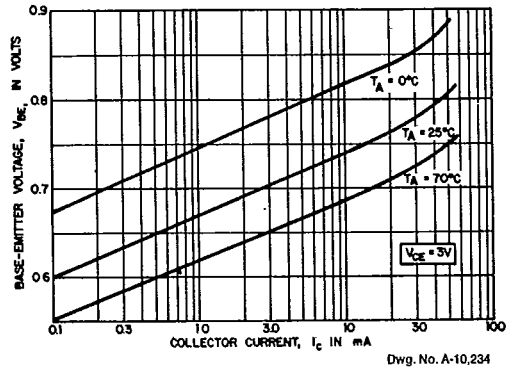
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**BASE-EMITTER SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT**



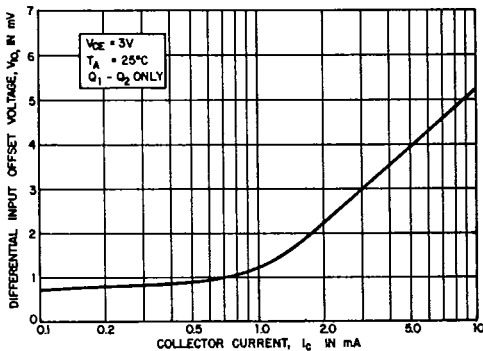
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**BASE-EMITTER VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT**



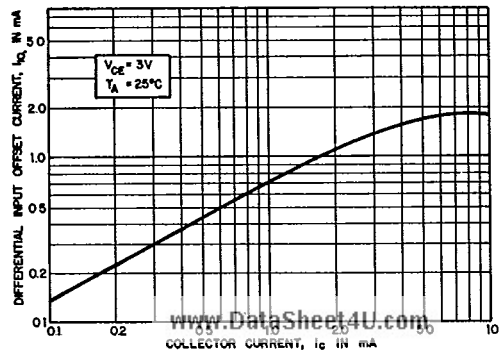
Dwg. No. A-10,234

**DIFFERENTIAL INPUT OFFSET VOLTAGE AS A FUNCTION OF COLLECTOR CURRENT**



Dwg. No. A-10,238

**DIFFERENTIAL INPUT OFFSET CURRENT AS A FUNCTION OF COLLECTOR CURRENT**



Dwg. No. A-10,240