

# 16K x 4 Static RAM

## Features

- High speed
  - 15 ns
- Output enable ( $\overline{OE}$ ) feature (CY7C166)
- CMOS for optimum speed/power
- Low active power
  - 633 mW
- Low standby power
  - 110 mW
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- CY7C164 is available in non Pb-free 22-pin (300-Mil) Molded DIP, CY7C166 in non Pb-free 24-pin Molded SOJ

## Functional Description

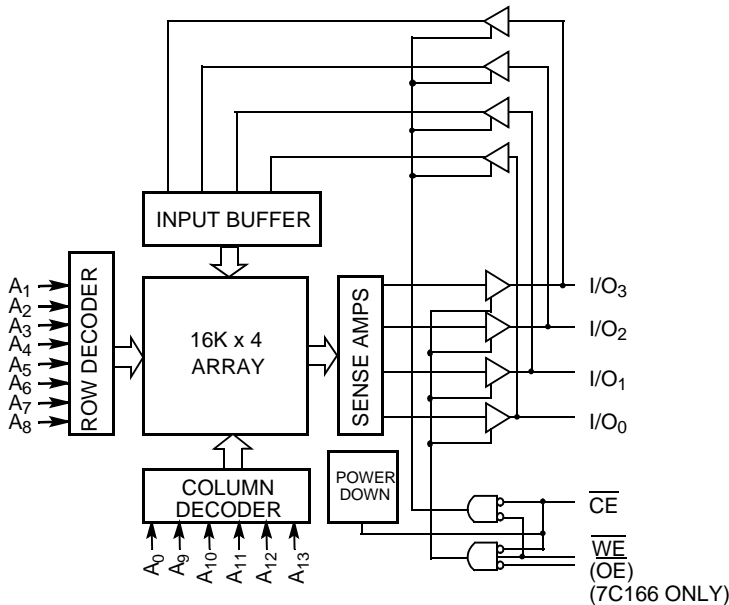
The CY7C164 and CY7C166 are high-performance CMOS static RAMs organized as 16,384 by 4 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{CE}$ ) and tri-state drivers. The CY7C166 has an active LOW Output Enable ( $\overline{OE}$ ) feature. Both devices have an automatic power-down feature, reducing the power consumption by 65% when deselected.

Writing to the device is accomplished when the Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs are both LOW (and the Output Enable ( $\overline{OE}$ ) is LOW for the CY7C166). Data on the four input/output pins ( $I/O_0$  through  $I/O_3$ ) is written into the memory location specified on the address pins ( $A_0$  through  $A_{13}$ ).

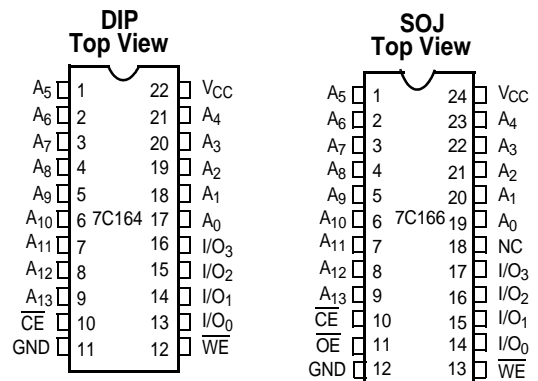
Reading the device is accomplished by taking Chip Enable ( $\overline{CE}$ ) LOW (and  $\overline{OE}$  LOW for CY7C166), while Write Enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in a high-impedance state when Chip Enable ( $\overline{CE}$ ) is HIGH (or Output Enable ( $\overline{OE}$ ) is HIGH for CY7C166). A die coat is used to insure alpha immunity.

## Logic Block Diagram



## Pin Configurations



## Selection Guide

	<b>CY7C164-15</b> <b>CY7C166-15</b>	<b>CY7C164-25</b> <b>CY7C166-25</b>
Maximum Access Time (ns)	15	25
Maximum Operating Current (mA)	115	105
Maximum CMOS Standby Current (mA)	20	20

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage to Ground Potential ..... -0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to +7.0V

DC Input Voltage<sup>[1]</sup> ..... -0.5V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%

## Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-15		-25		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub>	2.2	V <sub>CC</sub>	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA		115		105	mA
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current <sup>[2]</sup>	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ , Min. Duty Cycle = 100%		40		20	mA
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current <sup>[2]</sup>	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V		20		20	mA

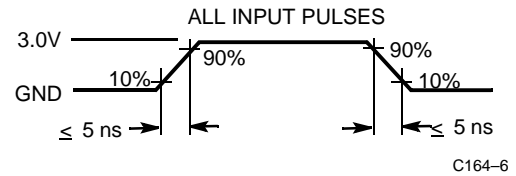
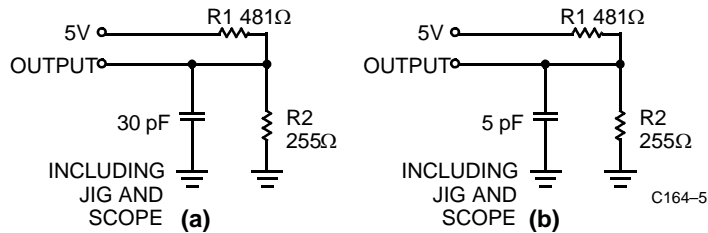
## Capacitance<sup>[3]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

### Notes:

1. Minimum voltage is equal to -3.0V for pulse durations less than 30 ns.
2. A pull-up resistor to V<sub>CC</sub> on the  $\overline{CE}$  input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.
3. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT  
 $167\Omega$   
 OUTPUT  $\rightarrow$   $1.73V$

## Switching Characteristics Over the Operating Range<sup>[4]</sup>

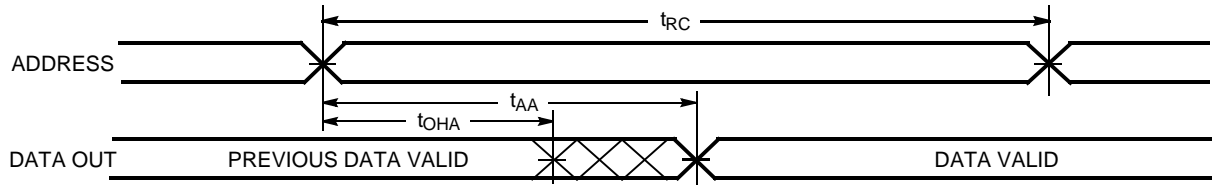
Parameter	Description	CY7C164-15 CY7C166-15		CY7C164-25 CY7C166-25		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
$t_{RC}$	Read Cycle Time	15		25		ns
$t_{AA}$	Address to Data Valid		15		25	ns
$t_{OHA}$	Output Hold from Address Change	3		5		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		15		25	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		10		12	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	7C166	3	3		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z	7C166	8		10	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[5]</sup>		3	5		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[5, 6]</sup>		8		10	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		15		20	ns
<b>WRITE CYCLE<sup>[7]</sup></b>						
$t_{WC}$	Write Cycle Time	15		20		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	12		20		ns
$t_{AW}$	Address Set-Up to Write End	12		20		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	12		15		ns
$t_{SD}$	Data Set-Up to Write End	10		10		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[5]</sup>	5		5		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[5, 6]</sup>		7		7	ns

### Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$  for any given device. These parameters are guaranteed by design and not 100% tested.
- $t_{HZCE}$  and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) in AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

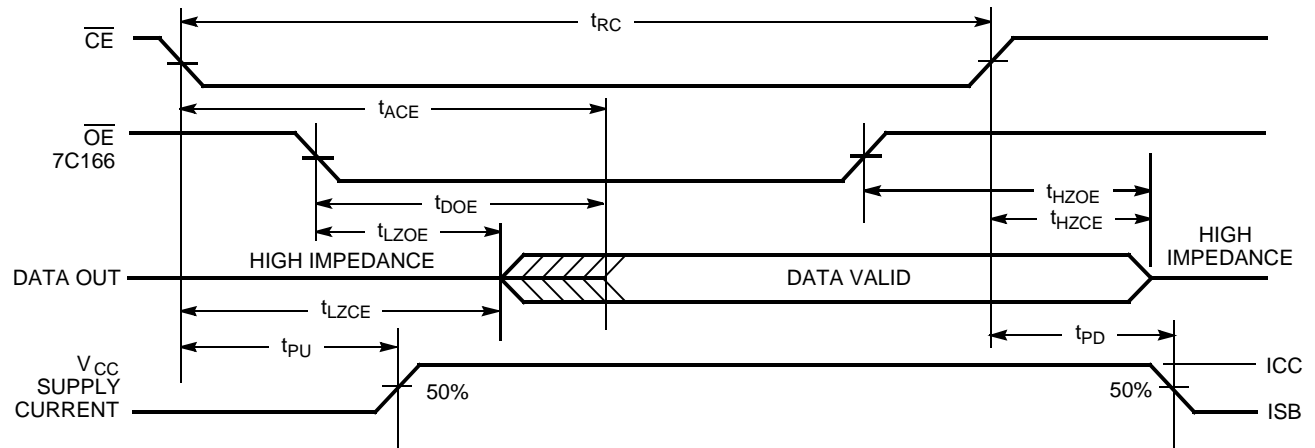
## Switching Waveforms

### Read Cycle No. 1<sup>[8,9]</sup>



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### Read Cycle No. 2<sup>[8,10]</sup>



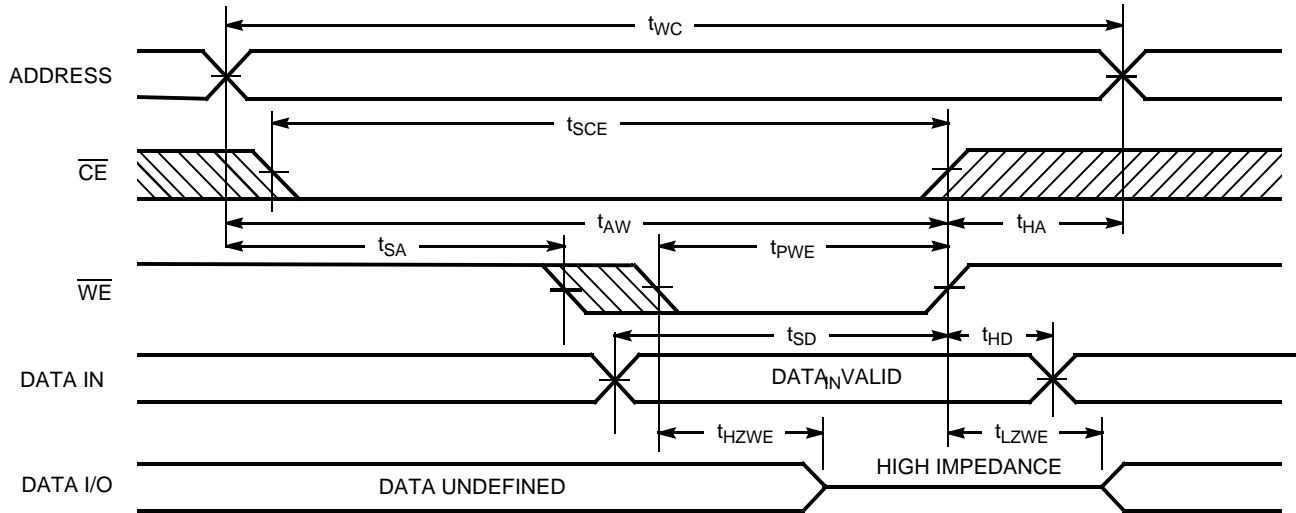
C164-8

#### Notes:

8.  $\overline{WE}$  is HIGH for read cycle.
9. Device is continuously selected,  $\overline{CE} = V_{IL}$ . (CY7C166:  $\overline{OE} = V_{IL}$  also).
10. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

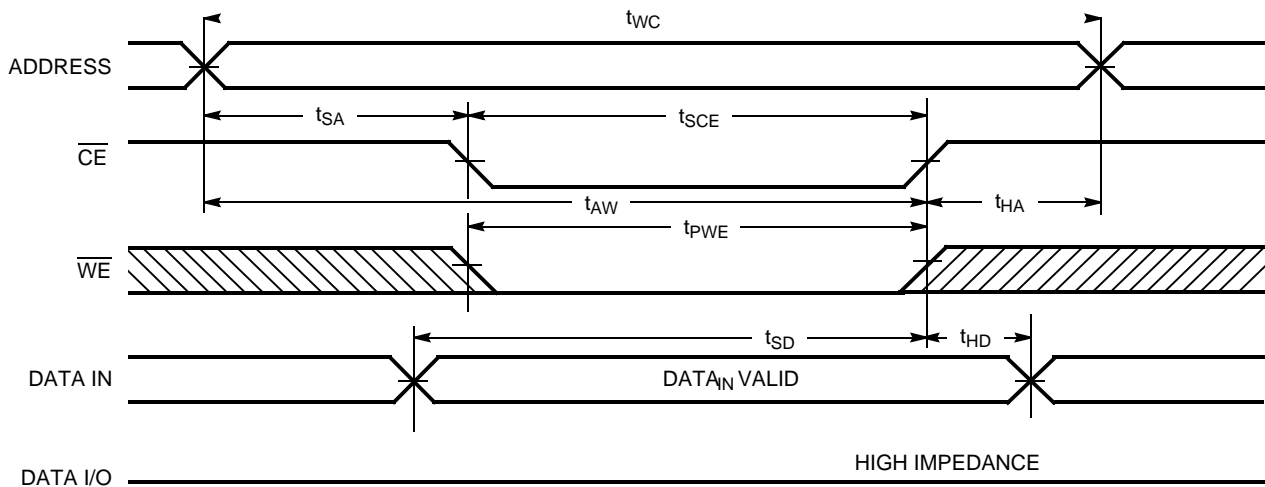
Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{WE}$  Controlled)<sup>[7,11]</sup>



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Write Cycle No. 2 ( $\overline{CE}$  Controlled)<sup>[7,11,12]</sup>

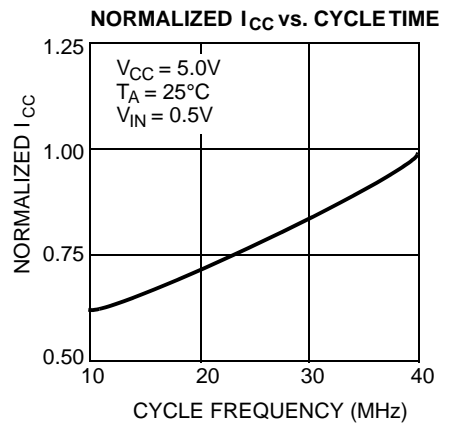
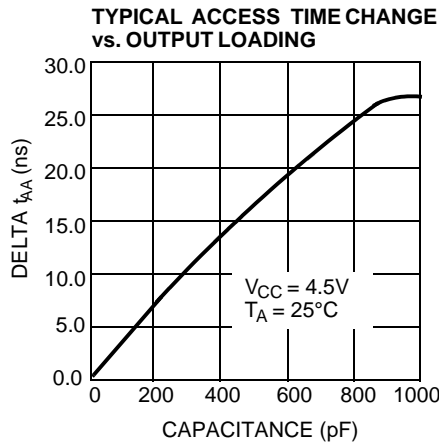
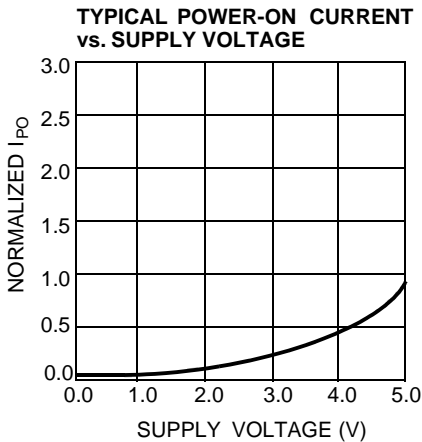
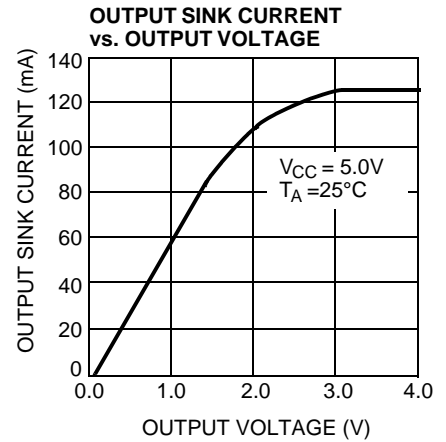
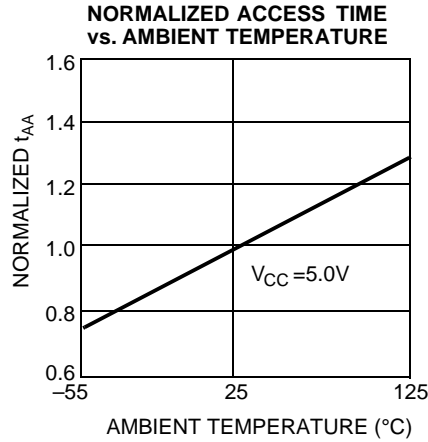
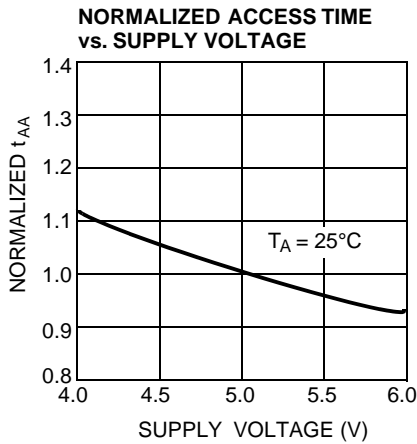
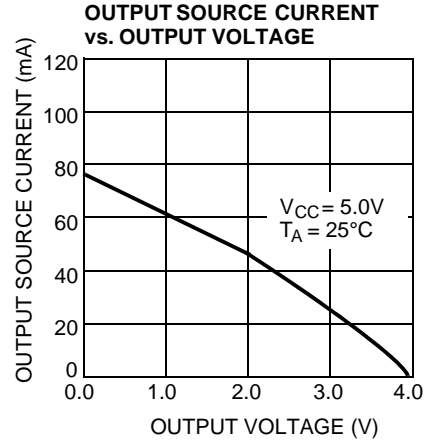
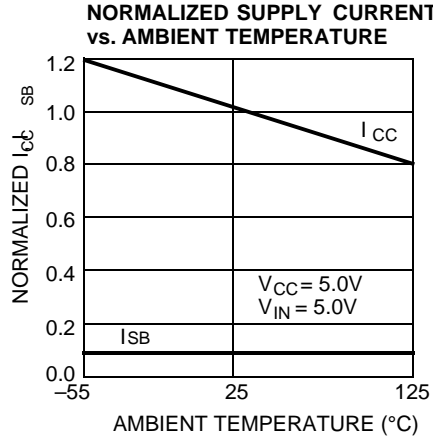
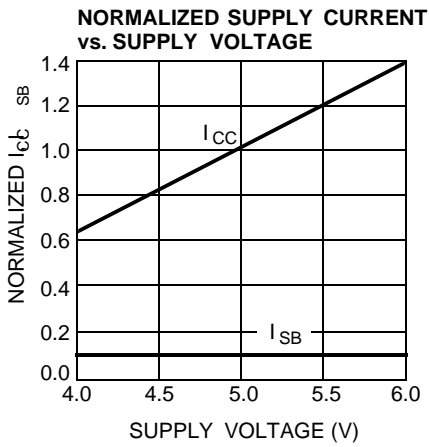


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Notes:

11. CY7C166 only: Data I/O will be high-impedance if  $\overline{OE} = V_{IH}$ .
12. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics



**CY7C164 Truth Table**

<b>CE</b>	<b>WE</b>	<b>Input/Output</b>	<b>Mode</b>	<b>Power</b>
H	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	Data Out	Read	Active ( $I_{CC}$ )
L	L	Data In	Write	Active ( $I_{CC}$ )

**CY7C166 Truth Table**

<b>CE</b>	<b>WE</b>	<b>OE</b>	<b>Input/Output</b>	<b>Mode</b>	<b>Power</b>
H	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	H	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Select/Output Disabled	Active ( $I_{CC}$ )

**Address Designators**

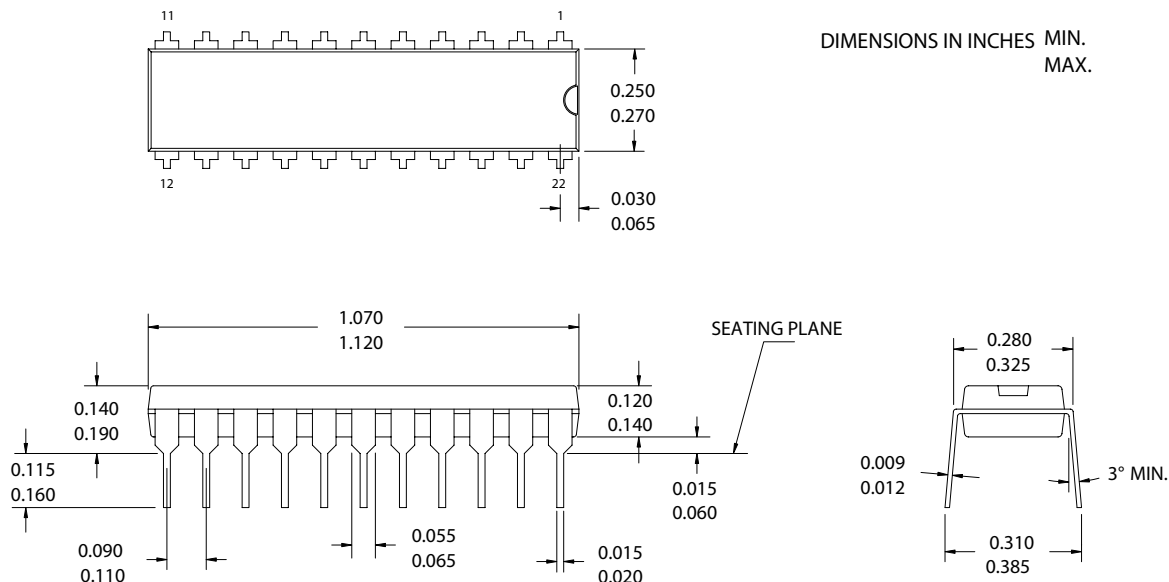
<b>Address Name</b>	<b>Address Function</b>	<b>CY 7C164 Pin Number</b>	<b>CY7C166 Pin Number</b>
A5	X3	1	1
A6	X4	2	2
A7	X5	3	3
A8	X6	4	4
A9	X7	5	5
A10	Y5	6	6
A11	Y4	7	7
A12	Y0	8	8
A13	Y1	9	9
A0	Y2	17	19
A1	Y3	18	20
A2	X0	19	21
A3	X1	20	22
A4	X2	21	23

**Ordering Information**

<b>Speed (ns)</b>	<b>Ordering Code</b>	<b>Package Diagram</b>	<b>Package Type</b>	<b>Operating Range</b>
15	CY7C164-15PC	51-85012	22-pin (300-Mil) Molded DIP	Commercial
	CY7C166-15VC	51-85030	24-pin (300-Mil) Molded SOJ	
25	CY7C164-25PC	51-85012	22-pin (300-Mil) Molded DIP	Commercial
	CY7C166-25VC	51-85030	24-pin (300-Mil) Molded SOJ	

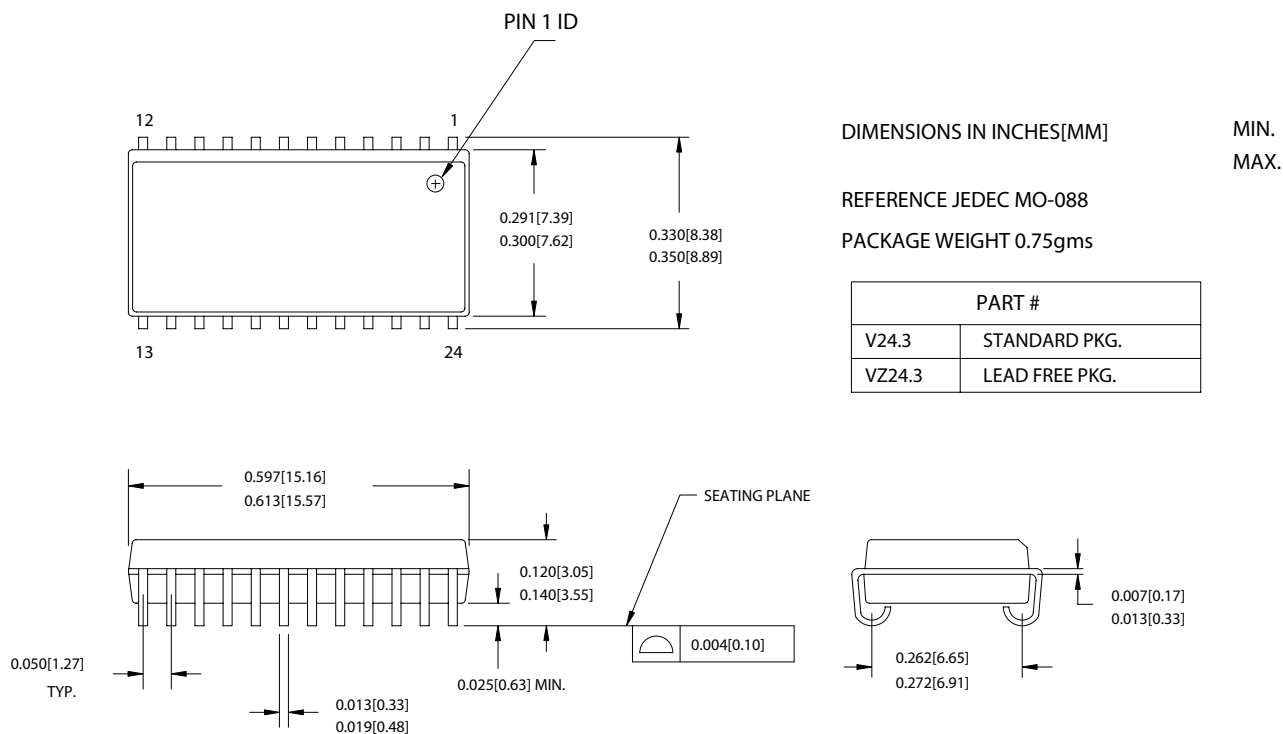
**Package Diagrams**

**22-pin (300-Mil) PDIP (51-85012)**



51-85012-\*A

**24-pin (300-mil) SOJ (51-85030)**



51-85030-\*B



**Document History Page**

Document Title: CY7C164/CY7C166 16K x 4 Static RAM Document Number: 38-05025				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	106811	09/10/01	SZV	Change from Spec number: 38-00032 to 38-05025
*A	486744	See ECN	NXR	Removed 20 ns and 35 ns speed bin from Product offering Removed 24-pin (300-Mil) Molded DIP package Changed the description of $I_{IX}$ from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed $I_{OS}$ parameter from DC Electrical Characteristics table Updated the ordering information table