DATA SHEET

OQ2538HP
SDH/SONET main amplifier

Preliminary specification
File under Integrated Circuits, IC19

1997 Nov 26

Philips
Semiconductors

PHILIPS

SDH/SONET main amplifier OQ2538HP

FEATURES

- Differential 100 Ω outputs for direct connection to Current-Mode Logic (CML) inputs
- Wide bandwidth (3 GHz)
- 48.5 dB limiting gain
- Noise figure typically 11 dB
- Automatic offset compensation
- Input level-detection circuits for Automatic Gain Control (AGC) and Loss Of Signal (LOS) detection
- Low power dissipation (typically 270 mW)
- Single –4.5 V supply voltage
- Low cost LQFP48 plastic package.

APPLICATIONS

- Main amplifier in Synchronous Digital Hierarchy (SDH) and Synchronous Optical Network (SONET) systems for short, medium and long haul optical transmission
- Level detector for laser diode control loops
- Wideband RF gain block with internal level detectors.

GENERAL DESCRIPTION

The OQ2538HP is a limiting amplifier IC intended for use as the main amplifier in 2.5 Gbits/s Non-Return to Zero (NRZ) transmission systems (SDH/SONET).

Comprised of four amplifier stages with a total gain of 48.5 dB, it provides for a wide input signal dynamic range at a constant CML compatible output level.

Two level-detection circuits are provided for monitoring AGC and LOS input signal levels. An internal automatic offset compensation circuit eliminates offset in the amplifier chain.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OQ2538HP	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM

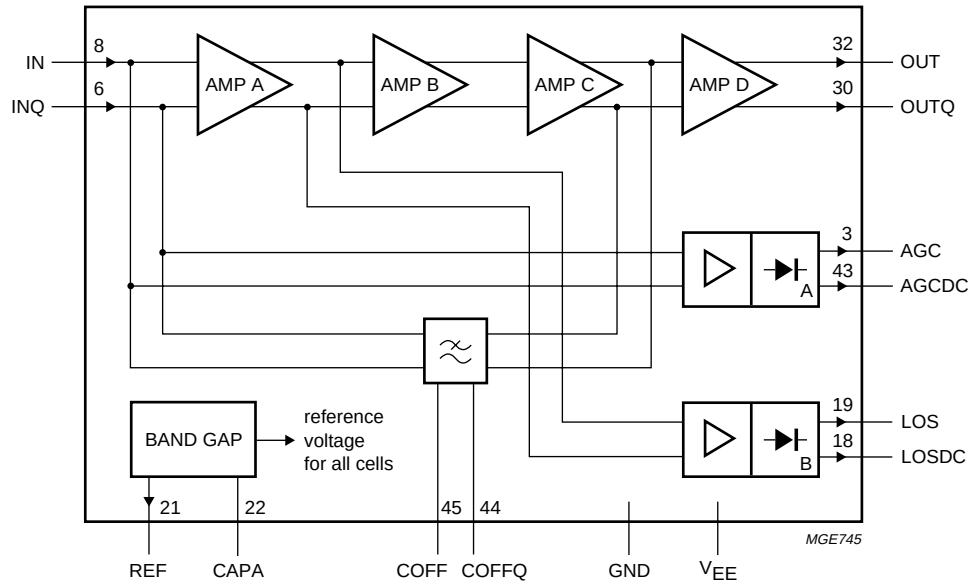


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION	TYPE[1]
V_{EE}	1	negative power supply	S
n.c.	2	not connected	–
AGC	3	rectifier A output	O
GND	4	ground	S
GND	5	ground	S
INQ	6	main amplifier inverting input	I
GND	7	ground	S
IN	8	main amplifier input	I
GND	9	ground	S
GND	10	ground	S
n.c.	11	not connected	–
V_{EE}	12	negative power supply	S
V_{EE}	13	negative power supply	S
n.c.	14	not connected	–
n.c.	15	not connected	–
GND	16	ground	S
GND	17	ground	S
LOSDC	18	rectifier B reference output	O
LOS	19	rectifier B output	O
GND	20	ground	S
REF	21	band gap reference	O
CAPA	22	pin for connecting band gap reference decoupling capacitor	A
n.c.	23	not connected	–
V_{EE}	24	negative power supply	S
V_{EE}	25	negative power supply	S
n.c.	26	not connected	–
n.c.	27	not connected	–
GND	28	ground	S
GND	29	ground	S
OUTQ	30	main amplifier inverted output	O
GND	31	ground	S
OUT	32	main amplifier output	O
GND	33	ground	S
GND	34	ground	S
n.c.	35	not connected	–
V_{EE}	36	negative power supply	S
V_{EE}	37	negative power supply	S
n.c.	38	not connected	–
GND	39	ground	S
n.c.	40	not connected	–

SYMBOL	PIN	DESCRIPTION	TYPE(1)
GND	41	ground	S
GND	42	ground	S
AGCDC	43	rectifier A reference output	O
COFFQ	44	pin for connecting automatic offset control capacitor (return)	A
COFF	45	pin for connecting automatic offset control capacitor	A
n.c.	46	not connected	–
n.c.	47	not connected	–
V_{EE}	48	negative power supply	S

Note

1. Pin type abbreviations: O = Output, I = Input, S = power Supply, A = Analog function.

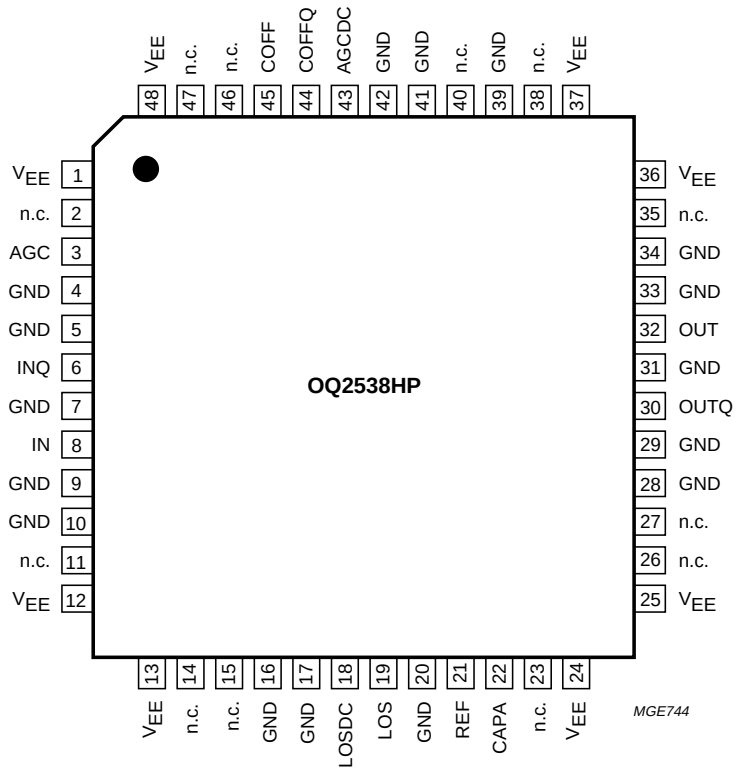


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The OQ2538HP is comprised of four DC-coupled amplifier stages along with additional circuitry for offset compensation and level detection.

The first amplifier stage contains a modified Cherry/Hooper amplifying cell with high gain (approximately 20 dB) and a wide bandwidth. Special attention is paid to minimizing the equivalent input noise at this stage, thus reducing the overall noise level. Additional feedback is applied at the second and third stages, improving isolation and reducing the gain to 14 dB per stage. The last stage is an output buffer, a unity gain amplifier, with an output impedance of 100 Ω.

The total gain of the OQ2538HP amounts to 48.5 dB, thus providing a constant CML-compatible output signal over a wide input signal range.

Two rectifier circuits are used to measure the input signal level. Two separate RF pre-amplifiers are used to generate the voltage gain needed to obtain a suitable rectifier output voltage. For rectifier A the gain is approximately 18 dB, for rectifier B it is about 14 dB. The output of rectifier A can be used for AGC at the pre-amplifier stage in front of the OQ2538HP. The output of rectifier B can be used for LOS detection. There is a linear relationship between the rectifier output voltage and the input signal level provided the amplifiers are not saturated.

Because the four gain stages are DC-coupled and provide a high overall gain, the effect of the input offset can be considerable. The OQ2538HP features an internal offset compensation circuit for eliminating the input offset. The bandwidth of the offset control loop is determined by an external capacitor.

COFF and COFFQ offset compensation

Automatic offset compensation eliminates the input offset of the OQ2538HP. This offset cancellation influences the low frequency gain of the amplifier stages. With a capacitance of 100 nF between COFF and COFFQ the loop bandwidth will be less than 1.5 kHz, small enough to have no influence on amplifier gain over the frequencies of interest. If the capacitor were omitted, the loop bandwidth would be greater than 30 MHz, which would influence the input signal gain. The loop bandwidth can be calculated from the following formula:

$$f_{loop} = \frac{1}{2\pi \times 1250\,\Omega \times C_{ext}} \quad (1)$$

where C_{ext} is the capacitance connected between COFF and COFFQ.

REF and CAPA band gap output and decoupling capacitance

To reduce band gap noise levels, a 1 nF decoupling capacitor on CAPA is recommended. Since the band gap is referenced to the negative supply, V_{EE}, the decoupling capacitor should be connected between CAPA and V_{EE}.

The band gap voltage is present for test purposes only. It is not intended to serve as an external reference.

RF input and output connections

Striplines, or microstrips, with an odd mode characteristic impedance of $Z_{o,odd}$ = 50 Ω must be used for the differential RF connections on the PCB. This applies to both the input signal pair IN and INQ and to the output signal pair OUT and OUTQ. The two lines in each pair should be the same length.

RF input matching circuit

The input circuit for pins IN and INQ contains internal 100 Ω resistors decoupled to ground via an internal common mode 6 pF capacitor. The topology is depicted in Fig.3. An external 200 Ω resistor between IN and INQ is recommended in order to match the inputs to a differential transmission line, coupled microstrip or stripline with an odd mode impedance $Z_{o,odd}$ of 50 Ω.

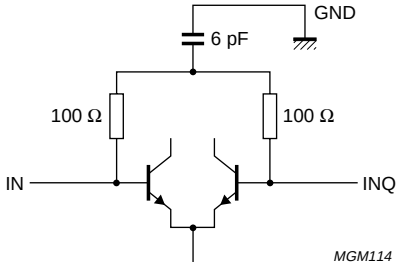


Fig.3 RF input topology.

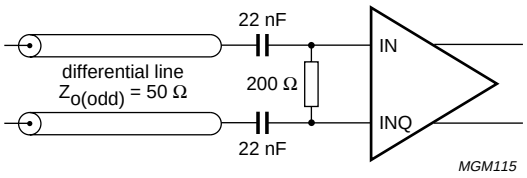


Fig.4 Differential input matching.

For single-ended excitation, separate matching networks on IN and INQ, as depicted in Fig.5, achieve optimum matching. Care should be taken to avoid DC loading, since the OQ2538HP controls its own DC input voltage.
The resistors on the unused input, INQ, may be combined for convenience.

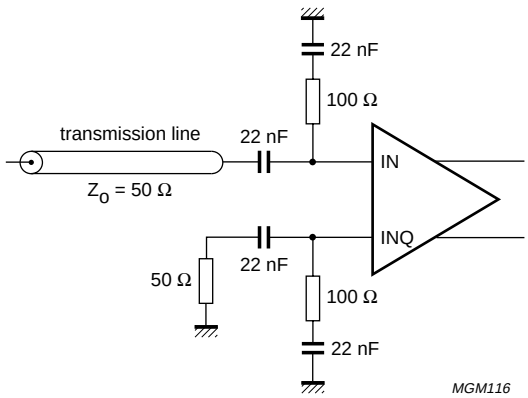


Fig.5 single-ended input matching.

In both cases, the essence of good matching is the equity of the circuitry on both input pins. The impedance seen on pins IN and INQ should be as equal as possible. For more information see *"Application Note AN96051*" describing the OM5801 STM16 demo board.

RF output matching circuit

Matching of the main amplifier outputs, OUT and OUTQ, is not mandatory. In most applications, the receiving end of the transmission line will be properly matched, so very little reflection will occur. Matching the transmitting end to absorb these reflections is only recommended for very sensitive applications. In such cases, 100 Ω pull-up resistors should be connected from OUT and OUTQ to ground, as close as possible to the IC pins. These matching resistors will not be needed in most applications, however. The output circuit of the OQ2538HP is depicted in Fig.6. For more information see *"Application Note AN96051*" describing the OM5801 STM16 demo board.

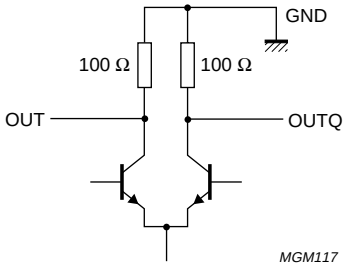


Fig.6 RF output topology.

RF gain and group delay measurements

The measurement set-up shown in Fig.7 was used to measure the single-ended small signal gain as specified in Chapter "Characteristics". Since the network analyzer can only perform single-ended measurements, the single-ended matching scheme described above is used to match the inputs of the OQ2538HP to 50 Ω. For greater accuracy, the outputs are also matched. The gain measured with this set-up is denoted by S_{21}. Graphs of typical S_{21} and group delay characteristics are shown in Figs 8 and 9. The OQ2538HP test PCB used for these measurements can be supplied on request.

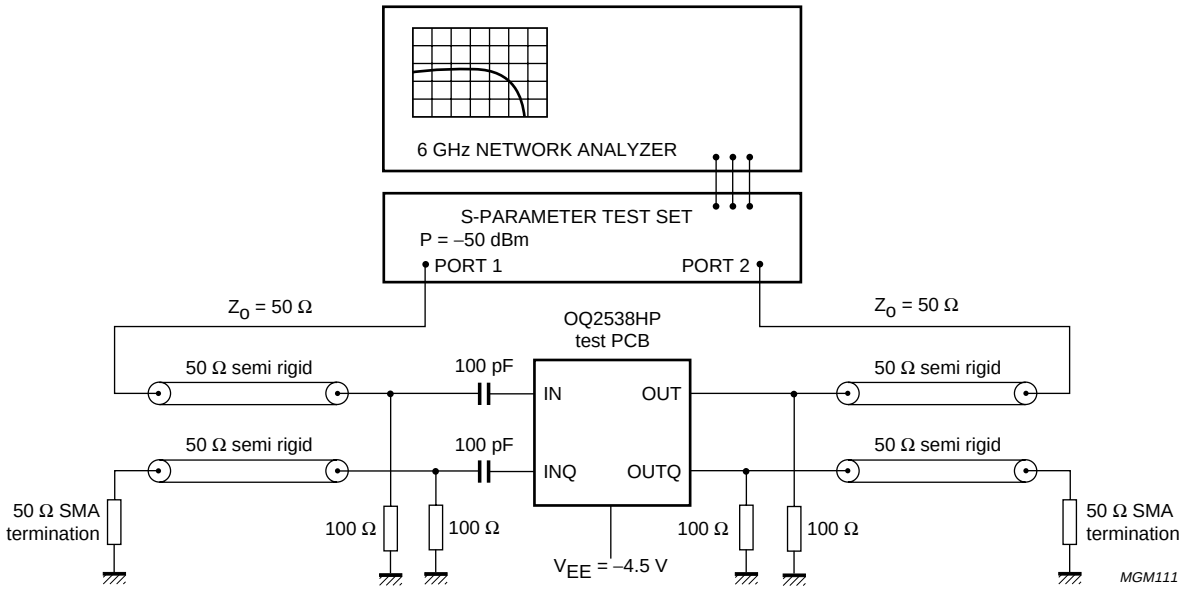
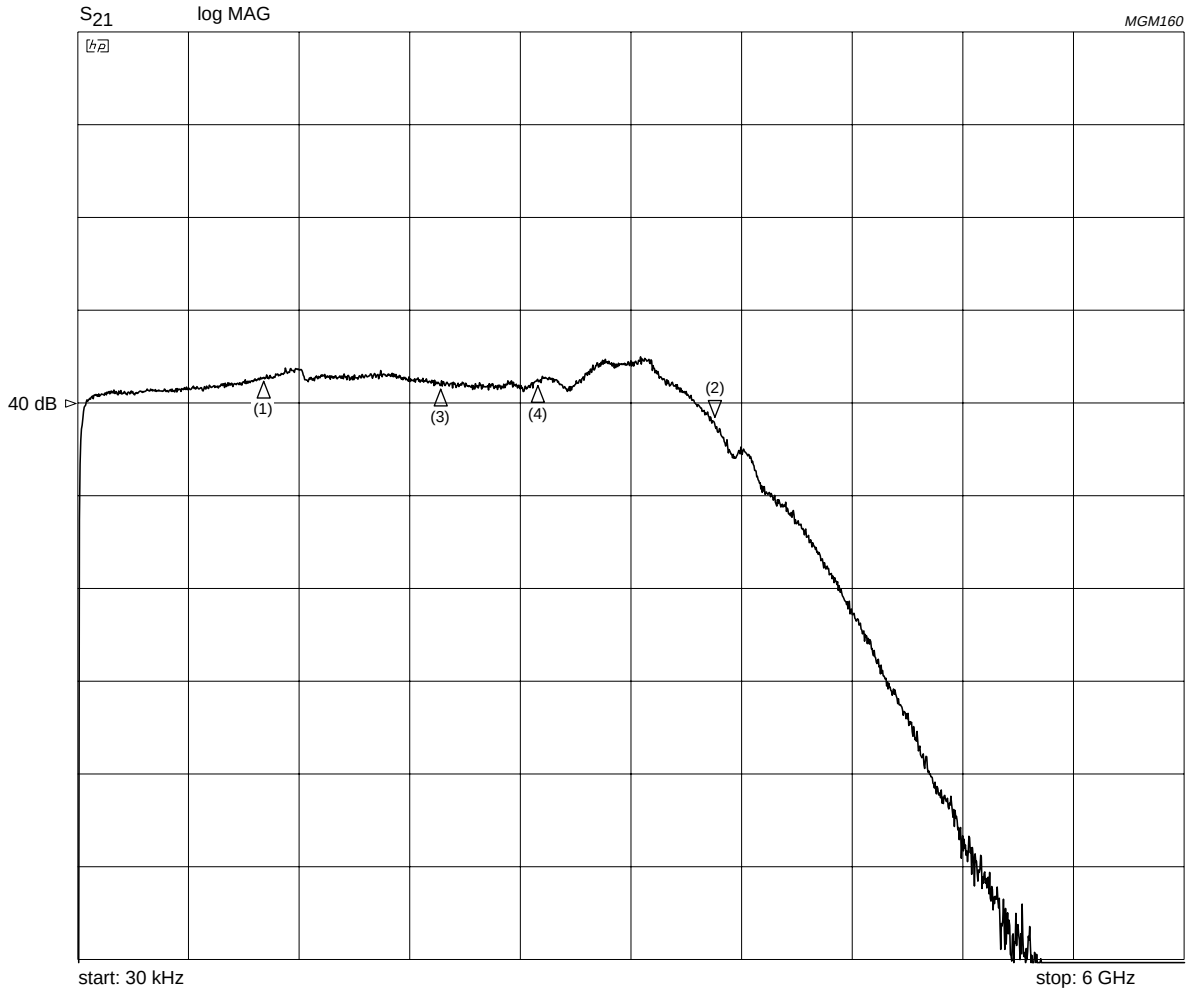


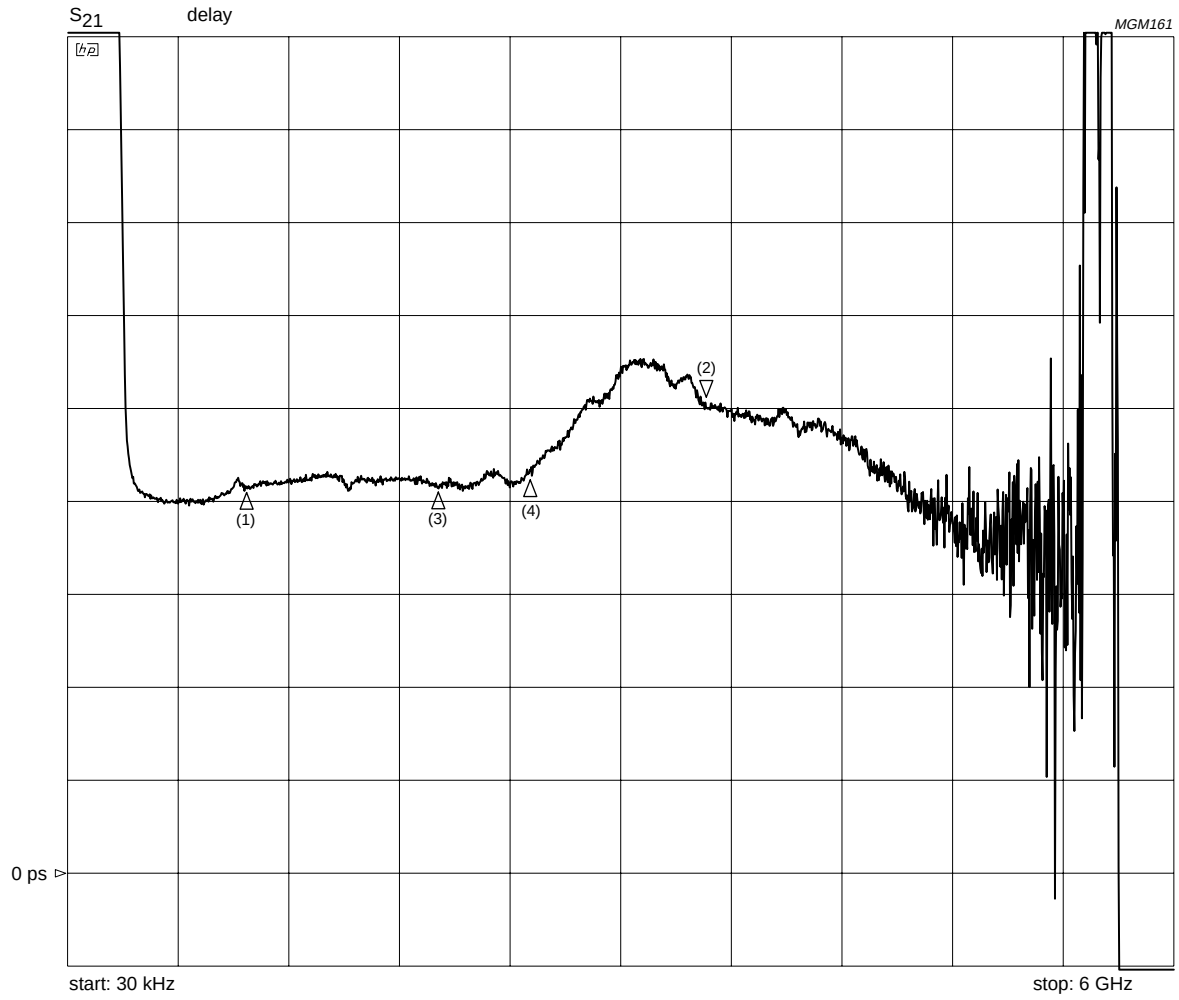
Fig.7 S_{21} and group delay measurement set-up.

Although the differential voltage gain of the OQ2538HP cannot be measured directly, it can be calculated from S_{21}. The differential voltage gain is 6 dB greater than the measured S_{21} value, typically 46 dB (40 dB + 6 dB). If the 100 Ω matching resistors on the output are omitted, the differential voltage gain is increased by a further 2.4 dB, typically to 48.4 dB. This is due to the fact that the output load is increased from 25 to 33 Ω, so the output voltage is increased by a factor of 1.32 (2.4 dB).



Vertical scale 6 dB/division.
Linear frequency sweep: start: 30 kHz; stop: 6 GHz.
(1) 41.603 dB; 1 GHz.
(2) 38.633 dB; 3.45 GHz.
(3) 41.291 dB; 2 GHz.
(4) 41.386 dB; 2.5 GHz.

Fig.8 S_{21} characteristic, measured on the OQ2538HP test PCB.



Vertical scale 200 ps/division.
Linear frequency sweep: start: 30 kHz; stop: 6 GHz.
(1) 832.91 ps; 1 GHz.
(2) 1007.4 ps; 3.45 GHz.
(3) 834 ps; 2 GHz.
(4) 860.93 ps; 2.5 GHz.

Fig.9 Group delay characteristic, measured on the OQ2538HP test PCB.

Noise figure measurements

The noise figure is the ratio of signal-to-noise ratio at the input (S_i/N_i) to signal-to-noise ratio at the output (S_o/N_o) of the amplifier. This definition is true for both single-ended and differential amplifiers, provided the correct values for S_i/N_i and S_o/N_o are substituted in the formula. The noise figure is measured using the differential set-up shown in Fig.10. The total noise on the output (N_o in dBm) is measured using the spectrum analyzer at the frequency of interest. From this value, the actual (differential) noise figure for that frequency (spot noise figure) can be calculated using the following formula:

$F = \frac{S_i/N_i}{S_o/N_o} = \frac{N_o}{2 \cdot S_{21} \cdot N_i} = \frac{N_o}{2 \cdot S_{21} \cdot kT}$ The factor 2 in the denominator is present to compensate for the fact that S_{21} is the single-ended power gain, whereas the differential power gain is applicable in this situation. N_i can be replaced with the available noise power at the input, which is kT under matched conditions (k is Boltzmann's constant). The formula expressed in dBm makes calculation easier: $F = N_o - (S_{21} + 3) + 173.8 \quad [dB]$, assuming log(kT) is –173.8 dBm (T = 298k) and N_o measured in 1 Hz bandwidth and expressed in dBm. For the OQ2538HP, in the differential configuration (including the 100 Ω matching resistors), this yields a typical noise figure of 11 dB.

While the performance of this measurement set-up cannot match that of a dedicated noise analysis system, the results are comparable for an amplifier with a noise figure of 11 dB.

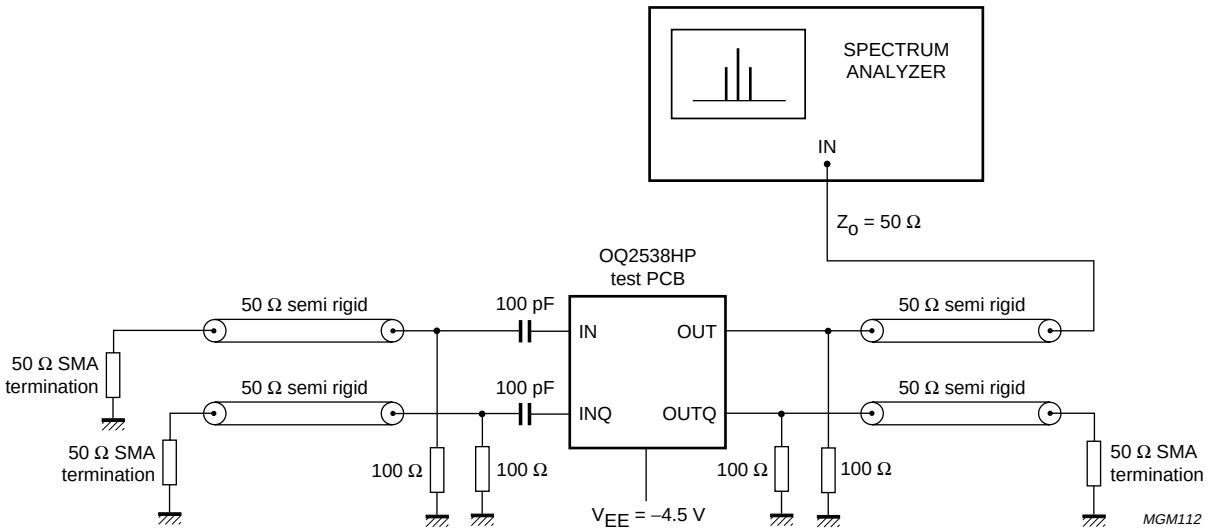
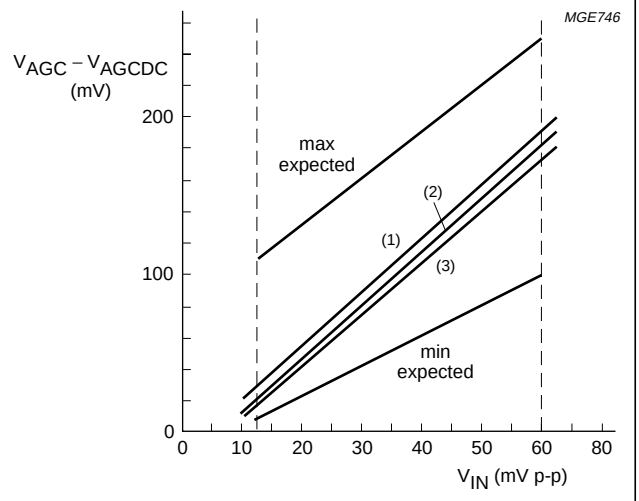
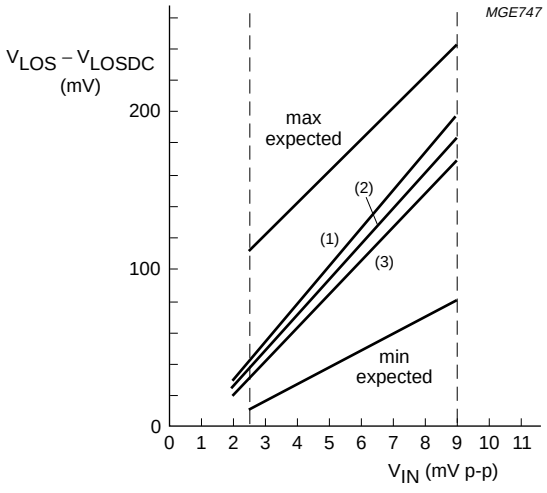


Fig.10 Noise figure measurement set-up.



(1) T_{amb} = –20 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.11 AGC transfer characteristics.



(1) T_{amb} = –20 °C.
(2) T_{amb} = +25 °C.
(3) T_{amb} = +85 °C.

Fig.12 LOS detection characteristics.

AGC and AGCDC level detection

When using rectifier A as an input signal level detector, the AGC and the AGCDC pins must be decoupled to ground with 100 nF capacitors. The AGCDC output is intended as a reference voltage against which the actual AGC output voltage can be compared. This voltage difference, $V_{AGC} - V_{AGCDC}$, can be used as a control input in an AGC loop. A graph depicting output voltage difference as a function of the input signal level (typical) is shown in Fig.11. Note that an input signal with the specified peak-to-peak value is applied to both IN and INQ inputs, but with complementary phase.

LOS and LOSDC level detection

The output of rectifier B can be used for LOS detection. The LOSDC output provides a reference voltage against which the voltage at the LOS output can be compared. The voltage difference $V_{LOS} - V_{LOSDC}$ can be used as input to a LOS detection circuit. Both outputs need to be decoupled using 100 nF capacitors. A graph depicting $V_{LOS} - V_{LOSDC}$ as a function of the input signal level (typical) is shown in Fig.12. Note that an input signal with the specified peak-to-peak value is applied to both IN and INQ inputs, but with complementary phase.

Grounding and power supply decoupling

The ground connection on the PCB needs to be a large copper area fill connected to a common ground plane with as low inductance as possible, preferably positioned directly underneath the LQFP48 package. The large area fill will improve heat transfer to the PCB and thus aid IC cooling.

All V_{EE} pins (two at each corner) need to be connected to a common supply plane with as low inductance as possible. This plane should be decoupled to ground. To avoid high frequency resonance, multiple bypass capacitors should not be mounted at the same location. To minimise low frequency switching noise in the vicinity of the OQ2538HP, the power supply line should be filtered once using an LC-circuit with a low cut-off frequency (see Fig.14).

Using alternative supply voltages

Although the OQ2538HP is intended to be used with a single –4.5 V supply voltage, a slightly modified –5 V supply can also be used. By connecting a Schottky diode between the V_{EE} power supply line and the IC, an additional 0.5 V voltage drop is obtained, bringing the supply voltage on the pins of the OQ2538HP within the specified range. A BAS85 Schottky diode is recommended. A –5 V application schematic is shown in Fig.15.

Extrapolating from this case, a +5 V application is also possible. However, care should be taken with the RF transmission lines. The on-chip signals refer to the GND pins, which become the positive supply pins in a +5 V application. The external transmission lines will most likely be referenced to system ground (V_{EE} pins). The RF signals will change from one reference plane to another at the interface to the RF input and output pins. The positive supply application is very vulnerable to interference at this point. For a successful +5 V application, special care should be taken when designing board layout to reduce the influence of interference and keep the positive supply as clean as possible.

ESD protection

Exceptions have been made to the standard ESD protection scheme in order to achieve high frequency performance. The inputs IN and INQ and the outputs OUT and OUTQ have **no protection** against ESD.
All other pins have a standard ESD protection structure, capable of withstanding 2 kV Human Body Model (HBM) zappings.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{EE}	supply voltage		–6.0	+0.5	V
ΔV_I	input voltage difference	note 1	–600	+600	mV
I_I, I_{IQ}	input current		–2.0	+2.0	mA
I_n	DC current				
	pins 30 and 32		–6	+10	mA
	pins 3, 18, 19 and 43		–3	+3	mA
	pin 21		–2	+2	mA
	pins 44 and 45		–1	+1	mA
	pin 22		–0.1	+0.1	mA
P_{tot}	total power dissipation		–	380	mW
T_j	junction temperature		–	150	°C
T_{stg}	storage temperature		–65	+150	°C

Note

1. $\Delta V_I = V_{IN} – V_{INQ}$ (AC only). The DC level is internally controlled.

THERMAL CHARACTERISTICS

SYMBOL	DESCRIPTION	VALUE	UNIT
$R_{th(j-s)}$	thermal resistance from junction to solder point	48	K/W

CHARACTERISTICS

At nominal supply voltages; T_{amb} = –40 to +85 °C; 50 Ω measuring environment.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{EE}	negative supply voltage		–4.725	–4.5	–4.275	V
I_{EE}	negative supply current		–	60	80	mA
P_{tot}	total power dissipation	note 1	–	270	380	mW
T_{amb}	operating ambient temperature	note 2	–40	–	+85	°C
T_j	operating junction temperature		–40	–	+120	°C
Main amplifier inputs: IN and INQ; note 3						
$V_{i(p-p)}$	signal voltage swing (peak-to-peak)	note 4	2	–	600	mV
V_I	DC input voltage	note 5	–2.4	–2.1	–1.7	V
V_{IO}	input offset voltage	note 6	–	0.2	–	mV
Z_i	single-ended input impedance	note 7	–	100	–	Ω
S_{21}	single-ended small signal gain	note 8	34	40	–	dB
$G_{v(dif)}$	differential voltage gain	note 9	–	48.5	–	dB
N_o	output noise power	note 10	–	–120	–	dBm
F	noise figure	note 10	–	11	–	dB
B_{-3dB}	3 dB bandwidth		2.4	3.0	–	GHz
Rectifier outputs: AGC and AGCDC; note 11						
$V_{O(ref)}$	DC reference voltage	open output	–3.3	–3.0	–2.5	V
$V_{i(p-p)}$	rectifier linear range for input signals IN and INQ (peak-to-peak value)	note 12	12.5	–	60	mV
ΔV	maximum input signal level related voltage difference	note 13	–	350	–	mV
V_{OO}	output offset voltage	note 14	–5	–	+5	mV
Rectifier outputs: LOS and LOSDC; note 11						
$V_{O(ref)}$	DC reference voltage	open output	–3.4	–3.1	–2.6	V
$V_{i(p-p)}$	rectifier linear range for input signals IN and INQ (peak-to-peak value)	note 12	2.5	–	9	mV
ΔV	maximum input signal level related voltage difference	note 13	–	400	–	mV
V_{OO}	output offset voltage	note 14	–15	–	+15	mV
Automatic offset compensation lowpass filter: COFF and COFFQ						
V_O	DC output voltage	open output	–2.4	–2.1	–1.7	V
R	offset compensation filter resistance		–	1250	–	Ω
Band gap reference: REF						
V_O	band gap voltage	referenced to V_{EE}; open output; note 15	1.1	1.3	1.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Band gap reference decoupling: CAPA						
V_O	decoupling voltage	referenced to V_{EE}; open output	–	2.9	–	V
Main amplifier outputs: OUT and OUTQ; note 16						
V_{OH}	HIGH-level output voltage		–20	–5	0	mV
V_{OL}	LOW-level output voltage	note 17	–280	–200	–140	mV
t_r	differential output rise time	input signal >2 mV (p-p)	–	100	150	ps
t_f	differential output fall time	input signal >2 mV (p-p)	–	100	150	ps
Z_o	single-ended output impedance	see Fig.6	83	100	117	Ω

Notes

1. No special cooling is required in the application if the total thermal resistance $R_{th(j-a)}$ is less than 90 K/W.
2. The temperature of the PCB in the vicinity of the IC is taken to be the ambient temperature.
3. The input signal must be AC coupled to the inputs through a coupling capacitance >22 nF.
4. $V_{i(p-p)}$ is the input signal on IN and INQ for full output clipping. It is assumed that both inputs carry a complementary signal of the specified peak-to-peak value. The lower specified limit is usually called the input sensitivity. This value is defined as a 20% increase in rise and fall times when compared to rise and fall times with a complementary input signal of 10 mV (p-p) applied to IN and INQ.
5. The DC voltage is fixed internally; only AC-coupling of the input signal is allowed.
6. $V_{IO} = |V_I - V_{IQ}|$
7. See Section “RF input matching circuit” for detailed information.
8. All signal ports are AC matched to 50 Ω and are measured at 1 GHz (see Fig.7). Flatness deviations are within ±3 dB over the entire bandwidth.
9. See section “RF gain and group delay measurements”.
10. F is the noise figure for a differential application and is measured at 1 GHz. See Section “Noise figure measurements”.
11. An external 100 nF capacitor is connected at each output to remove any spurious high frequency signals. Any circuitry driven from these pins must have an input impedance >50 kΩ.
12. The specified values are for indication only. The range is not production tested and guaranteed.
13. Voltage difference between AGC (LOS) and AGCDC (LOSDC), measured with a differential input signal of 600 mV (p-p) to pins IN and INQ.
14. The offset is measured with inputs IN and INQ shorted together.
15. The band gap voltage may not be used as an external reference.
16. Both outputs are connected to ground through a 50 Ω load resistance and carry complementary signals.
17. The output levels are dependent on load impedance. The specified values assume an external load impedance of 50 Ω. If the external 100 Ω matching resistors are connected at pins OUT and OUTQ, the output levels will fall to 75% of the specified values. (see also Section “RF gain and group delay measurements”).

APPLICATION INFORMATION

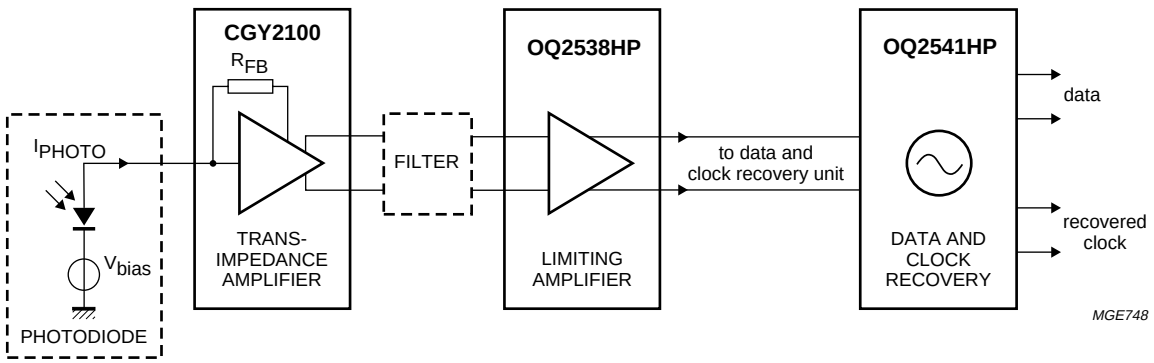


Fig.13 System application diagram.

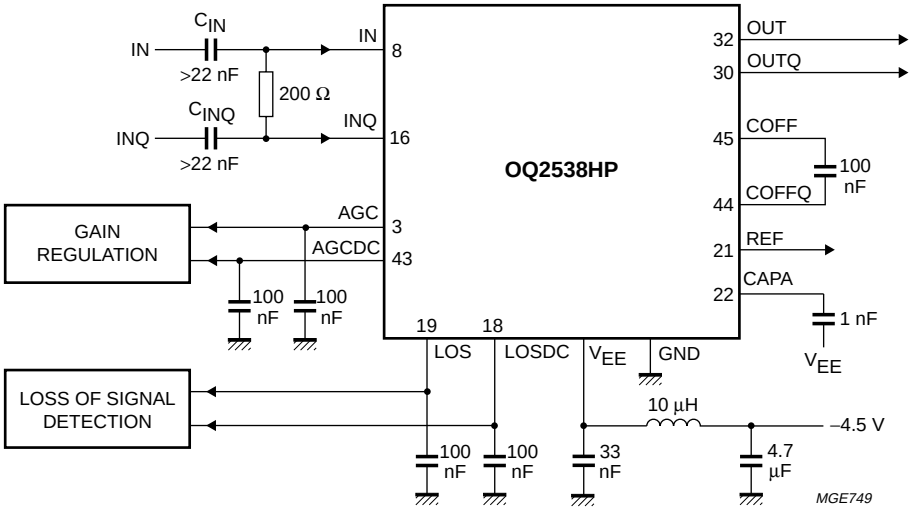


Fig.14 Typical application schematic.

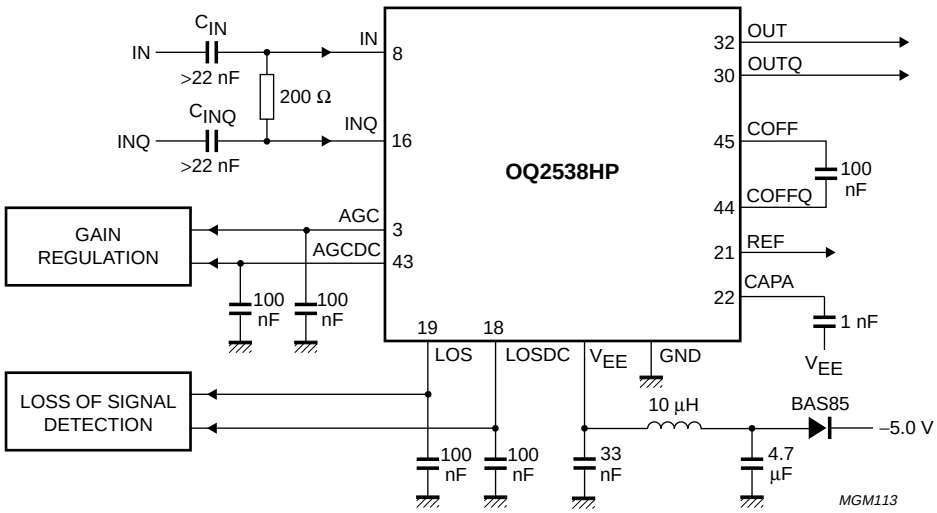
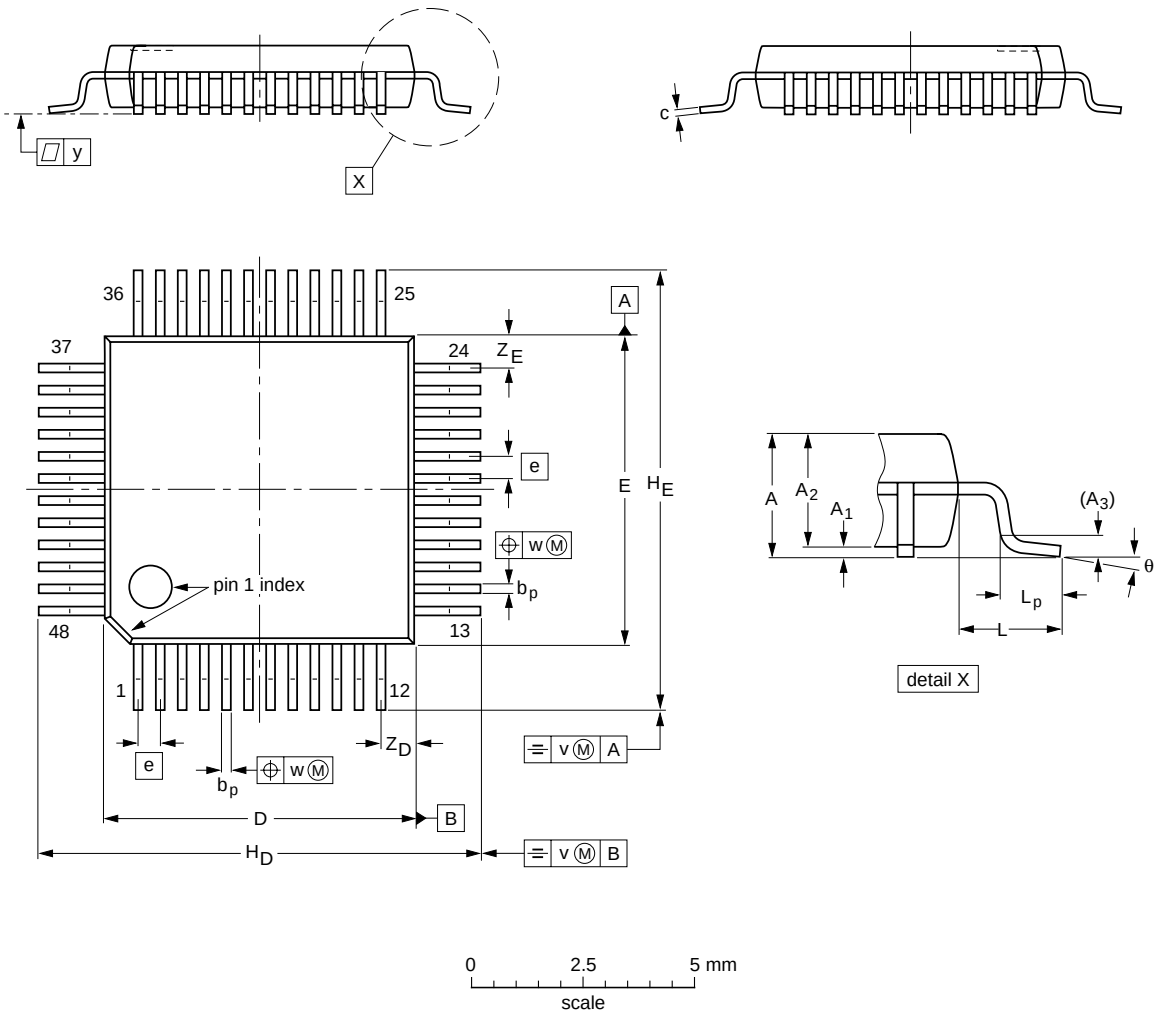


Fig.15 –5 V application schematic.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~94-12-19~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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