AVERLOGIC

AL4CX263/AL4CX273/ AL4CX283/ AL4CX293

16K/32K/64K/128K x9, 8K/16K/32K/64K x18 Synchronous FIFO

Applications

- ATM switches
- Routers
- Cable modems
- Wireless base stations
- SONET(Synchronous Optical Network) multiplexers
- Multimedia systems
- TBC(Time Base Corrector)
- Hard Disk cache memory
- Buffer for Communications

Description

The AL4CX263/AL4CX273/AL4CX283/ AL4CX293 FIFO (First In First Out) memory provides completely independent 18bit bus width input and output port operation with flexible x18/ x9 Bus-Matching data flow control at a maximum speed of 166 Mhz. The products are available in densities from 128Kbit to 1Mbit. Additional features of the AL4CX2x3 series include: fixed and programmable flags; low first word latency; partial reset; Endian select; expandable depth/width.

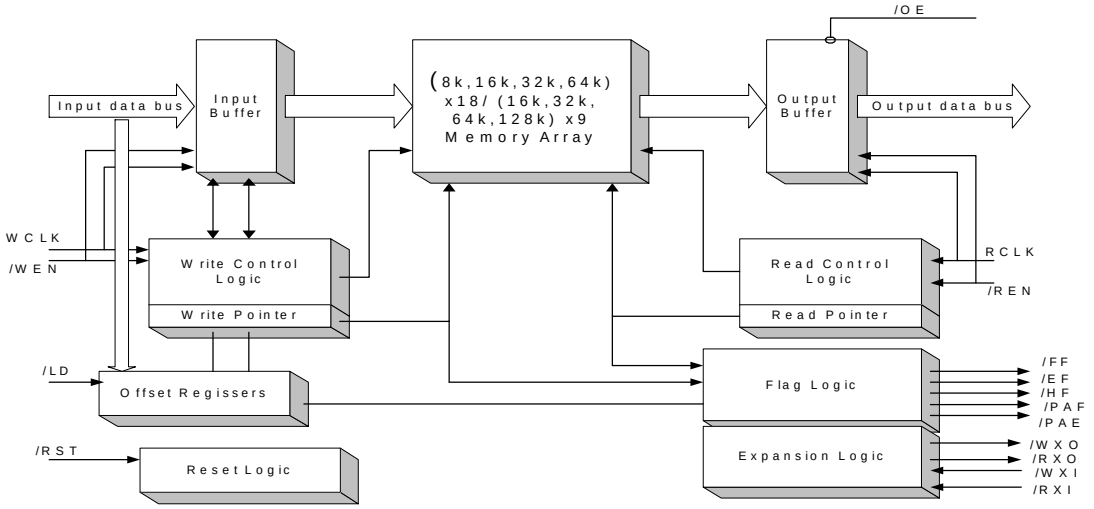
The embedded memory array with built-in address decoder, pointer manager and state-of-the-art circuits provide an easy-to-use interface to serial read/write memory and offer a flexible way to manage memory in the system design.

Features

- 8,192 x 18/16, 384 x 9-bit (AL4CX263)
- 16,384 x 18/32, 768 x 9-bit (AL4CX273)
- 32,768 x 18/65, 536 x 9-bit (AL4CX283)
- 65,536 x 18/131, 072 x 9-bit (AL4CX293)
- Maximum 166 MHz Operation
- 6 ns read/write cycle time
- Independent Read and Write operations Standard or First Word Fall Through mode
- Bus-Matching and Endian selection
- Empty, Full, Half-Full and Programmable Almost-Empty, Almost-Full Flags
- Depth and width expandable
- Output enable (data skipping)
- Master Reset clears entire FIFO
- Partial Reset, clears data
- Zero Latency Retransmit
- 3.3V power supply with 5V tolerant inputs
- Available in a 80-pin thin quad flat pack (TQFP)

Ordering Information

Part number	AL4CX263, AL4CX273, AL4CX283, AL4CX293
Package	80-pin plastic TQFP
Power Supply	+3.3V±10%



AL4CX2x3 FIFO Block Diagram

AL4CX2x3 FIFO memory is AverLogic Technologies, latest products that is designed to buffer high-speed data for a wide range of application such as optical storage controllers, Networking Switches and various communication applications.

The embedded memory array with built-in address decoder, pointer manager and state-of-the-art circuits provide an easy-to-use interface to serial read/write memory and offer a flexible way to manage memory in the system design.

The input port of the FIFO is controlled by a free running clock (WCLK), and an input enable (/WEN). The output port is controlled by another clock (RCLK) and an output enable (/REN). Data is read into or output from FIFO synchronous on every individual WRCK or RCLK clock cycle when /WEN or /REN is asserted respectively.

These FIFOs support selectable bus width up to 18bit for both input and output ports and can be configured as x18 to x18, x18 to x9, x9 to x18 and x9 to x9 multiple input and output port bus width. This allows for easy conversion of the bus width between the input flow and output flow.

There are two fixed flags, Empty Flag/Output Ready and Full Flag/Input Ready, and two programmable flags, Almost-Empty and Almost-Full. The flags enable further manipulation of the synchronous control.

Multiple AL4CX2x3s can be cascaded to expand the storage depth or can be used in parallel to expand bus width. The FIFOs are 3.3-volt devices with 5-volt input tolerance. And are available in the 80-pin thin quad flat Pack (TQFP Package).

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