P4C150
ULTRA HIGH SPEED 1K X 4
RESETTABLE STATIC CMOS RAM

FEATURES

- **Full CMOS, 6T Cell**
- **High Speed (Equal Access and Cycle Times)**
  - **– 10/12/15/20/25 ns (Commercial)**
  - **– 15/20/25/35 ns (Military)**
- **Chip Clear Function**
- **Low Power Operation**
- **Single 5V ± 10% Power Supply**
- **Separate Input and Output Ports**
- **Three-State Outputs**
- **Fully TTL Compatible Inputs and Outputs**
- **Standard Pinout (JEDEC Approved)**
  - **– 24-Pin 300 mil DIP**
  - **– 24-Pin 300 mil SOIC**
  - **– 28-Pin LCC (350 x 550 mils)**
  - **– 24-Pin CERPACK**

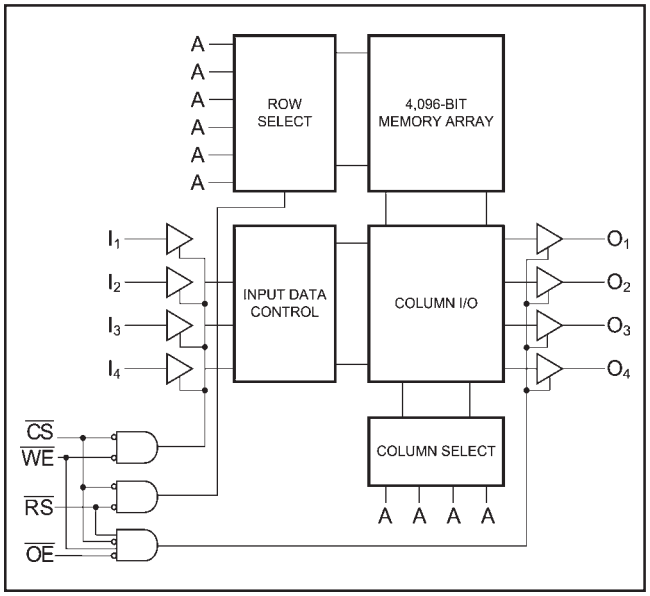
DESCRIPTION

The P4C150 is a 4,096-bit ultra high-speed static RAM organized as 1K x 4 for high speed cache applications. The RAM features a reset control to enable clearing all words to zero within two cycle times. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs and outputs are fully TTL-compatible. The RAM operates from a single 5V ± 10% tolerance power supply.

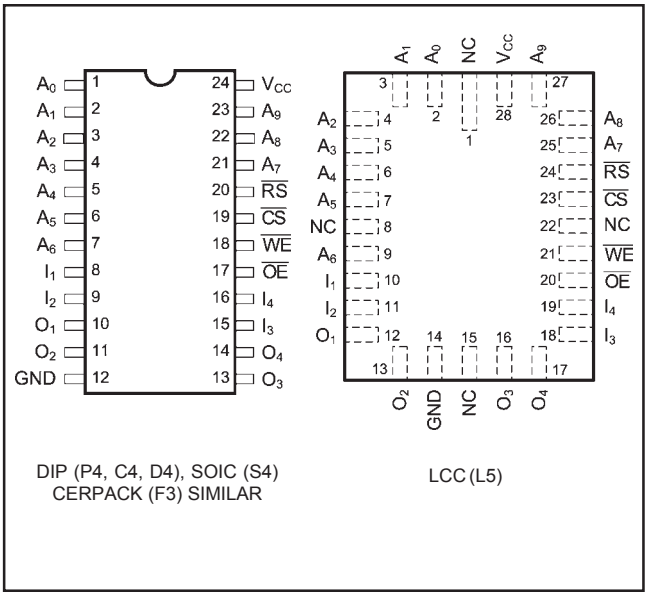
Access times as fast as 10 nanoseconds are available permitting greatly enhanced system operating speeds. Time required to reset is only 20 ns for the 10 ns SRAM. CMOS is used to reduce power consumption to a low level.

The P4C150 is available in 24-pin 300 mil DIP and SOIC packages providing excellent board level densities. The device is also available in a 28-pin LCC package as well as a 24-pin FLATPACK for military applications.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP (P4, C4, D4), SOIC (S4)
CERPACK (F3) SIMILAR

LCC (L5)

MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Pin with Respect to GND	–0.5 to +7	V
V_{TERM}	Terminal Voltage with Respect to GND (up to 7.0V)	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	–55 to +125	°C

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

RECOMMENDED OPERATING CONDITIONS

Grade[2]	Ambient Temp	Gnd	V_{CC}
Commercial	0°C to 70°C	0V	5.0V ± 10%
Military	-55°C to +125°C	0V	5.0V ± 10%

CAPACITANCES[4]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT}= 0V	7	pF

DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage (2)

Symbol	Parameter	Test Conditions	P4C150		Unit
			Min.	Max.	
V_{OH}	Output High Voltage (TTL Load)	I_{OH} = –4 mA, V_{CC} = Min.	2.4		V
V_{OL}	Output Low Voltage (TTL Load)	I_{OL} = +8 mA, V_{CC} = Min		0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} =+0.5	V
V_{IL}	Input Low Voltage		–0.5[3]	0.8	V
I_{LI}	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	–5	+5	µA
I_{LO}	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–5	+5	µA

POWER DISSIPATION CHARACTERISTICS VS. SPEED

Symbol	Parameter	Temperature Range	-10	-12	-15	-20	-25	-35	Unit
I_{CC}	Dynamic Operating Current	Commercial	130	130	120	115	100	N/A	mA
		Military	N/A	N/A	145	135	125	120	mA

Notes:

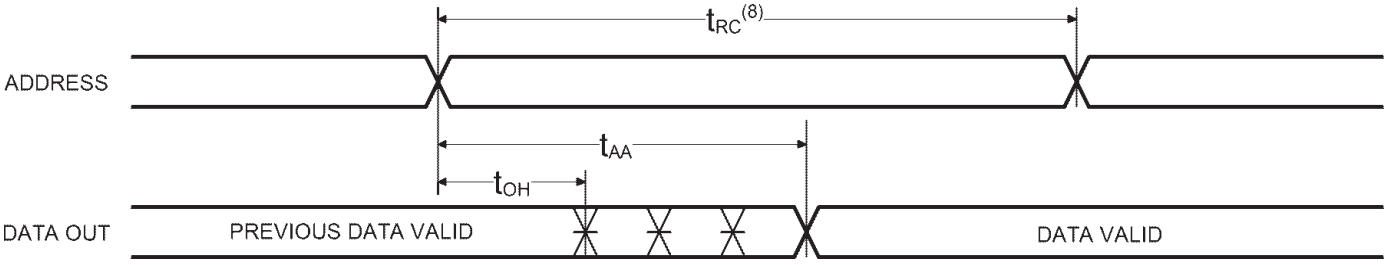
1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with V_{IL} and I_{IL} not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.

AC CHARACTERISTICS—READ CYCLE

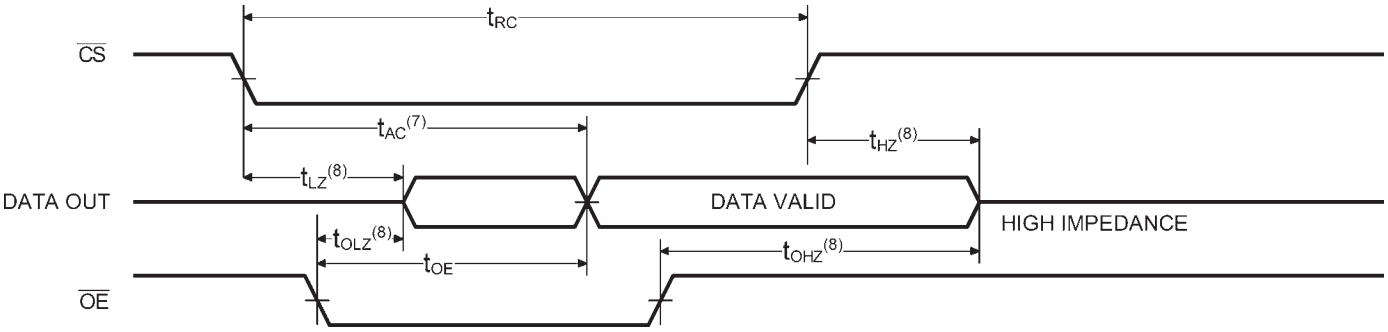
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-10		-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	10		12		15		20		25		35		ns
t_{AA}	Address Access Time		10		12		15		20		25		35	ns
t_{AC}	Chip Select Access Time		8		10		12		14		15		35	ns
t_{OH}	Output Hold from Address Change	2		2		2		2		2		2		ns
t_{LZ}	Chip Enable to Output in Low Z	2		2		2		2		2		2		ns
t_{HZ}	Chip Disable to Output in High Z		4		6		8		10		13		15	ns
t_{OE}	Output Enable to Data Valid		7		9		10		14		15		20	ns
t_{OLZ}	Output Enable to Output in Low Z	2		2		2		2		2		2		ns
t_{OHZ}	Output Disable to Output in High Z		5		7		9		11		13		16	ns

TIMING WAVEFORM OF READ CYCLE NO. 1[5,6]



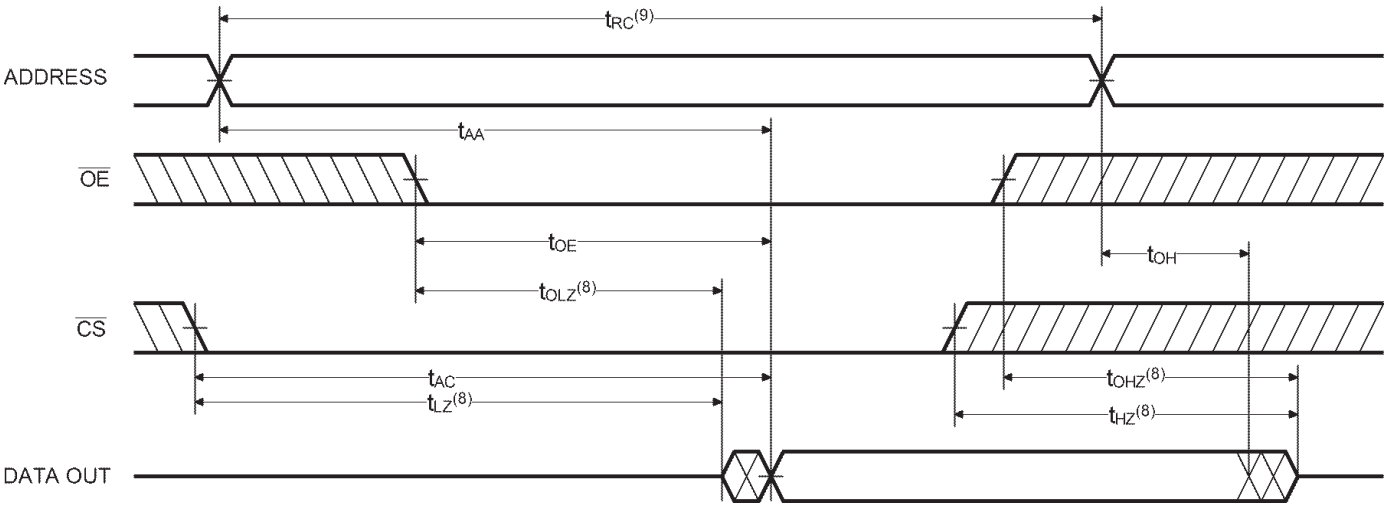
TIMING WAVEFORM OF READ CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[5,7]



Notes:

5. $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{CS}$ and $\overline{OE}$ are LOW for READ cycle.
7. ADDRESS must be valid prior to, or concident with, $\overline{CS}$ transition LOW, t_{AA} must still be met.
8. Transition is measured ±200 mV from steady state voltage prior to change, with loading as specified in Figure 1.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF READ CYCLE NO. 3 ($\overline{OE}$ Controlled)[5]

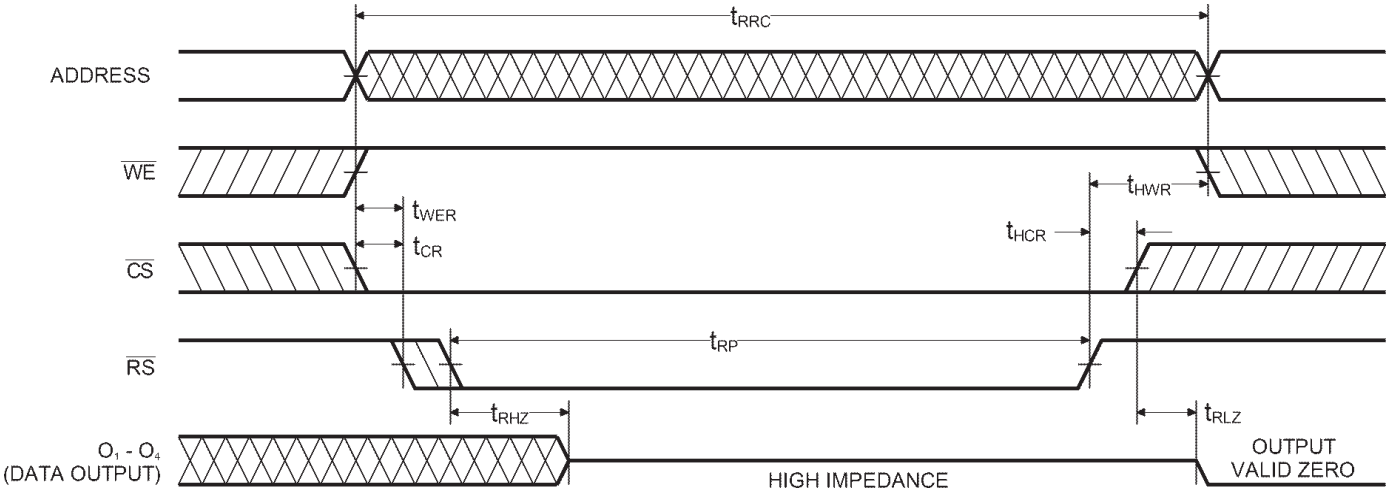


AC CHARACTERISTICS—RESET CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Symbol	Parameter	-10		-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RRC}	Reset Cycle Time	20		24		30		40		50		70		ns
t_{WER}	Write Enable High to Beginning of Reset	0		0		0		0		0		0		ns
t_{CR}	Chip Select Low to Beginning of Reset	0		0		0		0		0		0		ns
t_{RP}	Reset Pulse Width	10		12		15		20		25		30		ns
t_{HCR}	Chip Select Hold after End of Reset	0		0		0		0		0		0		ns
t_{HWR}	Write Enable Hold after End of Reset	10		12		15		20		25		35		ns
t_{RLZ}	Reset High to Output in Low Z	0		0		0		0		0		0		ns
t_{RHZ}	Reset Low to Output in High Z	0	8	0	10	0	12	0	16	0	20	0		ns

TIMING WAVEFORM OF RESET CYCLE

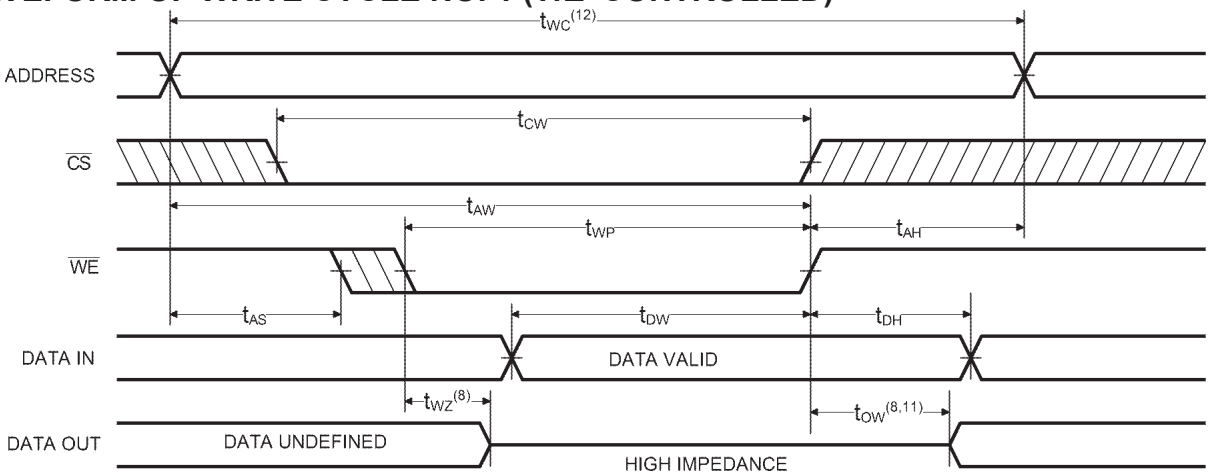


AC CHARACTERISTICS—WRITE CYCLE

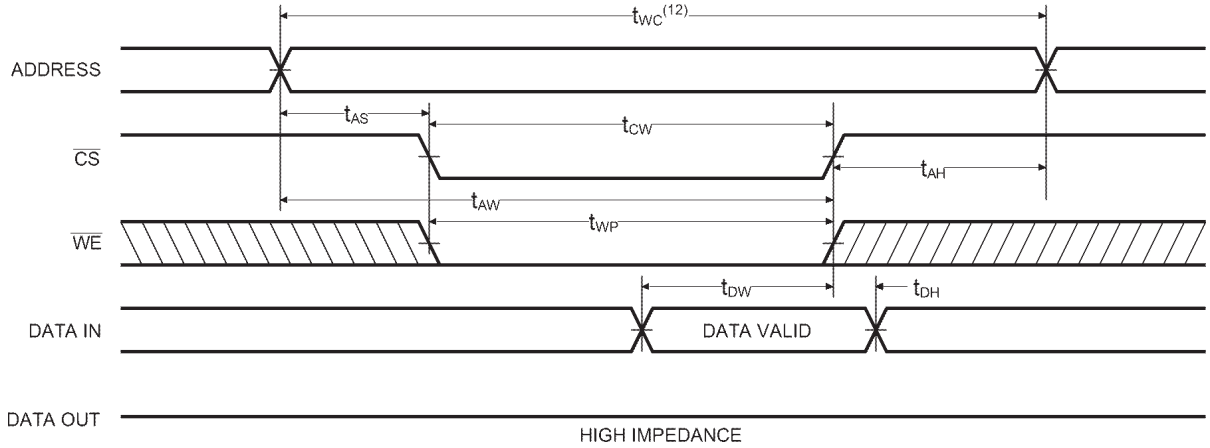
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym.	Parameter	-10		-12		-15		-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	10		12		15		20		25		35		ns
t_{CW}	Chip Enable Time to End of Write	8		10		11		13		15		20		ns
t_{AW}	Address Valid to End of Write	8		10		13		16		20		25		ns
t_{AS}	Address Set-up Time	0		1		1		1		2		2		ns
t_{WP}	Write Pulse Width	8		10		11		13		15		20		ns
t_{AH}	Address Hold Time from End of Write	0		1		1		1		2		2		ns
t_{DW}	Data Valid to End of Write	5		8		11		13		15		20		ns
t_{DH}	Data Hold Time	0		1		1		1		2		2		ns
t_{WZ}	Write Enable to Output in High Z		5		8		12		15		20		25	ns
t_{OW}	Output Active from End of Write	2		2		2		3		3		3		ns

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[10]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)[10]



Notes:

10. $\overline{CS}$ and $\overline{WE}$ must be LOW for WRITE cycle.
11. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
12. Write Cycle Time is measured from the last valid address to the first transition address.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 and 2

TRUTH TABLE

Mode	$\overline{RS}$	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output
Not Selected	X	H	X	X	High Z
RESET	L	L	X	H	High Z
Output Disabled	H	L	H	H	High Z
READ	H	L	L	H	D_{OUT}
WRITE	H	L	X	L	High Z

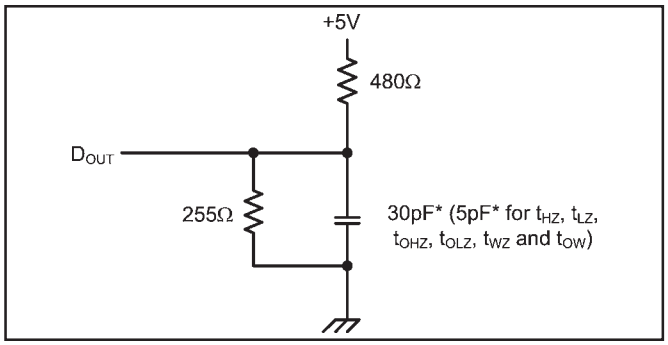


Figure 1. Output Load

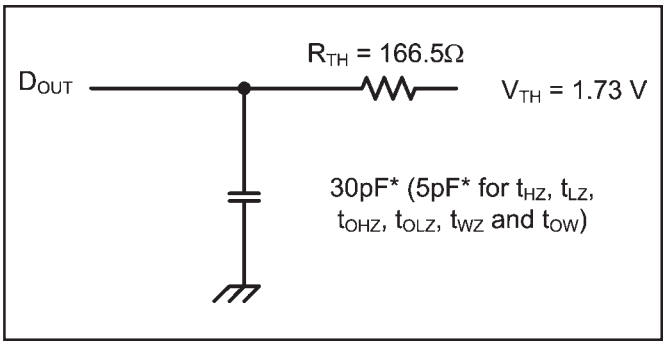
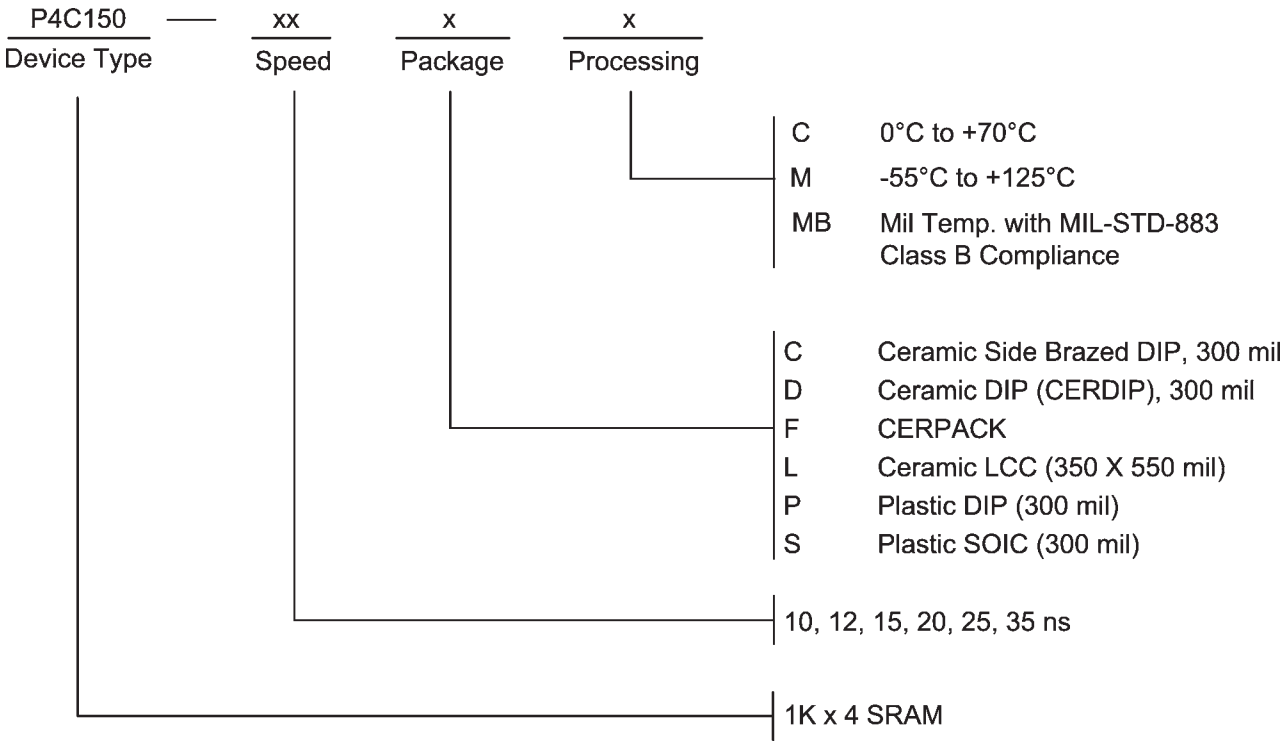


Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:
Due to the ultra-high speed of the P4C150, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

ORDERING INFORMATION



SELECTION GUIDE

The P4C150 is available in the following temperature, speed and package options.

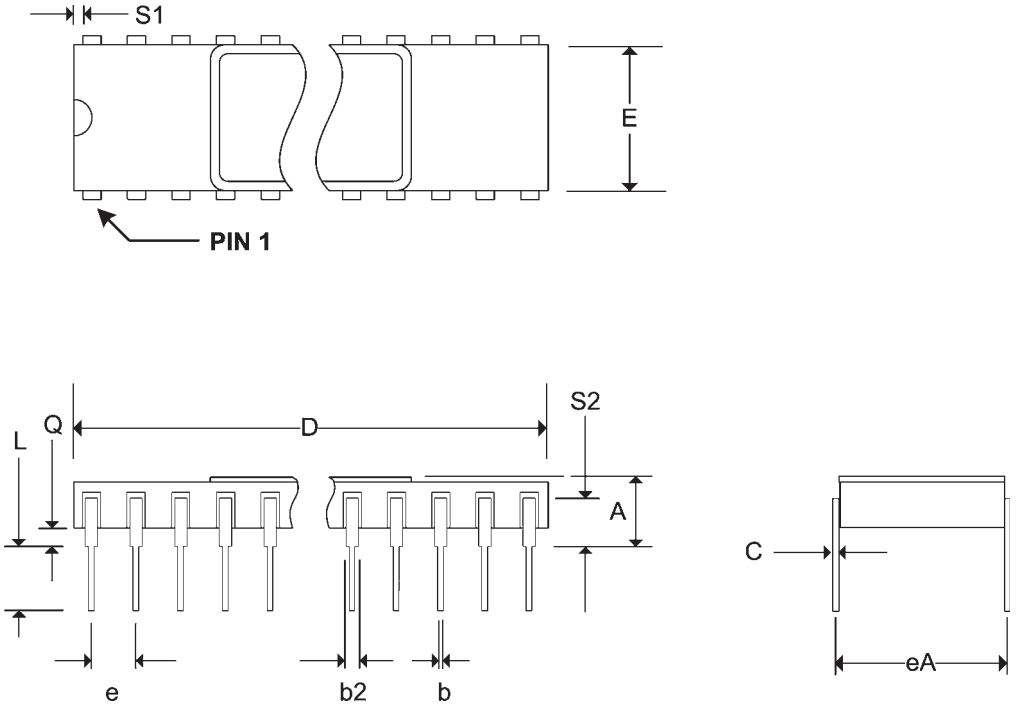
Temperature Range	Package	Speed (ns)					
		10	12	15	20	25	35
Commercial Temperature	Plastic DIP	-10PC	-12PC	-15PC	-20PC	-25PC	N/A
	Plastic SOIC	-10SC	-12SC	-15SC	-20SC	-25SC	N/A
Military Temperature	Side Brazed DIP	N/A	N/A	-15CM	-20CM	-25CM	-35CM
	CERDIP	N/A	N/A	-15DM	-20DM	-25DM	-35DM
	CERPACK	N/A	N/A	-15FM	-20FM	-25FM	-35FM
	LCC	N/A	N/A	-15LM	-20LM	-25LM	-35LM
Military Processed*	Side Brazed DIP	N/A	N/A	-15CMB	-20CMB	-25CMB	-35CMB
	CERDIP	N/A	N/A	-15DMB	-20DMB	-25DMB	-35DMB
	CERPACK	N/A	N/A	-15FMB	-20FMB	-25FMB	-35FMB
	LCC	N/A	N/A	-15LMB	-20LMB	-25LMB	-35LMB

* Military temperature range with MIL-STD-883, Class B processing.

N/A = Not Available

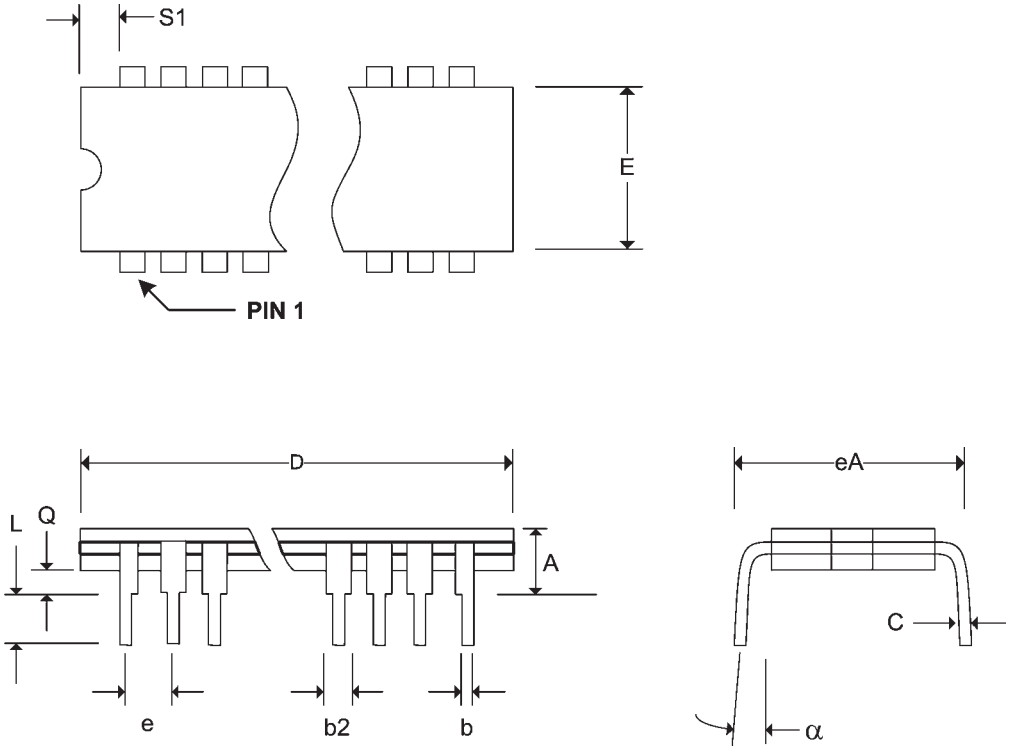
Pkg #	C4	
# Pins	24 (300 mil)	
Symbol	**Min**	**Max**
A	-	0.200
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.280
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-

SIDE BRAZED DUAL IN-LINE PACKAGE



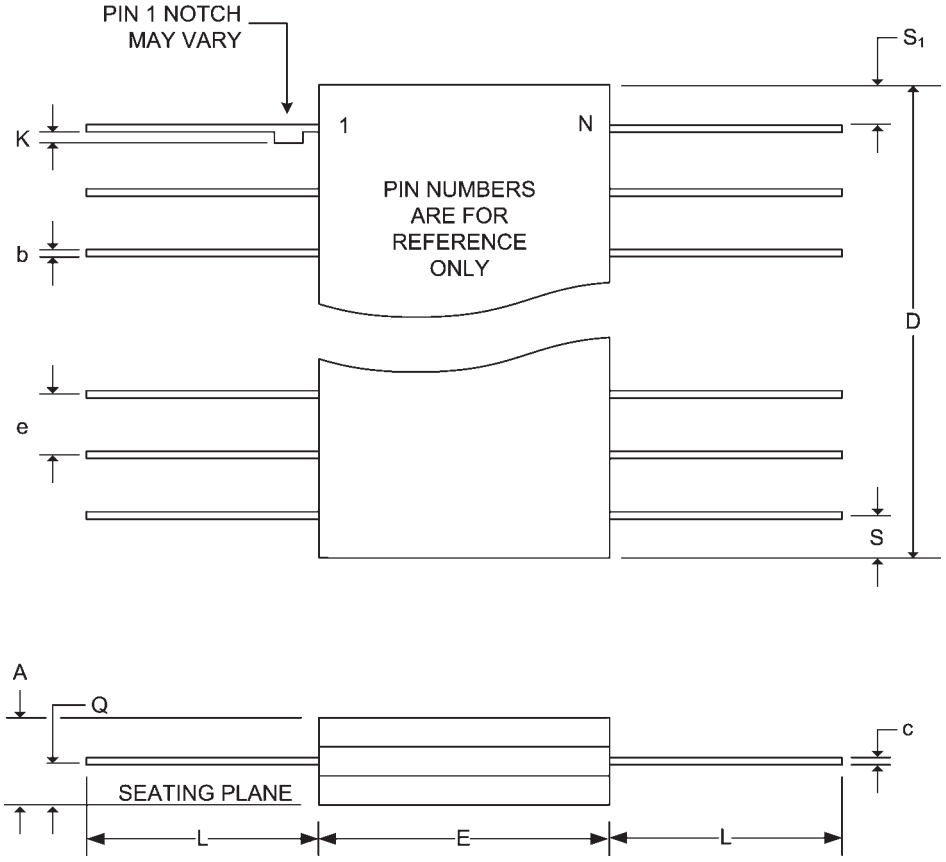
Pkg #	D4	
# Pins	24 (300 mil)	
Symbol	**Min**	**Max**
A	-	0.200
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.280
E	0.220	0.310
eA	0.300 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
α	0°	15°

CERDIP DUAL IN-LINE PACKAGE



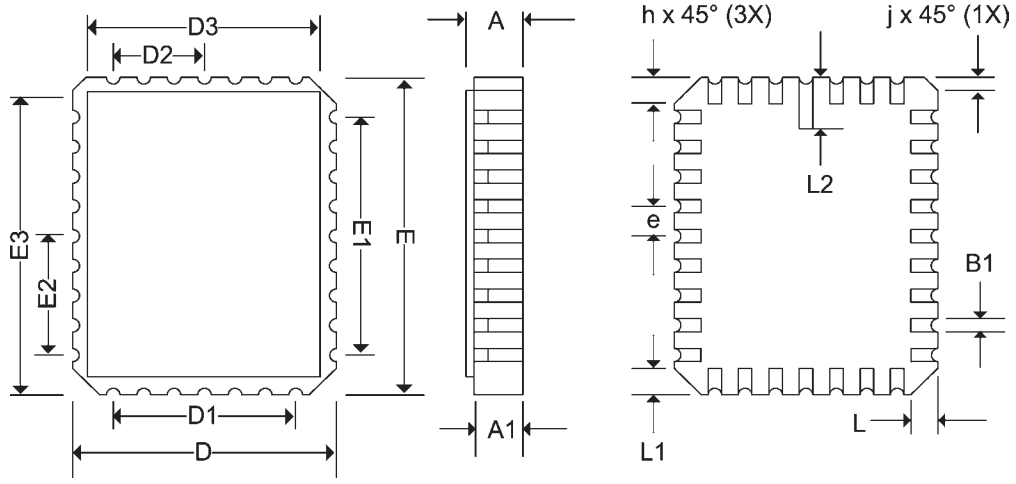
Pkg #	F3	
# Pins	24	
Symbol	**Min**	**Max**
A	0.060	0.090
b	0.015	0.022
c	0.004	0.009
D	-	0.630
E	0.330	0.380
e	0.050 BSC	
k	0.008	0.015
L	0.250	0.370
Q	0.026	0.045
S	-	0.085
S1	0.005	-

CERPACK CERAMIC FLAT PACKAGE



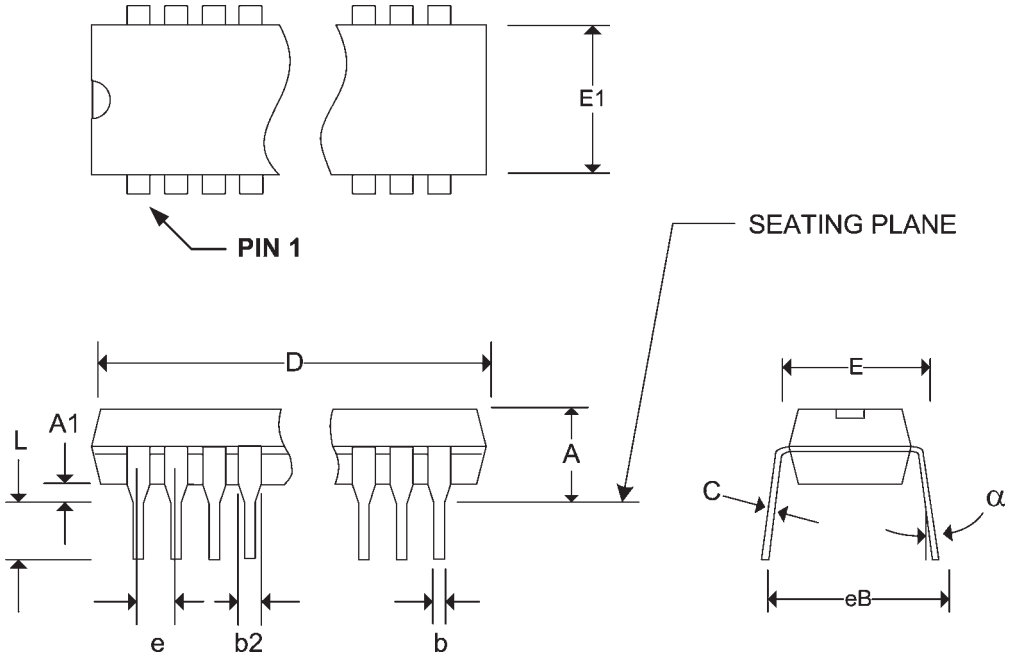
Pkg #	L5	
# Pins	28	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D	0.342	0.358
D1	0.200 BSC	
D2	0.100 BSC	
D3	-	0.358
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	-	0.558
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	5	
NE	9	

RECTANGULAR LEADLESS CHIP CARRIER



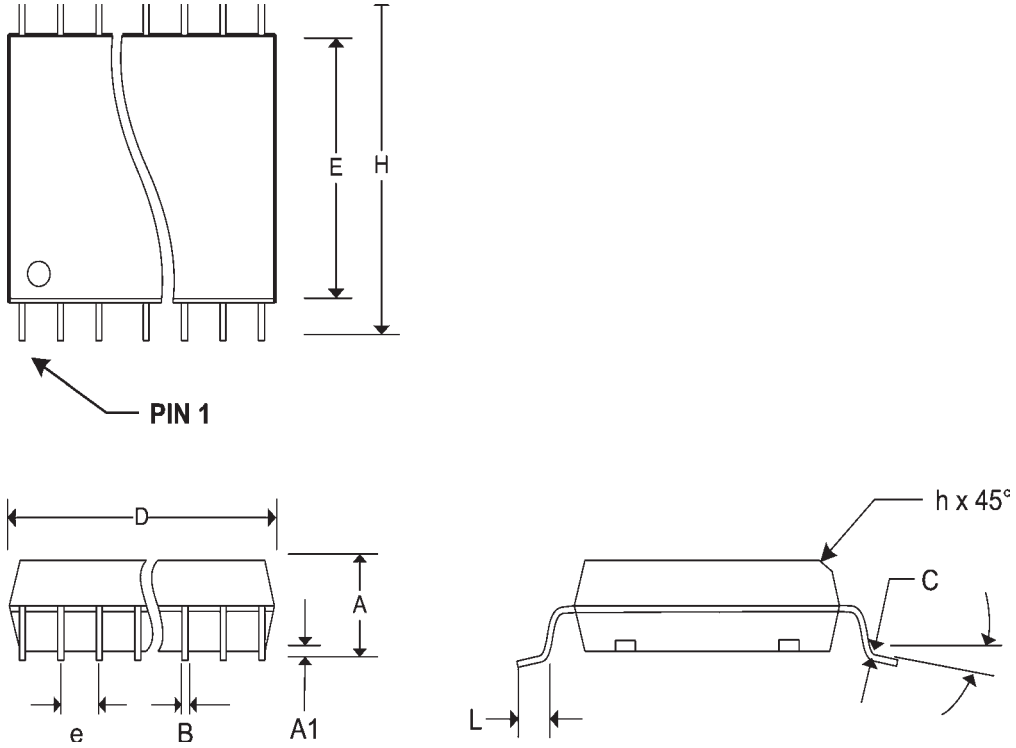
Pkg #	P4	
# Pins	24 (300 Mil)	
Symbol	**Min**	**Max**
A	-	0.210
A1	0.015	-
b	0.014	0.022
b2	0.045	0.070
C	0.008	0.014
D	1.230	1.280
E1	0.240	0.280
E	0.300	0.325
e	0.100 BSC	
eB	-	0.430
L	0.115	0.150
α	0°	15°

PLASTIC DUAL IN-LINE PACKAGE



Pkg #	S4	
# Pins	24 (300 Mil)	
Symbol	**Min**	**Max**
A	0.093	0.104
A1	0.004	0.012
b2	0.013	0.020
C	0.009	0.012
D	0.598	0.614
e	0.050 BSC	
E	0.291	0.299
H	0.394	0.419
h	0.010	0.029
L	0.016	0.050
α	0°	8°

SOIC/SOP SMALL OUTLINE IC PACKAGE



REVISIONS

DOCUMENT NUMBER:	SRAM105
DOCUMENT TITLE:	P4C150 ULTRA HIGH SPEED 1K x 4 RESETTABLE STATIC CMOS RAM

REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
OR	1997	DAB	New Data Sheet
A	Oct-05	JDB	Change logo to Pyramid