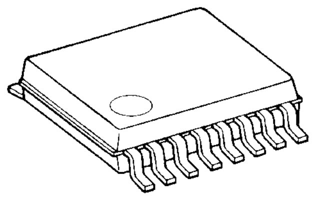
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC7MZ4051FK,TC7MZ4052FK,TC7MZ4053FK

TC7MZ4051FK 8-Channel Analog Multiplexer/Demultiplexer

TC7MZ4052FK Dual 4-Channel Analog Multiplexer/Demultiplexer

TC7MZ4053FK Triple 2-Channel Analog Multiplexer/Demultiplexer



Weight: 0.02 g (typ.)

The TC7MZ4051/4052/4053FK are high-speed, low-voltage drive analog multiplexer/demultiplexers using silicon gate CMOS technology. In 3 V and 5 V systems these can achieve high-speed operation with the low power dissipation that is a feature of CMOS.

The TC7MZ4051/4052/4053FK offer analog/digital signal selection as well as mixed signals. The 4051 has an 8-channel configuration, the 4052 has an 4-channel × 2 configuration, and the 4053 has a 2-channel × 3 configuration.

The switches for each channel are turned ON by the control pin digital signals.

Although the control signal logical amplitude (V_{CC} − GND) is small, the device can perform large-amplitude (V_{CC} − V_{EE}) signal switching.

For example, if V_{CC} = 3 V, GND = 0 V, and V_{EE} = −3 V, signals between −3 V and +3 V can be switched from the logical circuit using a single 3 V power supply.

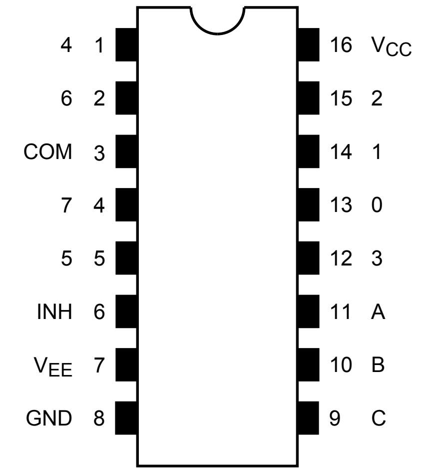
All input pins are equipped with a newly developed input protection circuit that avoids the need for a diode on the plus side (forward side from the input to the V_{CC}). As a result, for example, 5 V signals can be permitted on the inputs even when the power supply voltage to the circuits is off. As a result of this input power protection, the TC7MZ4051/4052/4053FK can be used in a variety of applications, including in the system which has two power supplies, and in battery backup circuits.

Features

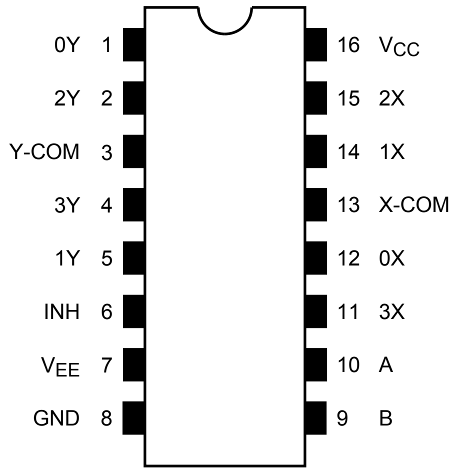
- Low ON resistance: R_{on} = 22 Ω (typ.) (V_{CC} − V_{EE} = 3 V)
  R_{on} = 15 Ω (typ.) (V_{CC} − V_{EE} = 6 V)
- High speed: t_{pd} = 3 ns (typ.) (V_{CC} = 3.0 V)
- Low power dissipation: I_{CC} = 4 μA (max) (Ta = 25°C)
- Input level: V_{IL} = 0.8 V (max) (V_{CC} = 3 V)
  V_{IH} = 2.0 V (min) (V_{CC} = 3 V)
- Power down protection is provided on all control inputs
- Pin and function compatible with 74HC4051/4052/4053

Pin Assignment (top view)

TC7MZ4051FK



TC7MZ4052FK



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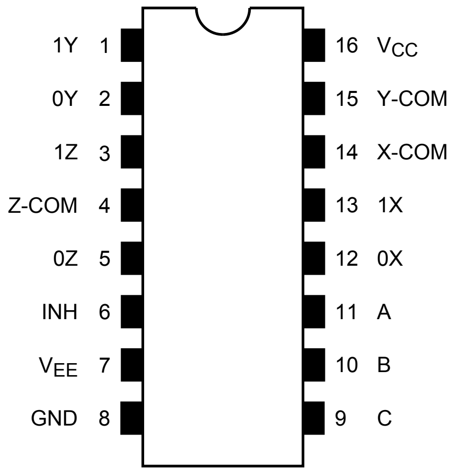


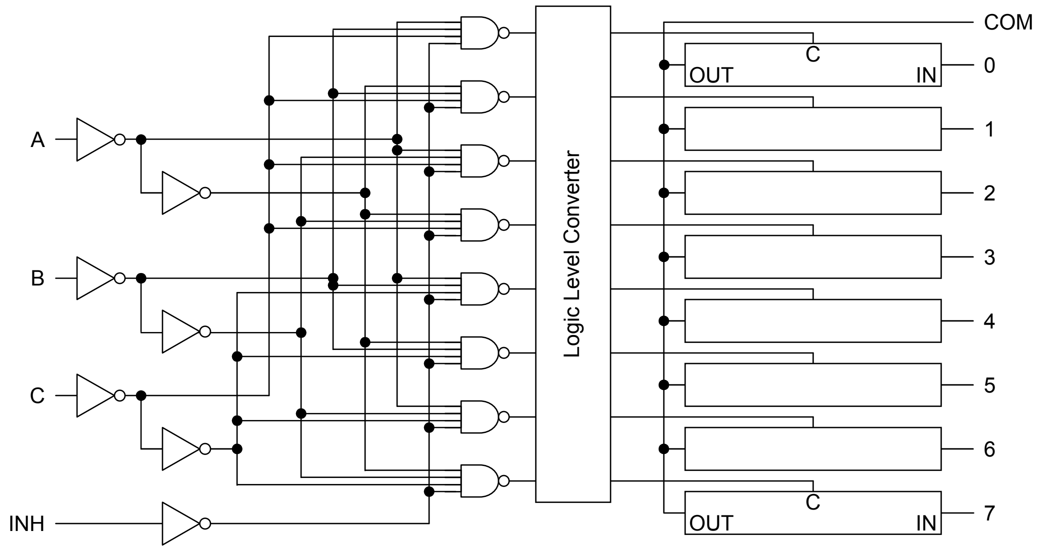
Truth Table

Control Inputs				"ON" Channel		
Inhibit	C*	B	A	MZ4051FK	MZ4052FK	MZ4053FK
L	L	L	L	0	0X, 0Y	0X, 0Y, 0Z
L	L	L	H	1	1X, 1Y	1X, 0Y, 0Z
L	L	H	L	2	2X, 2Y	0X, 1Y, 0Z
L	L	H	H	3	3X, 3Y	1X, 1Y, 0Z
L	H	L	L	4	—	0X, 0Y, 1Z
L	H	L	H	5	—	1X, 0Y, 1Z
L	H	H	L	6	—	0X, 1Y, 1Z
L	H	H	H	7	—	1X, 1Y, 1Z
H	X	X	X	None	None	None

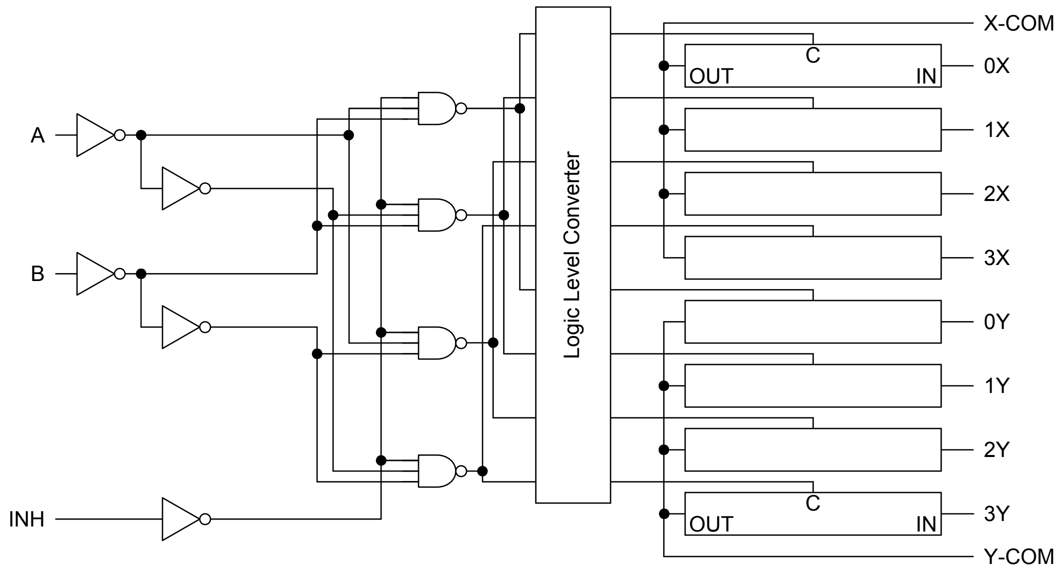
X: Don't care, *: Except MZ4052FK

System Diagram

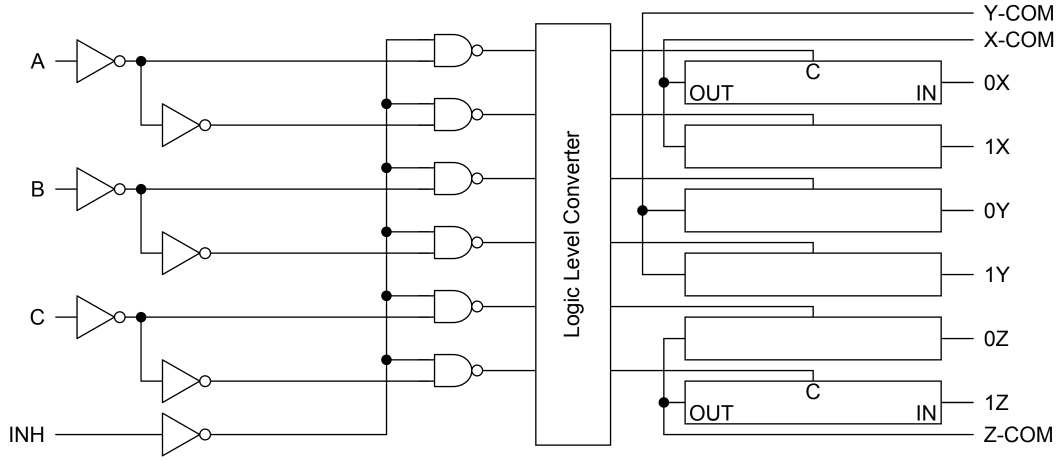
TC7MZ4051FK



TC7MZ4052FK



TC7MZ4053FK



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5~7.0	V
	V_{CC}~V_{EE}	−0.5~7.0	
Control input voltage	V_{IN}	−0.5~7.0	V
Switch I/O voltage	$V_{I/O}$	V_{EE} − 0.5~V_{CC} + 0.5	V
Input diode current	I_{IK}	−20	mA
I/O diode current	I_{IOK}	±20	mA
Switch through current	I_T	±25	mA
DC V_{CC} or ground current	I_{CC}	±50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65~150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Power supply voltage	V_{CC}	2~6	V
	V_{EE}	−4~0	
	V_{CC}~V_{EE}	2~6	
Input voltage	V_{IN}	0~6.0	V
Switch I/O voltage	$V_{I/O}$	V_{EE}~V_{CC}	V
Operating temperature	T_{opr}	−40~85	°C
Input rise and fall time	dt/dv	0~100 (V_{CC} = 3.3 ± 0.3 V)	ns/V
		0~20 (V_{CC} = 5 ± 0.5 V)	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused control inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Electrical Characteristics

Characteristics		Symbol	Test Condition			Ta = 25°C			Ta = –40~85°C		Unit
				V_{EE} (V)	V_{CC} (V)	Min	Typ.	Max	Min	Max	
Input voltage	High-level	V_{IH}	—		2.0	1.5	—	—	1.5	—	V
					3.0	2.0	—	—	2.0	—	
					4.5	3.15	—	—	3.15	—	
					6.0	4.2	—	—	4.2	—	
	Low-level	V_{IL}	—		2.0	—	—	0.5	—	0.5	
					3.0	—	—	0.8	—	0.8	
					4.5	—	—	1.35	—	1.35	
					6.0	—	—	1.8	—	1.8	
ON resistance		R_{ON}	$V_{IN} = V_{IL}$ or V_{IH} $V_{I/O} = V_{CC}$ to V_{EE} $I_{I/O} = 2$ mA	GND	2.0	—	200	—	—	—	Ω
				GND	3.0	—	45	86	—	108	
				GND	4.5	—	24	37	—	46	
				–3.0	3.0	—	17	26	—	33	
			$V_{IN} = V_{IL}$ or V_{IH} $V_{I/O} = V_{CC}$ or V_{EE} $I_{I/O} = 2$ mA	GND	2.0	—	28	73	—	84	
				GND	3.0	—	22	38	—	44	
				GND	4.5	—	17	27	—	31	
				–3.0	3.0	—	15	24	—	28	
Difference of ON resistance between switches		ΔR_{ON}	$V_{IN} = V_{IL}$ or V_{IH} $V_{I/O} = V_{CC}$ to V_{EE} $I_{I/O} = 2$ mA	GND	2.0	—	10	25	—	35	Ω
				GND	3.0	—	5	15	—	20	
				GND	4.5	—	5	13	—	18	
				–3.0	3.0	—	5	10	—	15	
Input/Output leakage current (switch OFF)		I_{OFF}	$V_{OS} = V_{CC}$ or GND V_{IS} = GND to V_{CC} $V_{IN} = V_{IL}$ or V_{IH}	GND	3.0	—	—	±0.25	—	±2.5	μA
				–3.0	3.0	—	—	±0.5	—	±5.0	
Input/Output leakage current (switch ON, output open)		I_{IN}	$V_{OS} = V_{CC}$ or GND $V_{IN} = V_{IL}$ or V_{IH}	GND	3.0	—	—	±0.25	—	±2.5	μA
				–3.0	3.0	—	—	±0.5	—	±5.0	
Control input current		I_{IN}	$V_{IN} = V_{CC}$ or GND	GND	6.0	—	—	±0.1	—	±0.1	μA
Quiescent supply current		I_{CC}	$V_{IN} = V_{CC}$ or GND	GND	3.0	—	—	4.0	—	40.0	μA
				–3.0	3.0	—	—	8.0	—	80.0	

AC Electrical Characteristics (C_L = 50 pF, Input: t_r = t_f = 3 ns, GND = 0 V)

Characteristics	Symbol	Test Condition		V_{EE} (V)	V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ.	Ta = 25°C Max	Ta = −40~85°C Min	Ta = −40~85°C Max	Unit
Phase difference between input and output	φI/O	All types		GND	2.0	—	3.2	6.0	—	6.9	ns
				GND	3.0	—	1.8	3.0	—	3.5	
				GND	4.5	—	1.3	1.8	—	2.1	
				−3.0	3.0	—	1.1	1.3	—	1.5	
Output enable time	t_{pZL} t_{pZH}	Figure 1 (Note 1)		GND	2.0	—	9.0	17	—	20	ns
				GND	3.0	—	5.7	9.0	—	11	
				GND	4.5	—	4.5	6.0	—	7.0	
				−3.0	3.0	—	5.8	8.0	—	10	
Output disable time	t_{pLZ} t_{pHZ}	Figure 1 (Note 1)		GND	2.0	—	13.5	21	—	25	ns
				GND	3.0	—	11.3	15	—	18	
				GND	4.5	—	10.3	12	—	14	
				−3.0	3.0	—	10.9	13	—	15	
Control input capacitance	C_{in}	All types (Note 2)		—	—	—	5	10	—	10	pF
COMMON terminal capacitance	C_{IS}	4051	Figure 2 (Note 2)	−3.0	3.0	—	11	25	—	25	pF
		4052					9	20		20	
		4053					7	15		15	
SWITCH terminal capacitance	C_{OS}	4051	Figure 2 (Note 2)	−3.0	3.0	—	6	13	—	13	pF
		4052					6	13		13	
		4053					6	13		13	
Feedthrough capacitance	C_{IOS}	4051	Figure 2 (Note 2)	−3.0	3.0	—	3	6	—	6	pF
		4052					3	6		6	
		4053					3	6		6	
Power dissipation capacitance	C_{PD}	4051	Figure 2 (Note 3)	GND	6.0	—	14	—	—	—	pF
		4052					24				
		4053					18				

Note 1: R_L = 1 kΩ

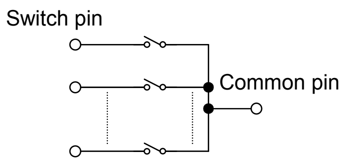
Note 2: C_{in}, C_{IS}, C_{OS} and C_{IOS} are guaranteed by the design.

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance of IC which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:
$I_{CC\ (opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

*Analog Switch Characteristics (GND = 0 V, Ta = 25°C)

Characteristics	Symbol	Test Condition		V_{EE} (V)	V_{CC} (V)	Typ.	Unit
Sine Wave Distortion (T.H.D)		R_L = 10 kΩ, C_L = 50 pF, f_{IN} = 1 kHz	V_{IN} = 2.0 V_{p-p}	0	3.0	0.100	%
			V_{IN} = 4.0 V_{p-p}	0	4.5	0.030	
			V_{IN} = 6.0 V_{p-p}	−0.3	3.0	0.020	
Frequency response (switch ON)	f_{max}	Adjust f_{IN} voltage to obtain 0dBm at V_{OS}. Increase f_{IN} frequency until dB meter reads −3dB. R_L = 50 Ω, C_L = 10 pF, f_{IN} = 1 MHz, sine wave Figure 3	4051	0	3.0	150	MHz
			4052			180	
			4053			200	
			4051	0	4.5	150	
			4052			180	
			4053			200	
			4051	−3.0	3.0	150	
			4052			180	
			4053			200	
Feed through attenuation (switch OFF)		V_{IN} is centered at (V_{CC} − V_{EE})/2. Adjust input for 0dBm. R_L = 600 Ω, C_L = 50 pF, f_{IN} = 1 MHz, sine wave Figure 4		0	3.0	−45	dB
				0	4.5	−45	
				−3.0	3.0	−45	
		R_L = 50 Ω, C_L = 10 pF, f_{IN} = 1 MHz, sine wave		0	3.0	−60	
				0	4.5	−60	
				−3.0	3.0	−60	
Crosstalk (control input to signal output)		R_L = 600 Ω, C_L = 50 pF, f_{IN} = 1 MHz, square wave (t_r = t_f = 6 ns) Figure 5		0	3.0	90	mV
				0	4.5	150	
				−3.0	3.0	120	
Crosstalk (between any switches)		Adjust V_{IN} to obtain 0dBm at input. R_L = 600 Ω, C_L = 50 pF, f_{IN} = 1 MHz, sine wave Figure 6		0	3.0	−45	dB
				0	4.5	−45	
				−3.0	3.0	−45	

*: These characteristics are determined by design of devices.



AC Test Circuit

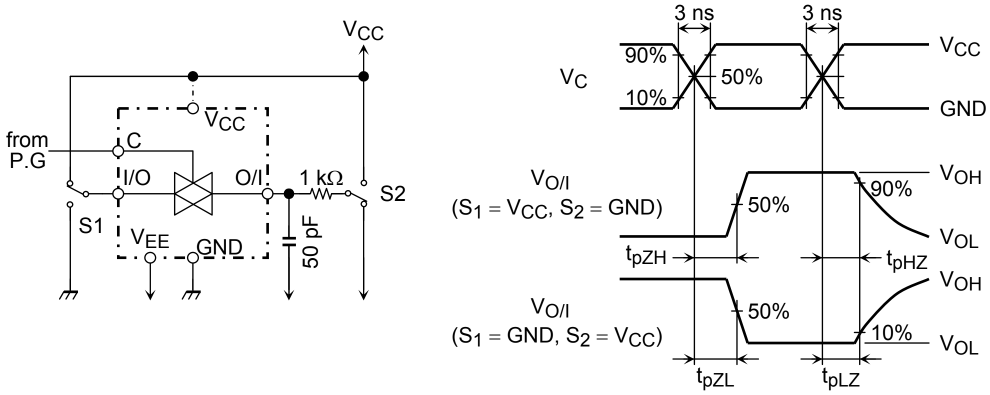


Figure 1 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}

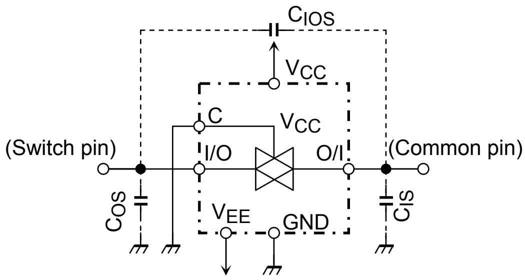


Figure 2 C_{IOS}, C_{IS}, C_{OS}

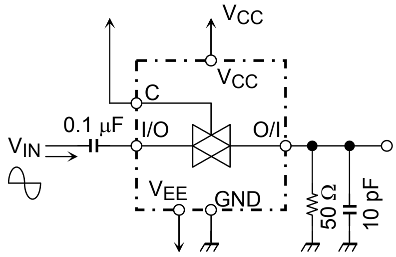


Figure 3 Frequency Response (switch on)

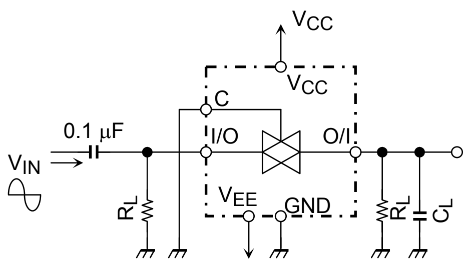


Figure 4 Feedthrough

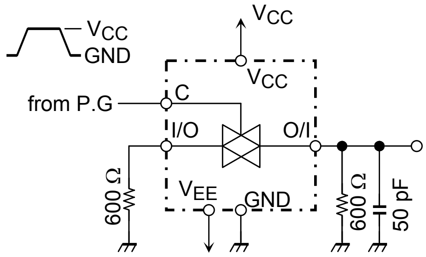


Figure 5 Cross Talk (control input to output signal)

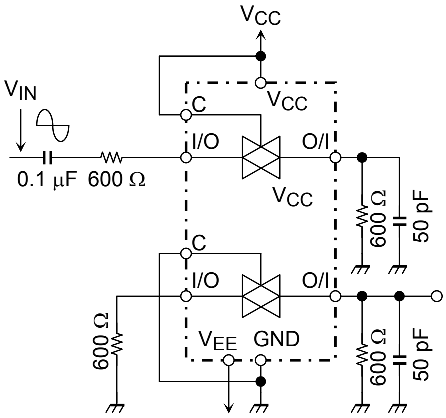
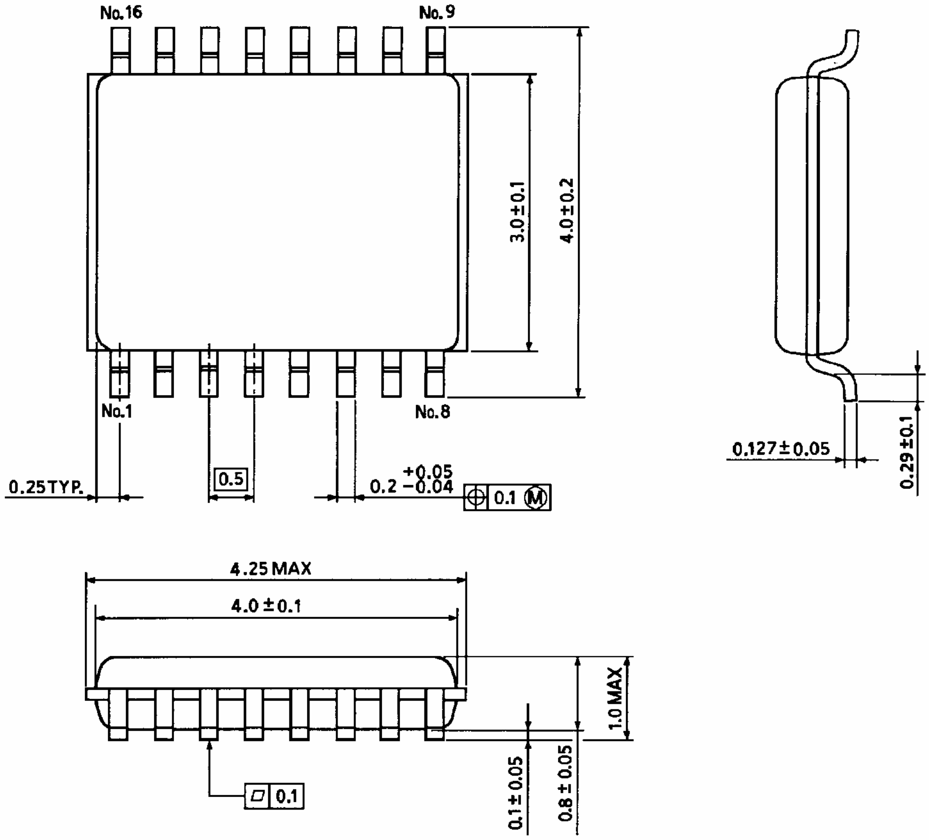


Figure 6 Cross Talk (between any two switches)

Package Dimensions

VSSOP16-P-0030-0.50 Unit : mm



Weight: 0.02 g (typ.)

RESTRICTIONS ON PRODUCT USE

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