

TOSHIBA Field-Effect Transistor Silicon P-Channel MOS Type

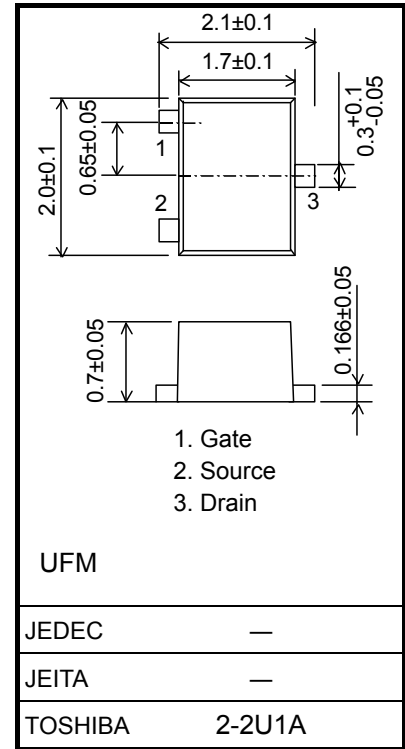
# SSM3J109TU

○ Power Management Switch Applications

○ High-Speed Switching Applications

- 1.8 V drive
- Low ON-resistance:  $R_{on} = 300 \text{ m}\Omega$  (max) (@ $V_{GS} = -1.8 \text{ V}$ )  
 $R_{on} = 172 \text{ m}\Omega$  (max) (@ $V_{GS} = -2.5 \text{ V}$ )  
 $R_{on} = 130 \text{ m}\Omega$  (max) (@ $V_{GS} = -4.0 \text{ V}$ )

Unit: mm



Weight: 6.6 mg (typ.)

## Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	$V_{DS}$	-20	V
Gate-source voltage	$V_{GS}$	$\pm 8$	V
Drain current	DC	$I_D$	-2
	Pulse	$I_{DP}$	-4
Drain power dissipation	$P_D$ (Note 1)	800	mW
	$P_D$ (Note 2)	500	
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55~150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 1: Mounted on a ceramic board  
(25.4 mm × 25.4 mm × 0.8 t, Cu Pad: 645 mm<sup>2</sup>)

Note 2: Mounted on an FR4 board  
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm<sup>2</sup>)

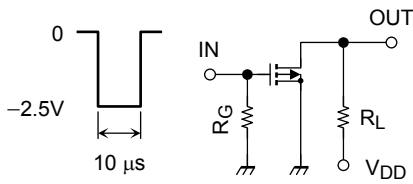
## Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Condition	Min	Typ.	Max	Unit	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1 \text{ mA}, V_{GS} = 0$	-20	—	—	V	
	$V_{(BR)DSX}$	$I_D = -1 \text{ mA}, V_{GS} = +8 \text{ V}$	-12	—	—		
Drain cutoff current	$I_{DSS}$	$V_{DS} = -20 \text{ V}, V_{GS} = 0$	—	—	-10	μA	
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0$	—	—	$\pm 1$	μA	
Gate threshold voltage	$V_{th}$	$V_{DS} = -3 \text{ V}, I_D = -1 \text{ mA}$	-0.3	—	-1.0	V	
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -3 \text{ V}, I_D = -1 \text{ A}$ (Note 3)	2.4	4	—	S	
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = -1.0 \text{ A}, V_{GS} = -4 \text{ V}$ (Note 3)	—	91	130	mΩ	
		$I_D = -0.5 \text{ A}, V_{GS} = -2.5 \text{ V}$ (Note 3)	—	123	172		
		$I_D = -0.2 \text{ A}, V_{GS} = -1.8 \text{ V}$ (Note 3)	—	175	300		
Input capacitance	$C_{iss}$	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	335	—	pF	
Output capacitance	$C_{oss}$	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	70	—	pF	
Reverse transfer capacitance	$C_{rss}$	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	56	—	pF	
Switching time	Turn-on time	$t_{on}$	$V_{DD} = -10 \text{ V}, I_D = -1 \text{ A},$	—	20	—	ns
	Turn-off time	$t_{off}$	$V_{GS} = 0 \sim -2.5 \text{ V}, R_G = 4.7 \Omega$	—	20	—	
Drain-source forward voltage	$V_{DSF}$	$I_D = 2 \text{ A}, V_{GS} = 0$ (Note 3)	—	0.85	1.2	V	

Note 3: Pulse test

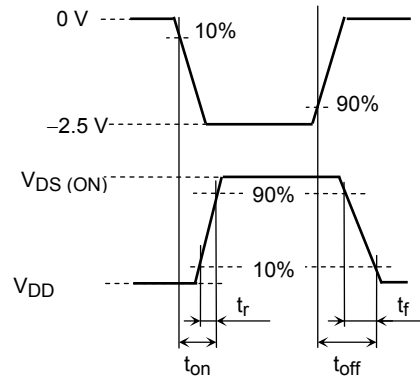
**Switching Time Test Circuit**

**(a) Test circuit**



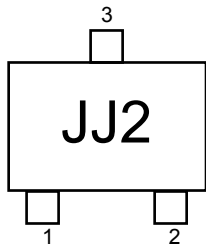
$V_{DD} = -10\text{ V}$   
 $R_G = 4.7\ \Omega$   
 Duty  $\leq 1\%$   
 $V_{IN}$ :  $t_r, t_f < 5\text{ ns}$   
 Common Source  
 $T_a = 25^\circ\text{C}$

**(b)  $V_{IN}$**

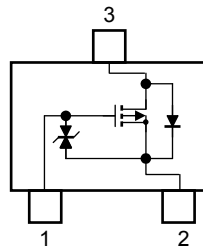


**(c)  $V_{OUT}$**

**Marking**



**Equivalent Circuit (top view)**



**Notice on Usage**

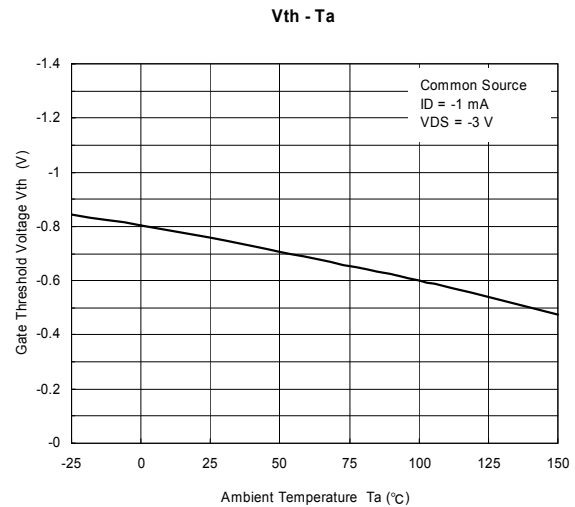
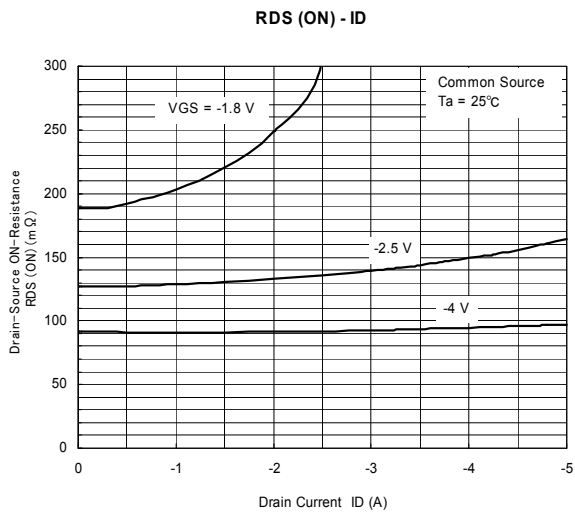
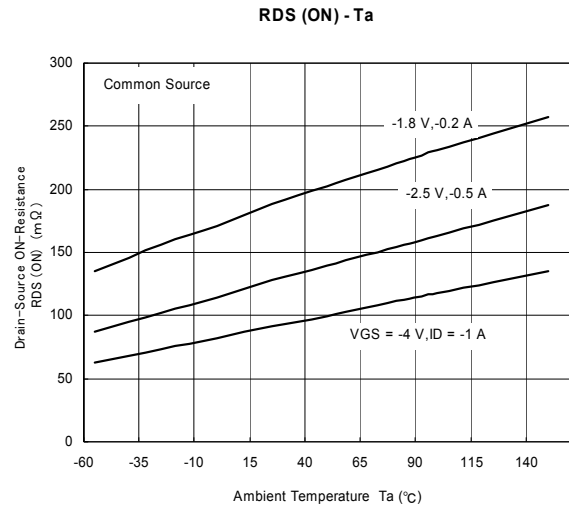
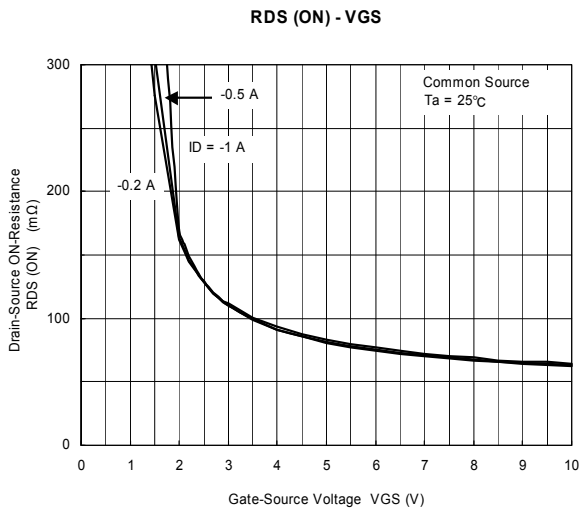
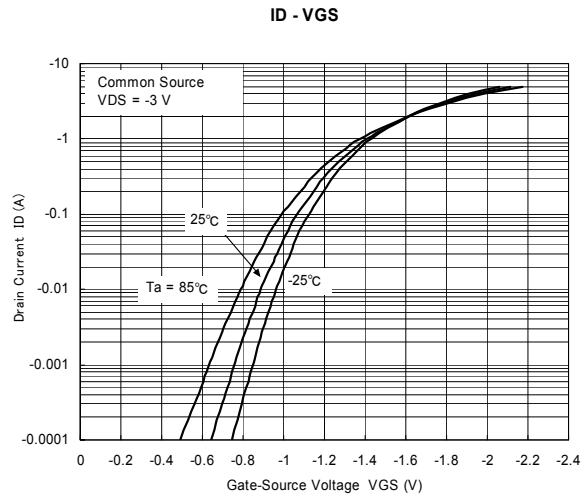
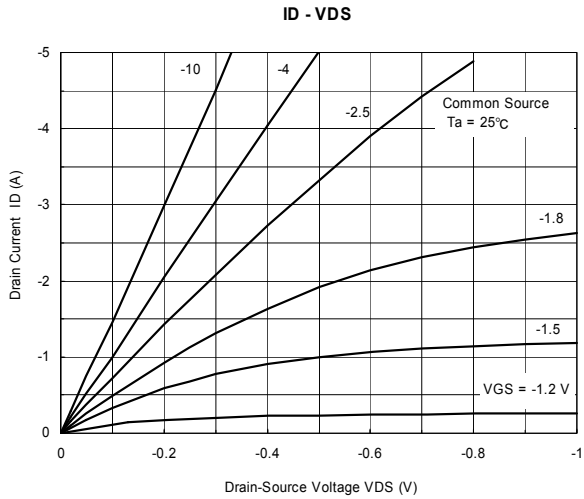
$V_{th}$  can be expressed as the voltage between gate and source when the low operating current value is  $I_D = -1\text{ mA}$  for this product. For normal switching operation,  $V_{GS(ON)}$  requires a higher voltage than  $V_{th}$  and  $V_{GS(OFF)}$  requires a lower voltage than  $V_{th}$ .

(The relationship can be established as follows:  $V_{GS(OFF)} < V_{th} < V_{GS(ON)}$ .)

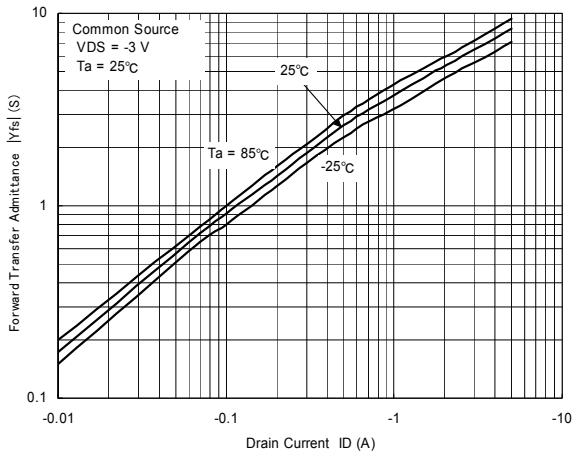
Take this into consideration when using the device.

**Handling Precaution**

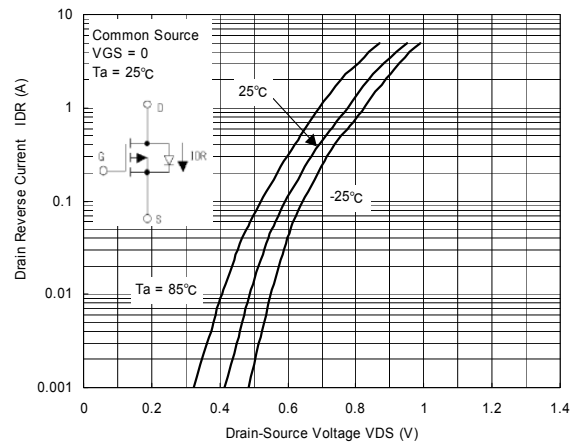
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.



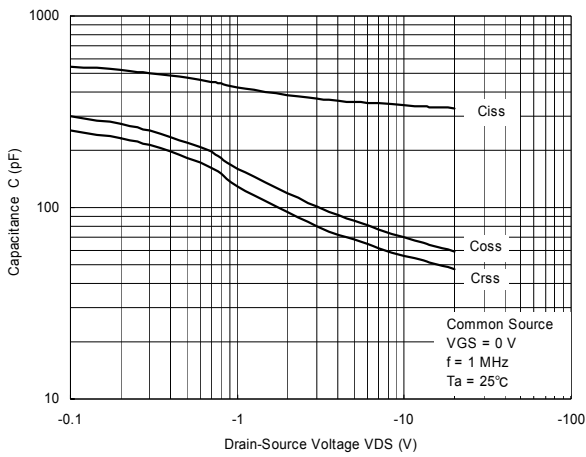
**|Yfs| - ID**



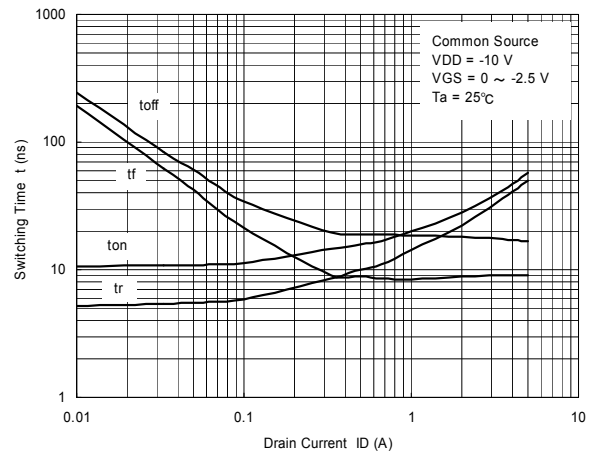
**IDR - VDS**



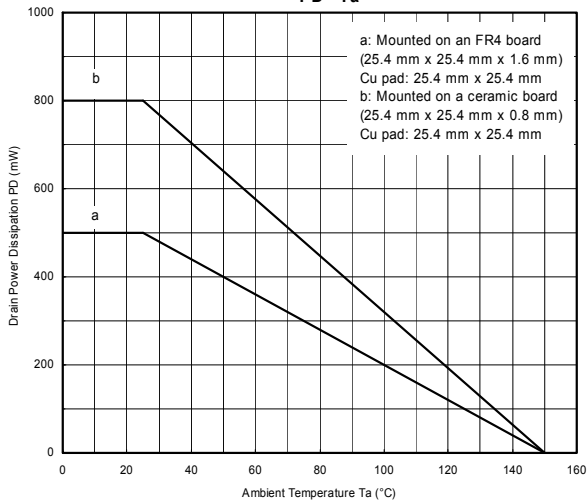
**C - VDS**



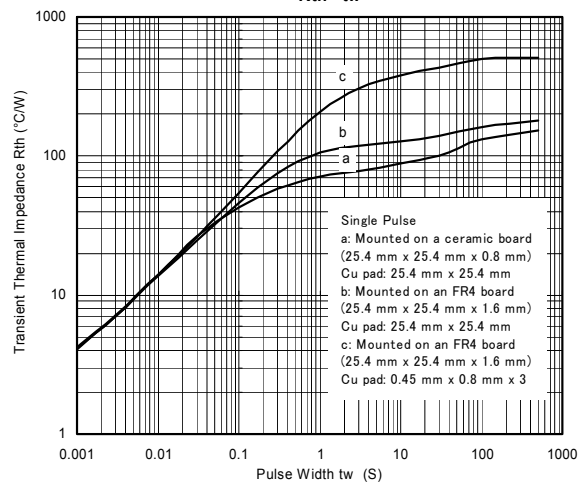
**t - ID**



**PD - Ta**



**Rth - tw**



**RESTRICTIONS ON PRODUCT USE**

20070701-EN GENERAL

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