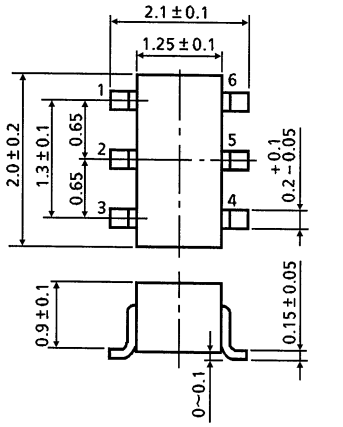
TOSHIBA Field Effect Transistor Silicon N·P Channel MOS Type

HN1L02FU

High Speed Switching Applications
Analog Switch Applications

Unit in mm



JEDEC	—
EIAJ	—
TOSHIBA	2-2J1C

Weight: 6.8mg

Q1, Q2 common

- 2.5V gate drive
- Low threshold voltage
  Q1: V_{th} = 0.5~1.5V Q2: V_{th} = −0.5~−1.5V
- High speed
- Small package

Q1 Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Drain-Source voltage	V_{DS}	20	V
Gate-Source voltage	V_{GSS}	10	V
Drain current	I_D	50	mA

Q2 Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Drain-Source voltage	V_{DS}	−20	V
Gate-Source voltage	V_{GSS}	−7	V
Drain current	I_D	−50	mA

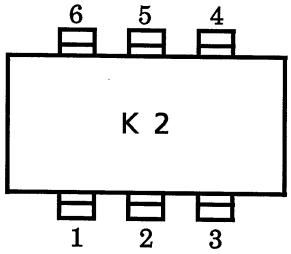
Absolute Maximum Ratings (Q1, Q2 Common) (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Drain power dissipation	P_{D*}	200	mW
Channel temperature	T_{ch}	150	°C
Storage temperature range	T_{stg}	−55~150	°C

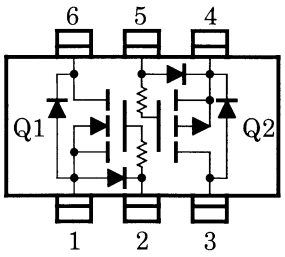
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

* Total rating

Marking



Equivalent Circuit (Top View)



Q1 Electrical Characteristics (Ta = 25°C)

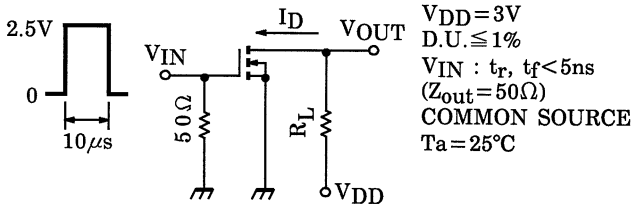
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = 10V, V_{DS} = 0	—	—	1	μA
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 100μA, V_{GS} = 0	20	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = 20V, V_{GS} = 0	—	—	1	μA
Gate threshold voltage		V_{th}	V_{DS} = 3V, I_D = 0.1mA	0.5	—	1.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 3V, I_D = 10mA	20	—	—	mS
Drain-Source ON resistance		$R_{DS\ (ON)}$	I_D = 10mA, V_{GS} = 2.5V	—	20	40	Ω
Input capacitance		C_{iss}	V_{DS} = 3V, V_{GS} = 0, f = 1MHz	—	5.5	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = 3V, V_{GS} = 0, f = 1MHz	—	1.6	—	pF
Output capacitance		C_{oss}	V_{DS} = 3V, V_{GS} = 0, f = 1MHz	—	6.5	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = 3V, I_D = 10mA, V_{GS} = 0~2.5V	—	0.14	—	μs
	Turn-off time	t_{off}	V_{DD} = 3V, I_D = 10mA, V_{GS} = 0~2.5V	—	0.14	—	μs

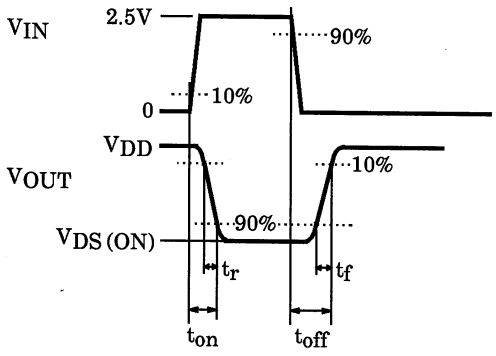
Q2 Electrical Characteristics (Ta = 25°C)

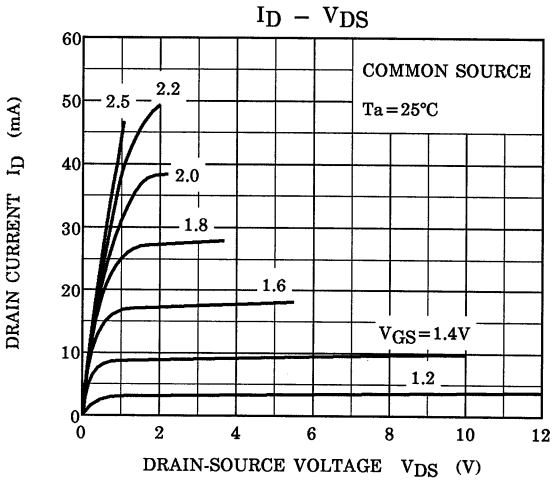
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = −7V, V_{DS} = 0	—	—	−1	μA
Drain-Source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −100μA, V_{GS} = 0	−20	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = −20V, V_{GS} = 0	—	—	−1	μA
Gate threshold voltage		V_{th}	V_{DS} = −3V, I_D = −0.1mA	−0.5	—	−1.5	V
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −3V, I_D = −10mA	15	—	—	mS
Drain-Source ON resistance		$R_{DS\ (ON)}$	I_D = −10mA, V_{GS} = −2.5V	—	20	40	Ω
Input capacitance		C_{iss}	V_{DS} = −3V, V_{GS} = 0, f = 1MHz	—	10.4	—	pF
Reverse transfer capacitance		C_{rss}	V_{DS} = −3V, V_{GS} = 0, f = 1MHz	—	2.8	—	pF
Output capacitance		C_{oss}	V_{DS} = −3V, V_{GS} = 0, f = 1MHz	—	8.4	—	pF
Switching time	Turn-on time	t_{on}	V_{DD} = −3V, I_D = −10mA, V_{GS} = 0~−2.5V	—	0.15	—	μs
	Turn-off time	t_{off}	V_{DD} = −3V, I_D = −10mA, V_{GS} = 0~−2.5V	—	0.13	—	μs

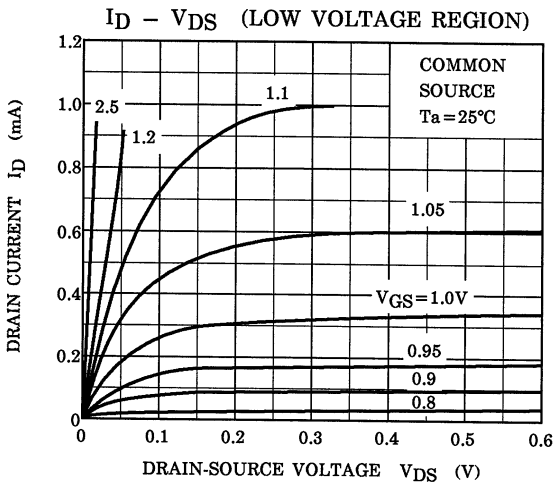
Q1 (Nch MOS FET)

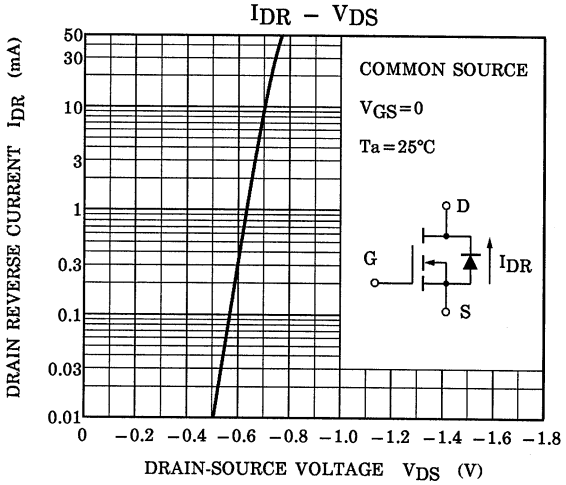
Switching Time Test Circuit

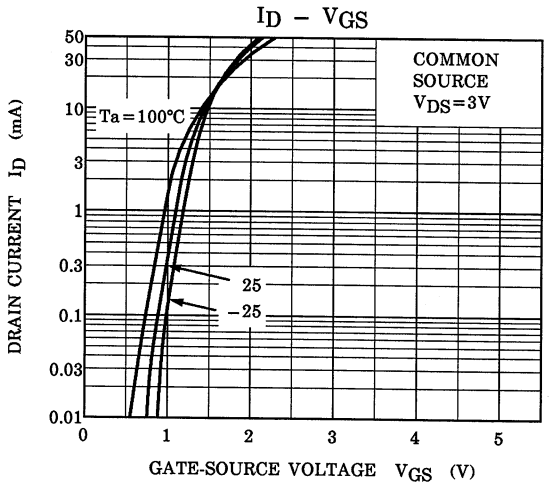




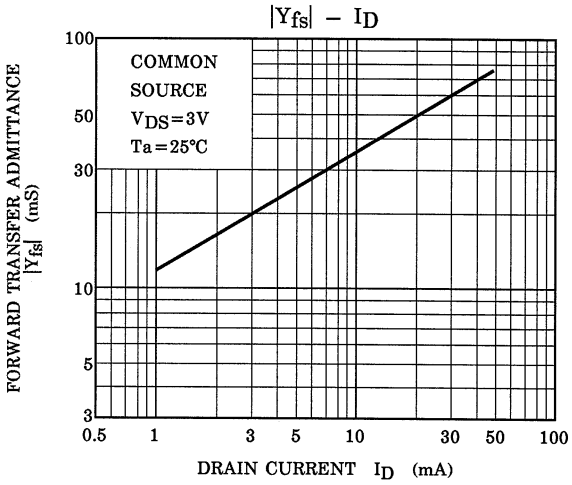


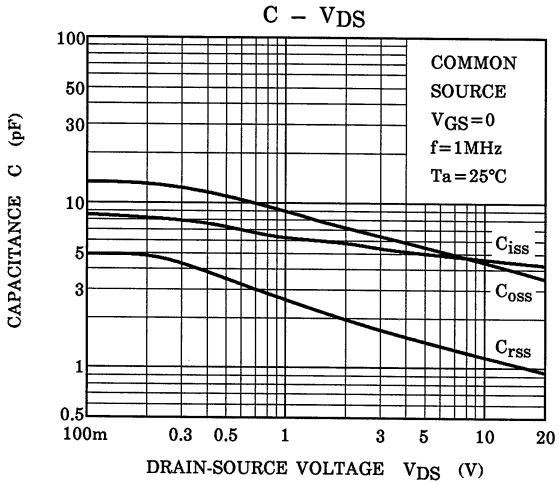


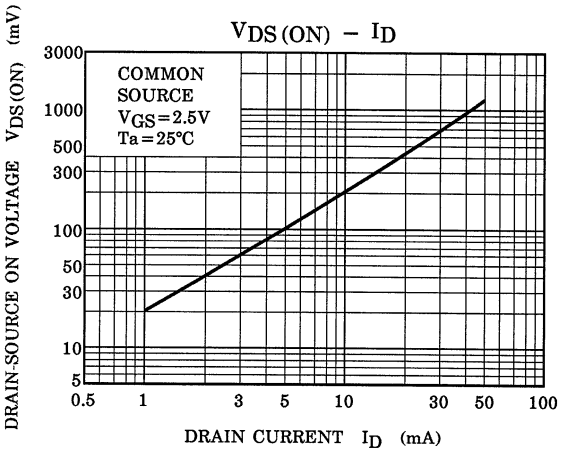


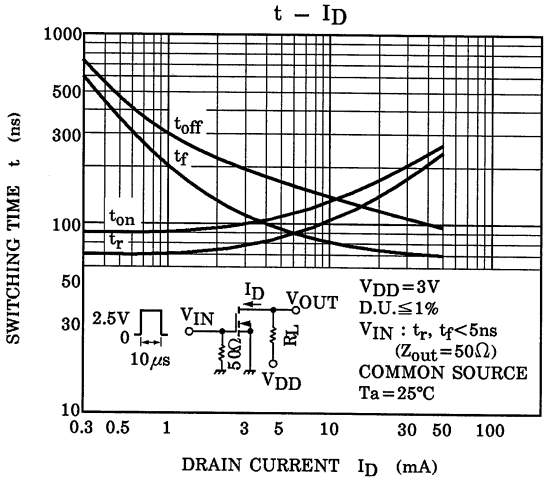


Q1 (Nch MOS FET)



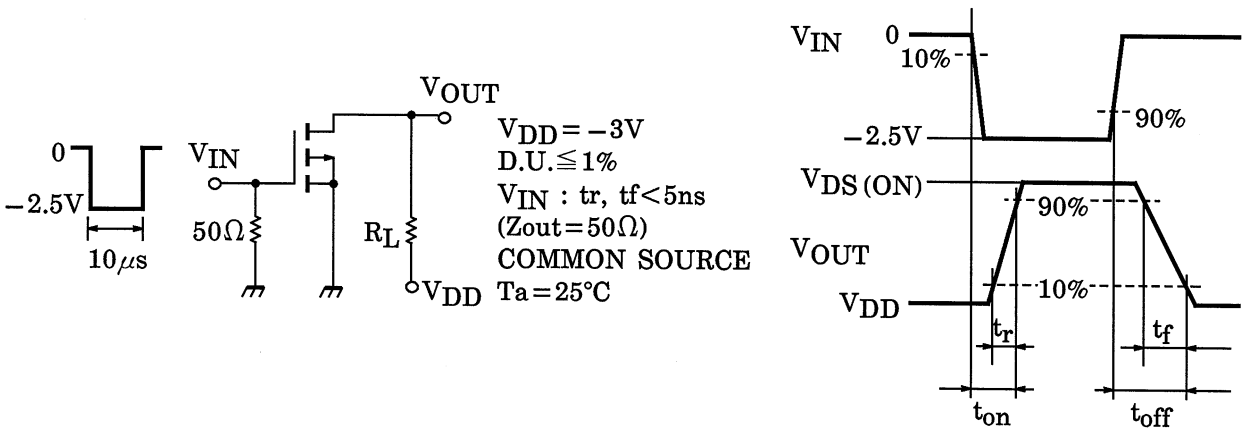


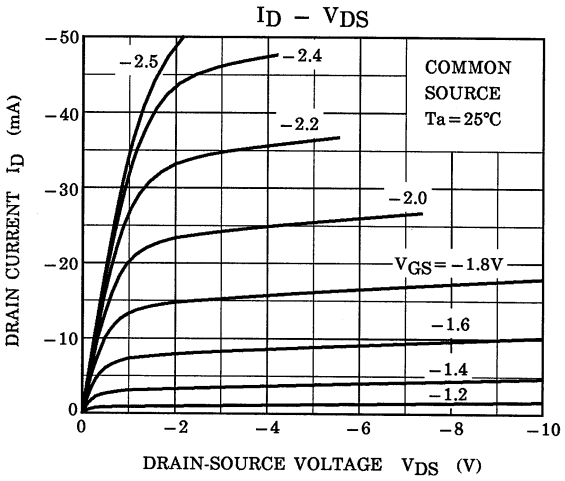


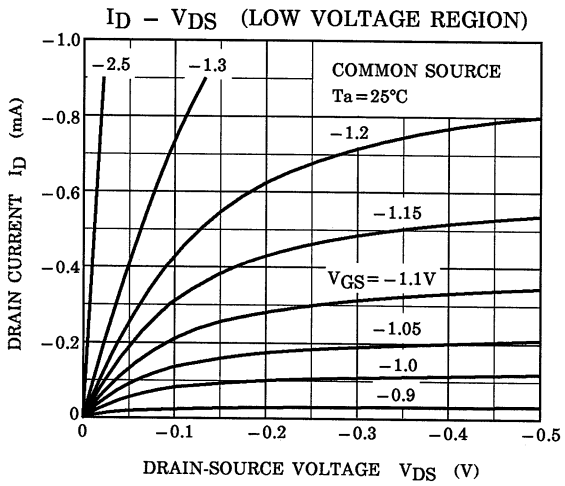


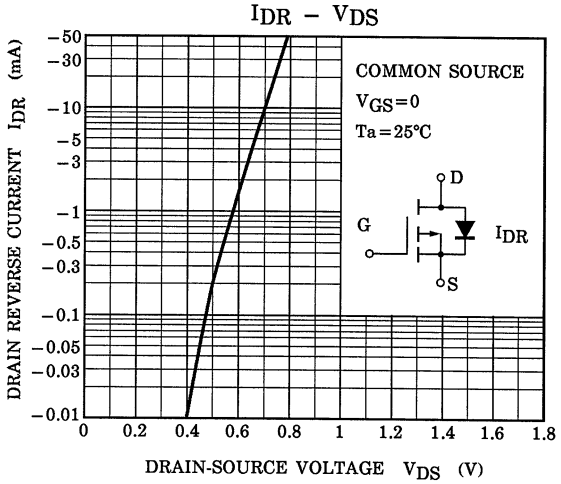
Q2 (Pch MOS FET)

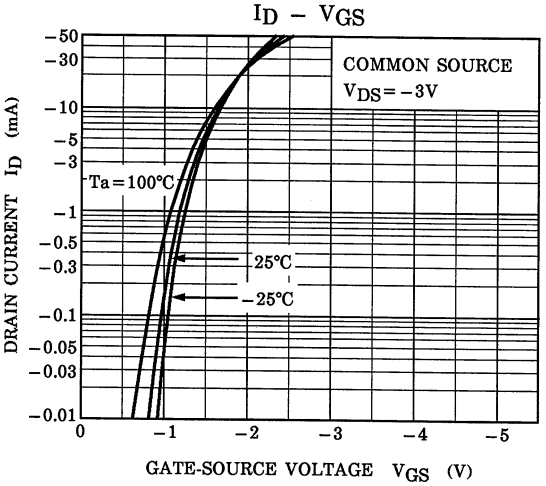
Switching Time Test Circuit





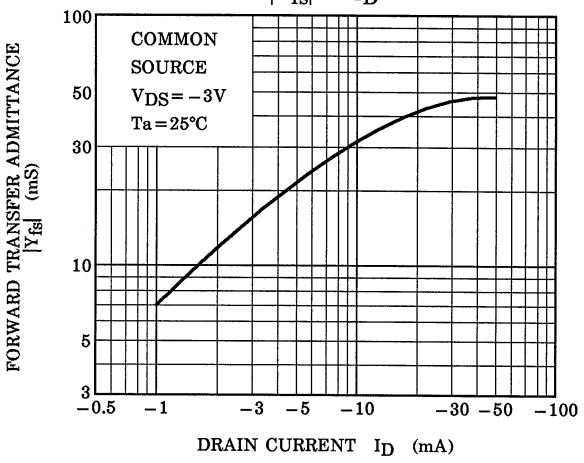




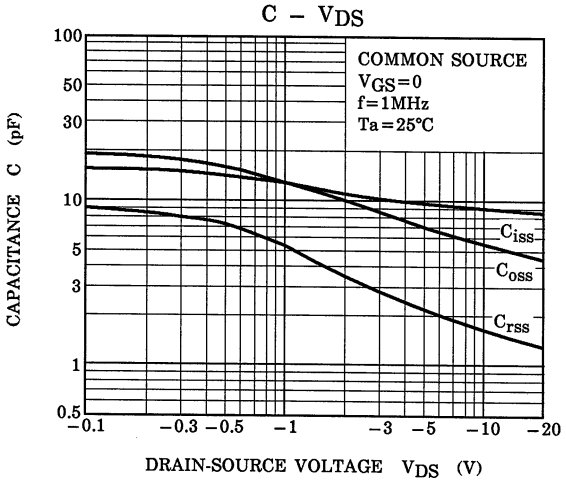


Q2 (Pch MOS FET)

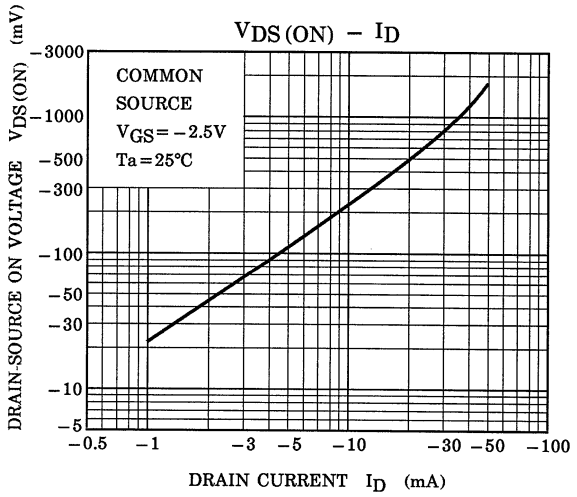
$|Y_{fs}|$ – I_D



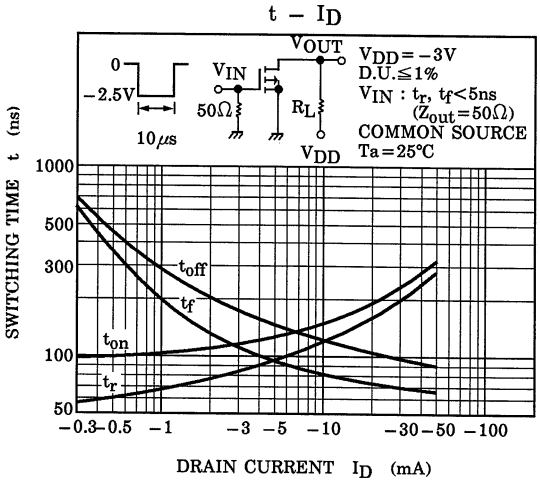
C – V_{DS}



$V_{DS\,(ON)}$ – I_D

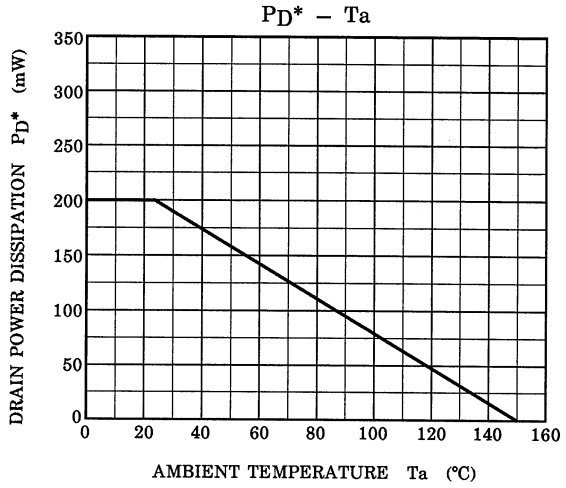


t – I_D



(Q1, Q2 common)

P_D* – Ta



* : Total Rating

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20070701-EN GENERAL

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