DRPIC1655X

High Performance Configurable 8-bit RISC Microcontroller ver 2.15

OVERVIEW

The DRPIC1655X is a low-cost, high performance, 8-bit, fully static soft IP Core, dedicated for operation with **fast** (typically on-chip) dual ported **memory**. The core has been designed with a special concern about **low power consumption**.

DRPIC1655X soft core is software-compatible with the industry standard PIC16C554 and PIC16C558. It implements an **enhanced Harvard architecture** (i.e. separate instruction and data memories) with independent address and data buses. The 14 bit program memory and 8-bit dual port data memory allow instruction fetch and data operations to occur simultaneously. The advantage of this architecture is that instruction fetch and memory transfers can be overlapped by multi stage pipeline, so that the next instruction can be fetched from program memory while the current instruction is executed with data from the data memory. The DRPIC1655X architecture is **4 times faster** compared to standard architecture. So most instructions are executed within **1 system clock period**, except the instructions which directly operates on program counter PC (GOTO, CALL, RETURN), this situation require the pipeline to be cleared and subsequently refilled. This operation takes additional one clock cycle.

The DRPIC1655X Microcontroller fits perfectly in applications ranging from high-speed automotive and appliance motor control to low-power remote transmitters/receivers, pointing devices and telecom processors. Built-in power save mode make this IP perfect for applications where power consumption is critical.

DRPIC1655X is delivered with **fully automated testbench** and **complete set of tests** allowing easy package validation at each stage of SoC design flow

CPU FEATURES

- Software compatible with industry standard PIC16C55X
- Pipelined Harvard architecture 4 times faster compared to original implementation
- 35 instructions
- 14 bit wide instruction word
- Up to 32 K bytes of internal Data Memory
- Up to 64K bytes of Program Memory
- Configurable hardware stack
- Power saving SLEEP mode
- Fully synthesizable, static synchronous design with no internal tri-states
- Technology independent HDL Source Code
- **1.4 GHz virtual** clock frequency in a 0.18u technological process

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PERIPHERALS

- Four 8 bit I/O ports
  - *Four 8-bit corresponding TRIS registers*
  - *Interrupt feature on PORTB(7:4) change*
- Timer 0
  - *8-bit timer/counter*
  - *Readable and Writable*
  - *8-bit software programmable prescaler*
  - *Internal or external clock select*
  - *Interrupt generation on timer overflow*
  - *Edge select for external clock*
- Watchdog Timer
  - *Configurable Time out period*
  - *7-bit software programmable prescaler*
  - *Dedicated independent Watchdog Clock input*
- Extended Interrupt Controller
  - *Three individually maskable Interrupt sources*
    - *External interrupt INT*
    - *Timer Overflow interrupt*
    - *Port B[7:4] change interrupt*
- DoCD™ debug unit
  - *Processor execution control*
    - *Run*
    - *Halt*
    - *Step into instruction*
    - *Skip instruction*
  - *Read-write all processor contents*
    - *Program Counter (PC)*
    - *Program Memory*
    - *Data Memory*
    - *Special Function Registers (SFRs)*
    - *Hardware Stack and Stack Pointer*
  - *Hardware execution breakpoints*
    - *Program Memory*
    - *Data Memory*
    - *Special Function Registers (SFRs)*
  - *Hardware breakpoints activated at a certain*
    - *Program address (PC)*
    - *Address by any write into memory*
    - *Address by any read from memory*
    - *Address by write into memory a required data*
    - *Address by read from memory a required data*
  - *Three wire communication interface*

DELIVERABLES

- Source code:
  - VHDL Source Code or/and
  - VERILOG Source Code or/and
  - Encrypted, or plain text EDIF netlist
- VHDL & VERILOG test bench environment
  - Active-HDL automatic simulation macros
  - ModelSim automatic simulation macros
  - Tests with reference responses
- Technical documentation
  - Installation notes
  - HDL core specification
  - Datasheet
- Synthesis scripts
- Example application
- Technical support
  - IP Core implementation support
  - 3 months maintenance
    - Delivery the IP Core updates, minor and major versions changes
    - Delivery the documentation updates
    - Phone & email support

CONFIGURATION

The following parameters of the DRPIC1655X core can be easy adjusted to requirements of dedicated application and technology. Configuration of the core can be prepared by effortless changing appropriate constants in package file. There is no need to change any parts of the code.

• Number of hardware stack levels	- 1-16 - default 8
• Memories type	- synchronous - asynchronous
• SLEEP mode	- used - unused
• WATCHDOG Timer	- used / width - unused
• Timer system	- used - unused
• Interrupt system	- used - unused
• PORTS A,B,C,D	- used - unused
• DoCD™ Debug Unit	- used - unused

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LICENSING

Comprehensible and clearly defined licensing methods without royalty fees make using of IP Core easy and simply.

Single Design license allows use IP Core in single FPGA bitstream and ASIC implementation.

Unlimited Designs, *One Year* licenses allow use IP Core in unlimited number of FPGA bitstreams and ASIC implementations.

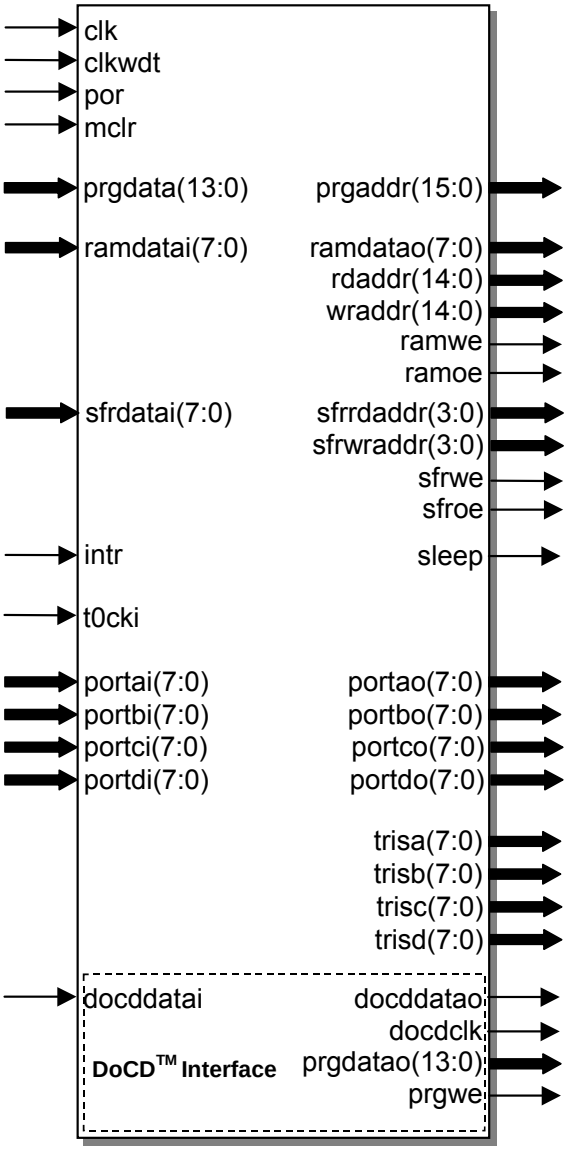
In all cases number of IP Core instantiations within a design, and number of manufactured chips are unlimited. There is no time restriction except *One Year* license where time of use is limited to 12 months.

- Single Design license for
  - *VHDL, Verilog source code called HDL Source*
  - *Encrypted, or plain text EDIF called Netlist*
- One Year license for
  - *Encrypted Netlist only*
- Unlimited Designs license for
  - *HDL Source*
  - *Netlist*
- Upgrade from
  - *HDL Source to Netlist*
  - *Single Design to Unlimited Designs*

PINS DESCRIPTION

PIN	TYPE	DESCRIPTION
clk	input	Global clock
clkwdt	input	Watchdog clock
por	input	Global reset Power On Reset
mclr	input	User reset
prgdata[13:0]	input	Data bus from program memory
ramdatai[7:0]	input	Data bus from int. data memory
sfrdatai[7:0]	input	Data bus from External SFR regs.
intr	input	External interrupt
t0cki	input	Timer 0 input
portxi[7:0]	input	Port A, B, C, D input
docddatai	input	DoCD™ Debugger input
prgaddr[15:0]	output	Program memory address bus
ramdatao[7:0]	output	Data bus for internal data memory
rdaddr[14:0]	output	RAM read address bus
wraddr[14:0]	output	RAM write address bus
ramwe	output	Data memory write
ramoe	output	Data memory output enable
sfrwraddr[3:0]	output	External SFR's write address bus
sfrrdaddr[14:0]	output	External SFR's read address bus
sfrwe	output	External SFR's write enable
sfroe	output	External SFR's output enable
sleep	output	Sleep signal
portxo[7:0]	output	Port A, B, C, D outputs
trisx[7:0]	output	Ports A, B, C, D data direction pins
docddatao	output	DoCD™ Debugger data output
docdclk	output	DoCD™ Clock line
prgdatao[13:0]	output	Program Memory data output
prgwe	output	Program Memory write enable

SYMBOL



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BLOCK DIAGRAM

ALU – Arithmetic Logic Unit performs arithmetic and logic operations during execution of an instruction. This module contains work register (W) and Status register.

Control Unit – It performs the core synchronization and data flow control. This module manages execution of all instructions. Performs decode and control functions for all other blocks. It contains program counter (PC) and hardware stack.

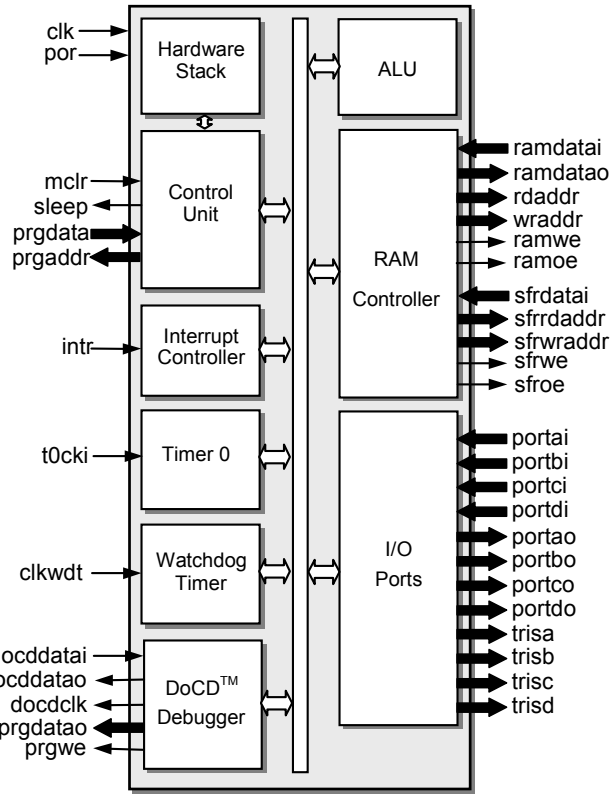
Hardware Stack – it's a configurable hardware stack. The stack space is not a part of either program or data space and the stack pointer is not readable or writable. The PC is pushed onto the stack when CALL instruction is executed or an interrupt causes a branch. The stack is popped while RETURN, RETFIE and RETLW instruction execution. The stack operates as a circular buffer. This means that after the stack has been pushed eight times, the ninth push overwrites the value that was stored from the first push.

RAM Controller – It performs interface functions between Data memory and DRPIC1655X internal logic. It assures correct Data Memory addressing and data transfers. The DRPIC1655X supports two addressing modes: direct or indirect. In Direct Addressing the 9-bit direct address is computed from RP(1:0) bits (STATUS) and 7 least significant bits of instruction word.
Indirect addressing is possible by using the INDF register. Any instruction using INDF register actually accesses data pointed to by the file select register FSR. Reading INDF register indirectly will produce 00h. Writing to the INDF register indirectly results in a no-operation. An effective 9-bit address is obtained by concatenating the IRP bit (STATUS) and the 8-bit FSR register.

Interrupt Controller – Interrupt Controller module is responsible for interrupt manage system for the external and internal interrupt sources. It contains interrupt related register called INTCON. There are three interrupt sources:

- External interrupt INT
- TMR0 overflow interrupt
- PORTB change interrupt (pins B7:B4)

The interrupt control register INTCON records individual interrupt requests in flag bits.
A global interrupt enable bit, GIE enables all unmasked interrupts. Each interrupt source has an individual enable bit, which can enable or disable corresponding interrupt.
When an interrupt is responded to, the GIE is cleared to disable any further interrupt, the return address is pushed into the stack and the PC is loaded with 0004h. The interrupt flag bits must be cleared in software before re-enabling interrupts.



Timer 0 – Main system's timer and prescaler. This timer operates in two modes: 8-bit timer or 8-bit counter. In the "timer mode", timer registers are incremented every 4 CLK periods. When the prescaler is assigned into the TIMER prescale ration can be divided by 2, 4 .. 256. In the "counter mode" the timer register is incremented every falling or rising edge of T0CKI pin, dependent on T0SE bit in OPTION register.

Watchdog Timer– it's a free running timer. WDT has own clock input separate from system clock. It means that the WDT will run even if the system clock is stopped by execution of SLEEP instruction. During normal operation, a WDT time-out generates a Watchdog reset. If the device is in SLEEP mode the WDT time-out causes the device to wake-up and continue with normal operation.

I/O Ports – Block contains DRPIC1655X's general purpose I/O ports and data direction registers (TRIS). The DRPIC1655X has four 8-bit full bi-directional ports PORT A, PORT B, PORT C, PORT D. Each port's bit can be individually accessed by bit addressable instructions. Read and write accesses to the I/O port are performed via their corresponding SFR's PORTA, PORTB, PORTC, PORTD. The reading instruction always reads the status of Port pins. Writing instructions always write into the Port latches. Each port's pin has an corresponding bit in TRISA, B, C and D registers. When the bit of TRIS register is set this means that the corresponding bit of port is configured as an input (output drivers are set into the High Impedance).

DoCD™ Debug Unit – it's a real-time hardware debugger provides debugging capability of a whole SoC system. In contrast to other on-chip debuggers DoCD™ provides non-intrusive debugging of running application. It can halt, run, step into or skip an instruction, read/write any contents of microcontroller including all registers, internal, external, program memories, all SFRs including user defined peripherals. Hardware breakpoints can be set and controlled on program memory, internal and external data memories, as well as on SFRs. Hardware breakpoint is executed if any write/read occurred at particular address with certain data pattern or without pattern. The DoCD™ system includes three-wire interface and complete set of tools to communicate and work with core in real time debugging. It is built as scalable unit and some features can be turned off to save silicon and reduce power consumption. A special care on power consumption has been taken, and when debugger is not used it is automatically switched in power save mode. Finally whole debugger is turned off when debug option is no longer used.

OPTIONAL PERIPHERALS

There are also available an optional peripherals, not included in presented DRPIC1655X Microcontroller Core. The optional peripherals, can be implemented in microcontroller core upon customer request.

- Timer 1 and Timer 2
- Full duplex UART
- SPI – Master and Slave Serial Peripheral Interface
  - *Supports speeds up ¼ of system clock*
    - *Mode fault error*
    - *Write collision error*
  - *Software selectable polarity and phase of serial clock SCK*
  - *System errors detection*
  - *Allows operation from a wide range of system clock frequencies (build-in 5-bit timer)*
  - *Interrupt generation*
- PWM – Pulse Width Modulation Timer
  - *2 independent 8-bit PWM channels, concatenated on one 16-bit PWM channel*
  - *Software-selectable duty from 0% to 100% and pulse period*
  - *Software-selectable polarity of output waveform*
- I2C bus controller - Master
  - *7-bit and 10-bit addressing modes*
  - *NORMAL, FAST, HIGH speeds*
  - *Multi-master systems supported*
  - *Clock arbitration and synchronization*
  - *User defined timings on I2C lines*
  - *Wide range of system clock frequencies*
  - *Interrupt generation*
- I2C bus controller - Slave
  - *NORMAL speed 100 kbs*
  - *FAST speed 400 kbs*
  - *HIGH speed 3400 kbs*
  - *Wide range of system clock frequencies*
  - *User defined data setup time on I2C lines*
  - *Interrupt generation*

PERFORMANCE

The following table gives a survey about the Core area and performance in the ALTERA® devices after Place & Route:

Device	Speed grade	Logic Cells	F_{max}
CYCLONE	-6	921	111 MHz
CYCLONE	-6	923	107 MHz
STRATIX	-5	922	114 MHz
STRATIX II	-3	823	189 MHz
STRATIX GX	-5	922	116 MHz
APEX II	-5	1131	94 MHz
APEX20KC	-7	1131	81 MHz
APEX20KE	-1	1131	70 MHz
APEX20K	-1	1131	41 MHz
ACEX1K	-1	1150	64 MHz
FLEX10KE	-1	1150	59 MHz

Core performance in ALTERA® devices

Area utilized by the each unit of DRPIC1655X core in vendor specific technologies is summarized in table below.

Component	AREA	
	[LC]	[FFs]
CPU*	711	285
Timer 0	60	29
Watchdog Timer	55	38
I/O Ports	96	64
Total area	922	416

*CPU – consisted of ALU, Control Unit, Bus Controller, Hardware Stack, Extended interrupt controller, External INT pin Interrupt Controller, Extended Interrupt controller, 512 B of RAM 8kW of program memory

Core components area utilization - CYCLONE

IMPROVEMENT

Most instruction of DRPIC1655X is executed within 1 CLK period, except program branches that require 2 CLK periods. The table below shows sample instructions execution times:

Mnemonic operands	DRPIC1655X (CLK cycles)	PIC16C554 (CLK cycles)	Impr.
ADDWF	1	4	4
ANDWF	1	4	4
RLF	1	4	4
BCF	1	4	4
DECFSZ	1(2)[1]	4(8)[1]	4
INCFSZ	1(2)[1]	4(8)[1]	4
BTFSC	1(2)[1]	4(8)[1]	4
BTFSS	1(2)[1]	4(8)[1]	4
CALL	2	8	4
GOTO	2	8	4
RETFIE	2	8	4
RETLW	2	8	4
RETURN	2	8	4

[1] number of clock in case when result of operation is 0.

DFPIC&DRPIC FAMILY OVERVIEW

The family of DCD DFPICXX & DRPICXX IP Cores combine a high–performance, low cost, and small compact size, offering the best price/performance ratio in the IP Market. The DCD's Cores are dedicated for use in cost-sensitive consumer products, computer peripherals, office automation, automotive control systems, security and telecommunication applications.

DCD's DFPICXX & DRPICXX IP Cores family contains four 8-bit microcontroller Cores to best meet your needs: DFPIC165X 12-bit program word, DFPIC1655X 14-bit program word, and DRPIC1655X and DRPIC166X single cycle microcontrollers with 14-bit program word. All three microcontroller cores are binary compatible with widely accepted PIC16C5X and PIC16CXXX. They employ a modified RISC architecture two or four times faster than the original ones.

The DFPICXXX & DRPICXX IP Cores are written in pure VHDL/VERILOG HDL languages which make them technologically independent. All of the DFPICXX & DRPICXX family members supports a power saving SLEEP mode and allows the user to configure the watchdog time-out period and a number of hardware stack levels. DFPICXX & DRPICXX can be fully customized according to customer needs.

Design	Program Memory space	Data Memory space	Program word length	Number of instructions	I/O Ports	Timer 0	Timer 1	Timer 2	Watchdog Timer	CCP1	USART	Sleep Mode	External interrupts	Internal Interrupts	Levels of hardware stack	Wake up on port pin change	Speed rate	DoCD™ Debugger	Size (gate)
DFPIC 165X	2k	128	12	33	24	✓	-	-	✓	-	-	✓	-	-	2	-	2	-	2 700
DFPIC 1655X	64k	512	14	35	16	✓	-	-	✓	-	-	✓	5	1	8	✓	2	✓*	3 900
DRPIC 1655X	64k	512	14	35	32	✓	-	-	✓	-	-	✓	5	1	8	✓	4	✓*	4 800
DRPIC 166X	64k	512	14	35	32	✓	✓	✓	✓	✓	✓	✓	5	5	8	✓	4	✓*	6 700

** Optional*

DFPIC & DRPIC family of High Performance Microcontroller Cores

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