TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

# TLCS-900/L Series

## TMP93PW20A

TOSHIBA CORPORATION

Semiconductor Company

# Preface

Thank you very much for making use of Toshiba microcomputer LSIs. Before use this LSI, refer the section, “Points of Note and Restrictions”.

Especially, take care below cautions.

**CAUTION**

**How to release the HALT mode**

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{\text{NMI}}$, INT0 to INT4, INTKEY and INTRTC), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of $f_{FPH}$) with IDLE1 or STOP mode (RUN and IDLE2 are not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

Low Voltage/Low Power

CMOS 16-Bit Microcontroller

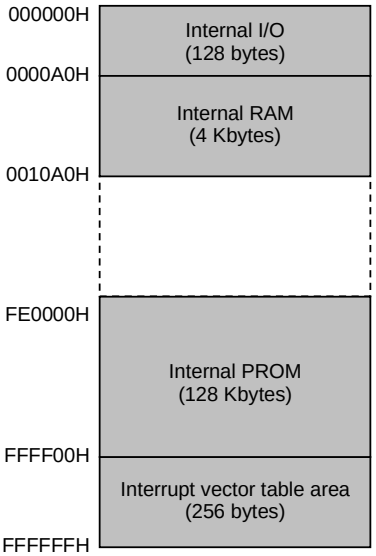
# TMP93PW20AF

## 1. Outline and Device Characteristics

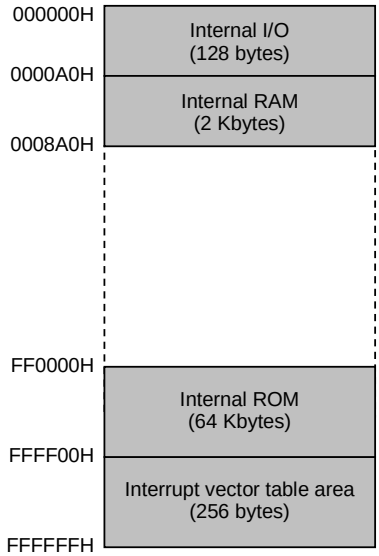
The TMP93PW20A is OTP type MCU which includes 128 Kbytes one-time PROM. Using the adapter-socket, you can write and verify the data for the TMP93CS20 by general EPROM programmer.

The TMP93PW20A has the same pin-assignment as the TMP93CS20 (Mask ROM type). Writing the program to built-in PROM, the TMP93PW20A operates as the same way as the TMP93CS20.

There are differences in the memory mapping area and the memory capacity of the internal PROM and RAM between the TMP93PW20A and the TMP93CS20. The internal PROM of the TMP93PW20A is 128 Kbytes, and the internal RAM is 4 Kbytes. The internal ROM of the TMP93CS20 is 64 Kbytes, and the internal RAM is 2 Kbytes. Memory maps are described as follows.

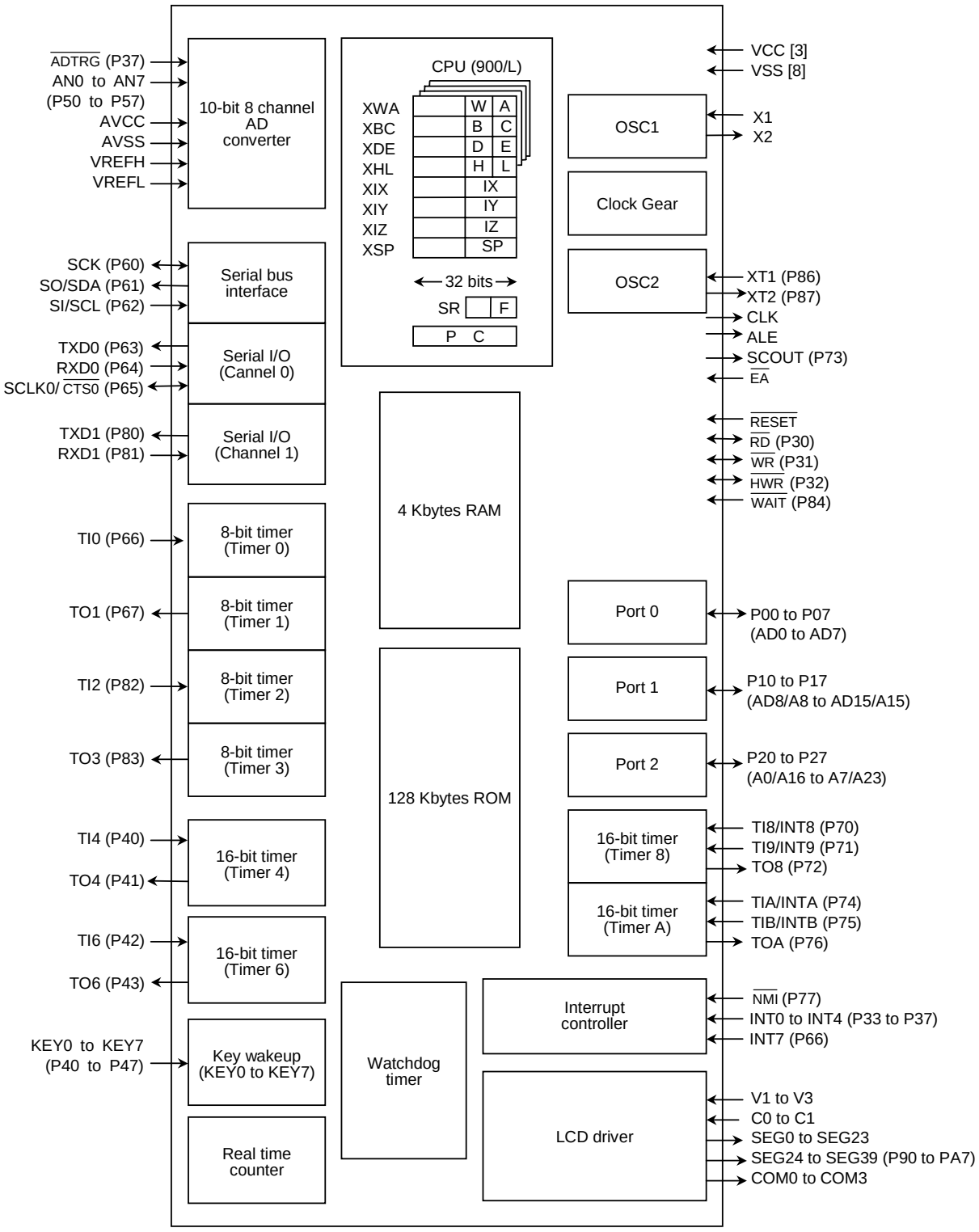



Memory map of TMP93PW20A




Memory map of TMP93CS20

| Product No. | ROM | RAM | Package | Adapter Socket |
|---|---|---|---|---|
| TMP93PW20A | OTP 128 Kbytes | 4 Kbytes | P-LQFP144-1616-0.40 | BM11141 |




Note: The item in parentheses ( ) are the initial setting after reset.

Figure 1.1 TMP93PW20A Block Diagram

# 2. Pin Assignment and Functions

The assignment of input/output pins for the TMP93PW20A their names and outline functions are described below.

## 2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93PW20AF.

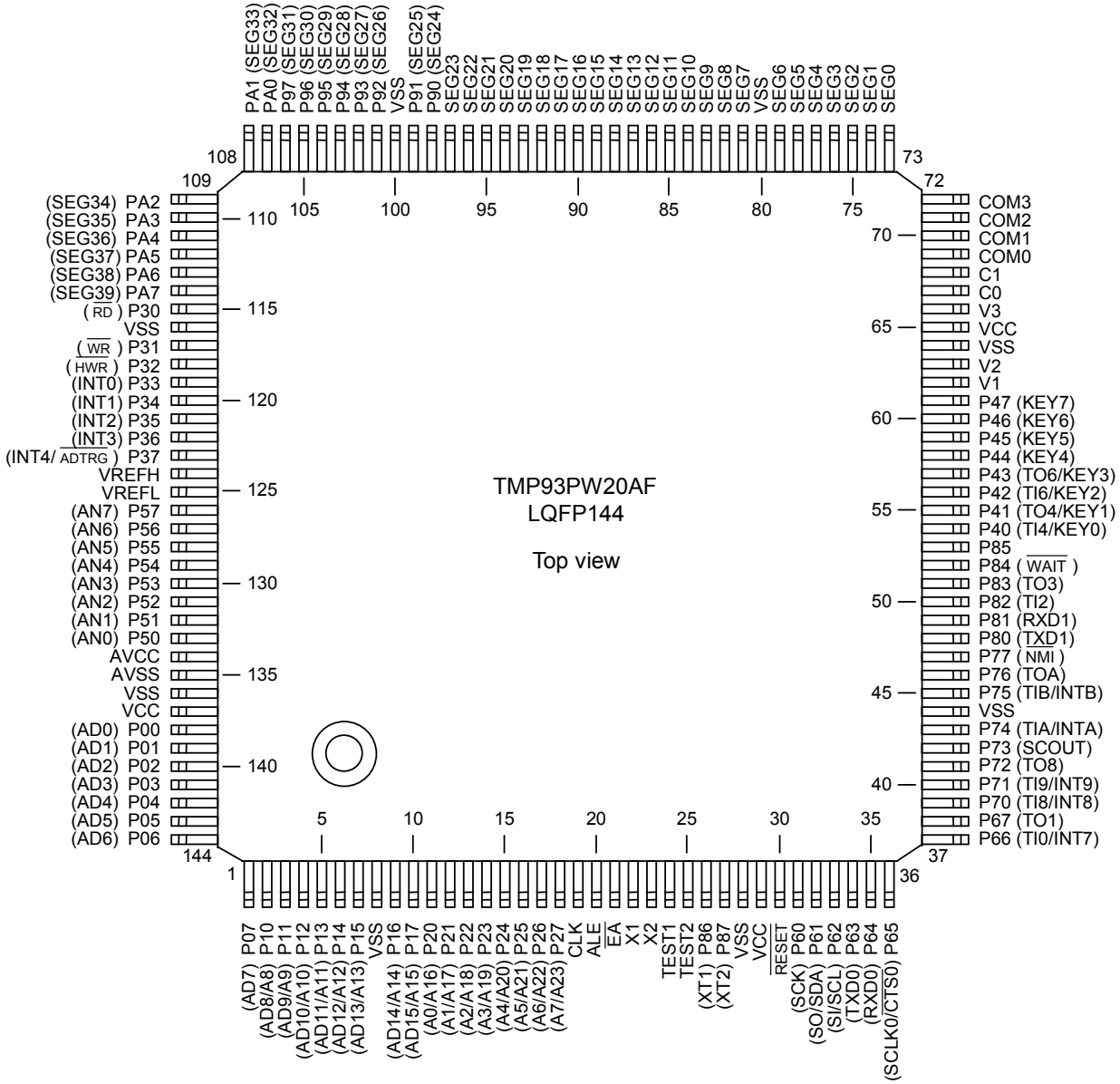



Figure 2.1.1 Pin Assignment (144-pin LQFP)

## 2.2 Pin Names and Functions

The TMP93PW20A has MCU mode and PROM mode.

(1) Pin functions of TMP93PW20A in MCU mode.

Table 2.2.1 Name and Function in MCU Mode (1/3)

| Pin Names | Number of Pins | I/O | Functions |
|---|---|---|---|
| P00 to P07<br>AD0 to AD7 | 8 | I/O<br>I/O | Port 0: I/O port that allows I/O to be selected at the bit level.<br>Address and data (lower): Bits 0 to 7 for address and data bus. |
| P10 to P17<br>AD8 to AD15<br>A8 to A15 | 8 | I/O<br>I/O<br>Output | Port 1: I/O port that allows I/O to be selected at the bit level.<br>Address and data (Upper): Bits 8 to 15 for address and data bus.<br>Address: Bits 8 to 15 for address bus. |
| P20 to P27<br>A0 to A7<br>A16 to A23 | 8 | I/O<br>Output<br>Output | Port 2: I/O port that allows I/O to be selected at the bit level (with pull-up resistor).<br>Address: Bits 0 to 7 for address bus.<br>Address: Bits 16 to 23 for address bus. |
| P30<br>$\overline{RD}$ | 1 | Output<br>Output | Port 30: Output port.<br>Read: Strobe signal for reading external memory.<br>(Read when reading internal memory at P3<P30> = 0, P3FC<P30F> = 1.) |
| P31<br>$\overline{WR}$ | 1 | Output<br>Output | Port 31: Output port.<br>Write: Strobe signal for writing data on pins AD0 to AD7. |
| P32<br>$\overline{HWR}$ | 1 | I/O<br>Output | Port 32: I/O port (with pull-up resistor).<br>High write: Strobe signal for writing data on pins AD8 to AD15. |
| P33<br>INT0 | 1 | I/O<br>Input | Port 33: I/O port (with pull-up resistor).<br>Interrupt request pin 0: Interrupt request pin with programmable level/rising/falling edge. |
| P34<br>INT1 | 1 | I/O<br>Input | Port 34: I/O port (with pull-up resistor).<br>Interrupt request pin 1: Interrupt request pin with programmable rising/falling edge. |
| P35<br>INT2 | 1 | I/O<br>Input | Port 35: I/O port (with pull-up resistor).<br>Interrupt request pin 2: Interrupt request pin with programmable rising/falling edge. |
| P36<br>INT3 | 1 | I/O<br>Input | Port 36: I/O port (with pull-up resistor).<br>Interrupt request pin 3: Interrupt request pin with programmable rising/falling edge. |
| P37<br>INT4<br><br>$\overline{ADTRG}$ | 1 | I/O<br>Input<br><br>Input | Port 37: I/O port (with pull-up resistor).<br>Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge.<br>ADTRG Input AD external trigger pin: External trigger pin to start AD conversion. |
| P40<br>TI4<br>KEY0 | 1 | I/O<br>Input<br>Input | Port 40: I/O port (with pull-up resistor).<br>Timer input 4: 16-bit timer 4 input.<br>Key input 0: Key-on wakeup pin 0. |
| P41<br>TO4<br>KEY1 | 1 | I/O<br>Output<br>Input | Port 41: I/O port (with pull-up resistor).<br>Timer output 4: 16-bit timer 4 output.<br>Key input 1: Key-on wakeup pin 1. |
| P42<br>TI6<br>KEY2 | 1 | I/O<br>Input<br>Input | Port 42: I/O port (with pull-up resistor).<br>Timer input 6: 16-bit timer 6 input.<br>Key input 2: Key-on wakeup pin 2. |
| P43<br>TO6<br>KEY3 | 1 | I/O<br>Output<br>Input | Port 43: I/O port (with pull-up resistor).<br>Timer output 6: 16-bit timer 6 output.<br>Key input 3: Key-on wakeup pin 3. |
| P44 to P47<br>KEY4 to KEY7 | 4 | I/O<br>Input | Port 44 to 47: I/O port (with pull-up resistor).<br>Key input 4 to 7: Key-on wakeup pin 4 to 7. |
| P50 to P57<br>AN0 to AN7 | 8 | Input<br>Input | Port 50 to 57: Pin used to input port.<br>Analog input 0 to 7. |

Table 2.2.1 Name and Function in MCU Mode (2/3)

| Pin Names | Number of Pins | I/O | Functions |
|---|---|---|---|
| P60<br>SCK | 1 | I/O<br>I/O | Port 60: I/O port.<br>Clock I/O pin in SIO mode of the serial bus interface. |
| P61<br>SO<br>SDA | 1 | I/O<br>Output<br>I/O | Port 61: I/O port (with programmable open drain).<br>Data send channel in SIO mode of the serial bus interface.<br>Data I/O pin in $I^2C$ bus mode of the serial bus interface. |
| P62<br>SI<br>SCL | 1 | I/O<br>Input<br>I/O | Port 62: I/O port (with programmable open drain).<br>Data receive channel in SIO mode of the serial bus interface.<br>Clock I/O pin in $I^2C$ bus mode of the serial bus interface. |
| P63<br>TXD0 | 1 | I/O<br>Output | Port 63: I/O port (with programmable open drain).<br>Serial send data 0. |
| P64<br>RXD0 | 1 | I/O<br>Input | Port 64: I/O port.<br>Serial receive data 0. |
| P65<br>SCLK0<br>$\overline{\text{CTS0}}$ | 1 | I/O<br>I/O<br>Input | Port 65: I/O port.<br>Serial clock I/O 0.<br>Serial data send enable 0 (Clear to send). |
| P66<br>TI0<br>INT7 | 1 | I/O<br>Input<br>Input | Port 66: I/O port.<br>Timer input 0: 8-bit timer 0 input.<br>Interrupt request pin 7: Interrupt request pin with programmable rising/falling edge. |
| P67<br>TO1 | 1 | I/O<br>Output | Port 67: I/O port.<br>Timer output1: 8-bit timer 0 or timer 1 output. |
| P70<br>TI8<br>INT8 | 1 | I/O<br>Input<br>Input | Port 70: I/O port (with pull-up resistor).<br>Timer input 8: 16-bit timer 8 input.<br>Interrupt request pin 8: Interrupt request pin with programmable rising/falling edge. |
| P71<br>TI9<br>INT9 | 1 | I/O<br>Input<br>Input | Port 71: I/O port (with pull-up resistor).<br>Timer input 9: 16-bit timer 8 input.<br>Interrupt request pin 9: Interrupt request pin with rising edge. |
| P72<br>TO8 | 1 | I/O<br>Output | Port 72: I/O port (with pull-up resistor).<br>Timer output 8: 16-bit timer 8 output. |
| P73<br>SCOUT | 1 | I/O<br>Output | Port 73: I/O port (with pull-up resistor).<br>System clock output: System clock or double system clock output to be synchronized with the external circuit. |
| P74<br>TIA<br>INTA | 1 | I/O<br>Input<br>Input | Port 74: I/O port (with pull-up resistor).<br>Timer input A: 16-bit timer A input.<br>Interrupt request pin A: Interrupt request pin with programmable rising/falling edge. |
| P75<br>TIB<br>INTB | 1 | I/O<br>Input<br>Input | Port 75: I/O port (with pull-up resistor).<br>Timer input B: 16-bit timer B input.<br>Interrupt request pin B: Interrupt request pin with rising edge. |
| P76<br>TOA | 1 | I/O<br>Output | Port 76: I/O port (with pull-up resistor).<br>Timer output A: 16-bit timer A output. |
| P77<br>$\overline{\text{NMI}}$ | 1 | I/O<br>Input | Port 77: I/O port (with pull-up resistor).<br>Non-maskable interrupt request pin: Interrupt request pin with programmable falling edge or both edges. |
| P80<br>TXD1 | 1 | I/O<br>Output | Port 80: I/O port (with programmable open drain).<br>Serial send data 1. |
| P81<br>RXD1 | 1 | I/O<br>Input | Port 81: I/O port (with programmable open drain).<br>Serial receive data 1. |
| P82<br>TI2 | 1 | I/O<br>Input | Port 82: I/O port (with programmable open drain).<br>Timer input 2: 8-bit timer 2 input pin. |
| P83<br>TO3 | 1 | I/O<br>Output | Port 83: I/O port (with programmable open drain).<br>Timer output 3: 8-bit timer 2, 3 output pin. |
| P84<br>$\overline{\text{WAIT}}$ | 1 | I/O<br>Input | Port 84: I/O port (with programmable open drain).<br>Wait: Pin used to request CPU bus wait. |

Table 2.2.1 Name and Function in MCU Mode (3/3)

| Pin Names | Number of Pins | I/O | Functions |
|---|---|---|---|
| P85 | 1 | I/O | Port 85: I/O port (with programmable open drain). |
| P86<br>XT1 | 1 | I/O<br>Input | Port 86: I/O port (Open drain).<br>Low-frequency oscillator connecting pin. |
| P87<br>XT2 | 1 | I/O<br>Output | Port 87: I/O port (Open drain).<br>Low-frequency oscillator connecting pin. |
| P90 to P97<br>SEG24 to SEG31 | 8 | Output<br>Output | Port 90 to port 97: Output port (Open drain).<br>Segment data output pin. |
| PA0 to PA7<br>SEG32 to SEG39 | 8 | Output<br>Output | Port A0 to A7: Output port, large current port (Open drain).<br>LCD segment output pin. |
| SEG0 to SEG23 | 24 | Output | LCD segment output. |
| COM0 to COM3 | 4 | Output | LCD common output. |
| AVCC | 1 | Power supply | Power supply pin for AD converter. |
| AVSS | 1 | Power supply | GND pin for AD converter (0 V). |
| VREFH | 1 | Input | Pin for reference voltage input to AD converter (H). |
| VREFL | 1 | Input | Pin for reference voltage input to AD converter (L). |
| X1 | 1 | Input | Oscillator connecting pin. |
| X2 | 1 | Output | Oscillator connecting pin. |
| $\overline{\text{RESET}}$ | 1 | Input | Reset: Initializes LSI. |
| ALE | 1 | Output | Address latch enable.<br>Can be disabled for reducing noise. |
| CLK | 1 | Output | Clock output: Outputs “external input clock × 1 ÷ 4” clock.<br>Pulled-up during reset.<br>Can be disabled for reducing noise. |
| $\overline{\text{EA}}$ | 1 | Input | The VCC pin should be connected. |
| VCC | 3 | Power supply | Power supply pin (All Vcc pins should be connected with the power supply pin). |
| VSS | 8 | Power supply | GND pin (0 V) (All Vss pins should be connected with GND (0 V)). |
| TEST1<br>TEST2 | 2 | Output<br>Input | TEST1 should be connected with TEST2 pin.<br>Do not connect to any other pins. |
| C0, C1,<br>V1 to V3 | 5 | LCD pin | LCD drive boosting pin.<br>A condenser should be connected between C0 and C1, V1, V2, V3 and GND. |

Note: All pins that have built-in pull-up resistors can be disconnected from the built-in pull-up resistor by software.

(2) Pin function of the TMP93PW20A in PROM mode

Pin names and functions are shown in Table 2.2.2.

Table 2.2.2 Pin Names and Function in PROM Mode

| Pin Names | Number of Pins | Input/Output | Functions | Pin Names (in MCU mode) |
|---|---|---|---|---|
| A7 to A0 | 8 | Input | Memory address of program | P27 to P20 |
| A15 to A8 | 8 | Input | | P17 to P10 |
| A16 | 1 | Input | | P67 |
| D7 to D0 | 8 | I/O | Memory data of program | P07 to P00 |
| $\overline{CE}$ | 1 | Input | Chip enable | P32 |
| $\overline{OE}$ | 1 | Input | Output control | P30 |
| $\overline{PGM}$ | 1 | Input | Program control | P31 |
| VPP | 1 | Power supply | 12.75 V/5 V (Power supply of program) | $\overline{EA}$ |
| VCC | 4 | Power supply | 6.25 V/5 V | VCC, AVCC |
| VSS | 9 | Power supply | 0 V | VSS, AVSS |

| Pin Names | Number of Pins | Input/Output | Pin State |
|---|---|---|---|
| P60 | 1 | Input | Fix to low level (Security pin) |
| $\overline{RESET}$ | 1 | Input | Fix to low level (PROM mode) |
| CLK | 1 | Input | |
| ALE | 1 | Output | Open |
| X1 | 1 | Input | Self oscillation with resonator |
| X2 | 1 | Output | |
| P66 to P61 | 6 | Input | Fix to high level |
| TEST1<br>TEST2 | 2 | Output<br>Input | TEST1 should be connected with TEST2 pin<br>Do not connect to any other pins |
| P37 to P33<br>P47 to P40<br>P57 to P50<br>P77 to P70<br>P87 to P80<br>P97 to P90<br>PA7 to PA0<br>SEG23 to SEG0<br>VREFH<br>VREFL<br>C0, C1<br>COM3 to COM0<br>V3 to V1 | 88 | I/O | Open |

# 3. Operation

This section describes the functions and basic operational blocks of the TMP93PW20A.

The TMP93PW20A has PROM in place of the mask ROM which is included in the TMP93CS20. The other configuration and functions are the same as the TMP93CS20. Regarding the function of the TMP93PW20A, which is not described herein, see the TMP93CS20.

The TMP93PW20A has two operational modes: MCU mode and PROM mode.

## 3.1 MCU mode

(1) Mode setting and function

The MCU mode is set by releasing the CLK pin (Pin open).

In the MCU mode, the operation is the same as TMP93CS20.

(2) Memory map

The memory map of TMP93PW20A differs from that of TMP93CS20.

The memory map in MCU mode is show in Figure 3.1.1, and the memory map in PROM mode is shown in Figure 3.1.2.

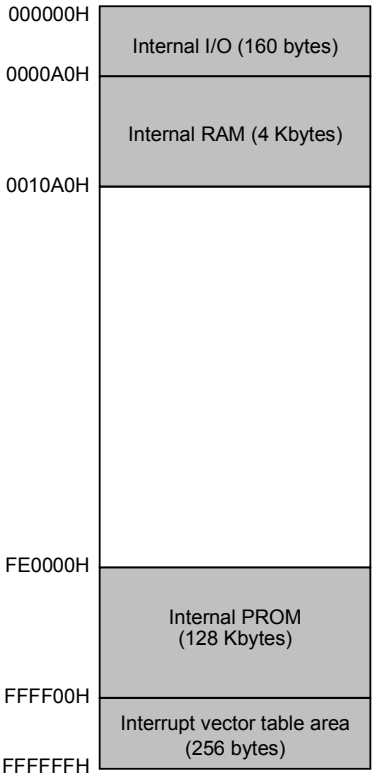



Figure 3.1.1 Memory Map in MCU Mode

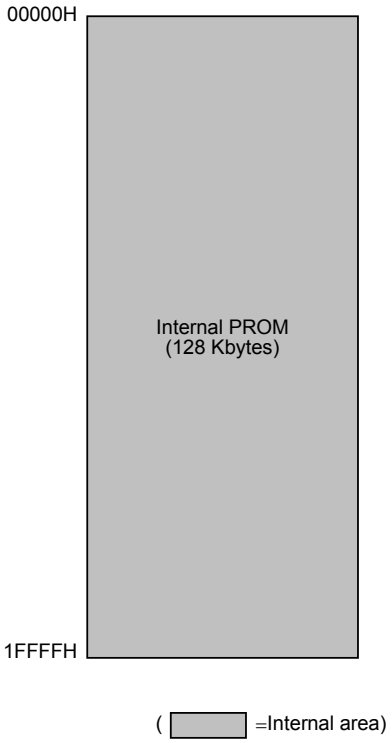



Figure 3.1.2 Memory Map in PROM Mode

(3) Note on setting of the wait controller

The TMP93PW20A has a wide memory area compared as the TMP93CS20. For the addressing area of WAITC1, there is a difference between the TMP93PW20A and the TMP93CS20.

When bits 1 and 0 < B1C1:0> in the chip select and wait control register 1 (WAITC1) is set to 00, the address area is specified as follows.

| TMP93PW20A | TMP93CS20 |
|---|---|
| 10A0H to 7FFFH | 8A0H to 7FFFH |

## 3.2 PROM Mode

(1) Mode setting and programming

PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the "Low" level.

The programming and verification for the internal PROM is achieved by using a general PROM programmer with the adaptor socket.

1. OTP adaptor

   BM11141: TMP93PW20AF adaptor

2. Setting OTP adaptor

   Set the switch (SW1) to N side.

3. Setting PROM programmer

   i) Set PROM type to TC571000D.

   Size: 1 Mbits (128 K × 8 bits)

   VPP: 12.75 V

   $t_{PW}$: 100 μs

   Electric signature function: None

   ii) Transferring the data (Copy)

   In TMP93PW20AF, PROM is placed on addresses 00000H to 1FFFFH in PROM mode, and addresses FE0000H to FFFFFFH in MCU mode.

   Therefore data should be transferred to addresses 00000H to 1FFFFH in PROM mode using the object converter (tuconv) or the block transfer mode. (See instruction manual of PROM programmer.)

   iii) Setting program address

   Start address: 00000H

   End address: 1FFFFH

4. Programming

   Program/verify according to the procedures of PROM programmer.

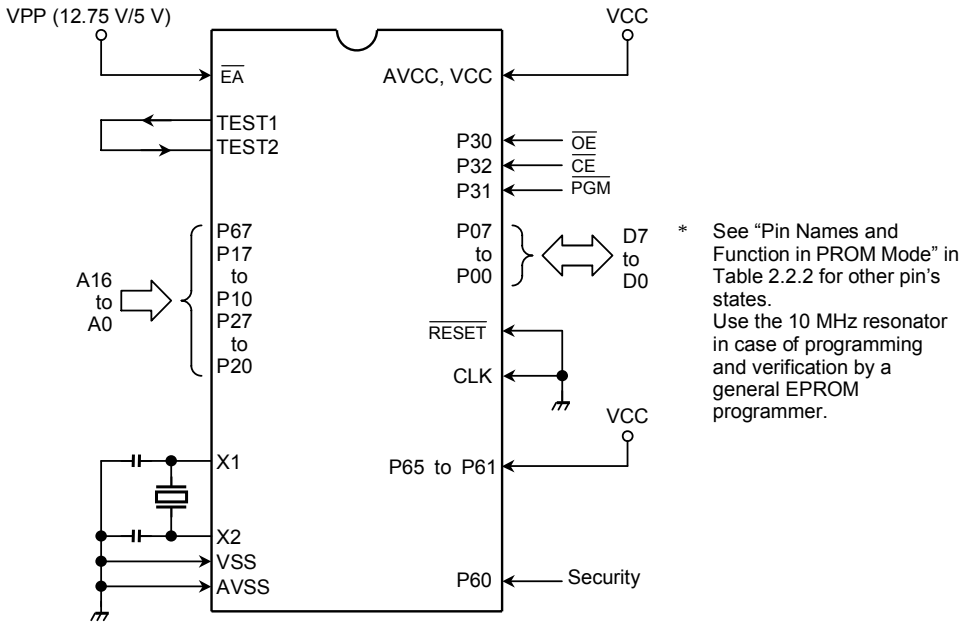



Figure 3.2.1 Pin Setting in PROM Mode

(2) Note on electric signature

The electric signature mode (Hereinafter referred to as "signature") is not supported in the TMP93PW20A. Therefore using signature with PROM programmer applies voltage of 12 ± 0.5 V to pin 9 (A9) of the address, and the device is damaged. Do not use signature.

(3) Program mode

The TMP93PW20A is provided with all bits set to 1 (OFF). When programming it, write data 0 to necessary bit locations.

Applying $V_{PP}$ = 12.5 V, $\overline{OE}$ = $V_{IH}$ $\overline{CE}$ = $V_{IL}$ enables writing data.
The one-time PROM which is included in the TMP93PW20A can write data in any order. It is possible to write a special address.

(4) Adapter socket (BM11141)

The BM11141 is an adapter socket to write data to the one-time PROM in the TMP93PW20A using a general PROM programmer.

(5) Program storage area in PROM mode

The TMP93PW20A has a program area (FE0000H to FFFFFFH) of 128 Kbytes. In PROM mode, addresses 00000H to 1FFFFH correspond to addresses FE0000H to FFFFFFH in MCU mode.

(6) How to program with a general PROM programmer

The PROM programmer should be equivalent to TC571000D.

1. Set a switch (SW1) of BM11141 to a program side (NOR). (BM11141 is hereinafter referred as an adapter.) (Note 1)
2. Set a MCU to the adapter. (Note 2)
3. Set the adapter to the PROM programmer. (Note 2)
4. Specify TC571000D as a type of the PROM.
5. Set a start address to 00000H and an end address to 1FFFFH to write the PROM. (Note 3)
6. Write the one-time PROM and verify according to operational procedures of the PROM programmer.

Note 1: If you write a data to the one-time PROM without setting the switch (SW1) to the program side, a device should be damaged.

Note 2: 1 pin marked on the socket of the PROM programmer must be matched to the 1 pin of the adapter. If you set them in reverse, the MCU or the PROM programmer should be damaged.

Note 3: When data 0 is written to an address over 1FFFFH, there is a possibility that the data is written to addresses 00000H to 1FFFFH and an original program is corrupted.

(7) Programming flow chart

The programming mode is set by applying 12.75 V (programming voltage) to the $V_{PP}$ pin when the following pins are set as follows, (VCC: 6.25 V, $\overline{\text{RESET}}$: "Low" level, CLK: "Low" level).

While address and data are fixed and $\overline{\text{CE}}$ pin is set to "L" level, 0.1 ms of "Low" level pulse is applied to PGM pin to program the data.
Then the data in the address is verified.
If the programmed data is incorrect, another 0.1 ms pulse is applied to $\overline{\text{PGM}}$ pin.
This programming procedure is repeated until correct data is read from the address (25 times maximum).
Subsequently, all data are programmed in all addresses.
The verification for all data is done under the condition of $V_{PP} = V_{CC} = 5$ V after all data were written.

Figure 3.2.2 shows the programming flowchart.

High Speed Program Writing.

Flowchart

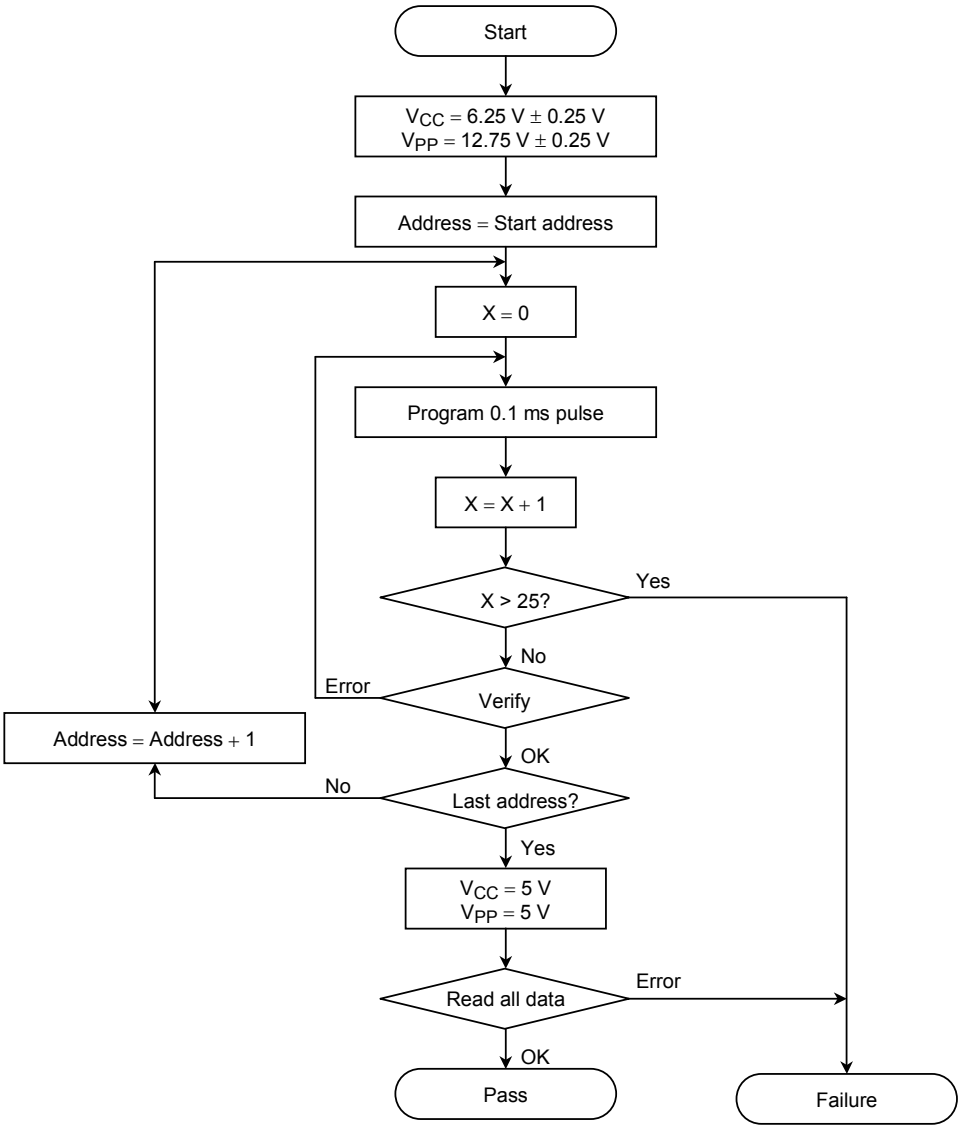



Figure 3.2.2 Flowchart

(8) Security bit

The TMP93PW20A has a security bit.
If the security bit is programmed to 0, the content of the PROM can not be read in PROM mode. (Outputs data FFH)

(How to program the security bit)

The difference from the programming procedures described in section 3.2 (1) are follows.

1. Setting OTP adapter

   Set the switch (SW1) to S side.

2. Setting PROM programmer

   i) Transferring the data

   ii) Setting programming address

   The security bit is in bit 0 of address 00000H.

   Set the start address 00000H and the end address 00000H.

   Set the data FEH at the address 00000H.

# 4. Electrical Characteristics

## 4.1 Maximum Rating (TMP93PW20A)

"X" used in an expression shows a frequency for the clock $f_{FPH}$ selected by SYSCR1<SYSCK>. The value of X changes according to whether a clock gear or a low speed oscillator is selected. An example value is calculated for fc, with gear = fc/1 (SYSCR1<SYSCK, GEAR2:0> = 0000).

| Parameter | Symbol | Rating | | Unit |
|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | −0.5 to 6.5 | | V |
| Input voltage | $V_{IN}$ | Except $\overline{EA}$ pin | −0.5 to $V_{CC}$ + 0.5 | |
| | | $\overline{EA}$ pin | −0.5 to 14.0 | |
| Output current (Per one pin), large current port | $I_{OL1}$ | 20 | | mA |
| Output current (Per one pin) | $I_{OL2}$ | 2 | | |
| Output current (Total of large current port) | $\Sigma I_{OL1}$ | 80 | | |
| Output current (Total) | $\Sigma I_{OL}$ | 120 | | |
| Output current (Total) | $\Sigma I_{OH}$ | −80 | | |
| Power dissipation (Ta = 85°C) | $P_D$ | 600 | | mW |
| Soldering temperature (10 s) | $T_{SOLDER}$ | 260 | | °C |
| Storage temperature | $T_{STG}$ | −65 to150 | | |
| Operating temperature | $T_{OPR}$ | −40 to 85 | | |

Note: The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no maximum rating value will ever be exceeded.

## 4.2 DC Characteristics (1/2)

Ta = −40 to 85°C

| Parameter | | Symbol | Condition | | Min | Typ. (Note) | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Power supply voltage ($AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS} = 0$ V) | | $V_{CC}$ | fc = 4 to 20 MHz | fs = 30 to 34 kHz | 4.5 | | 5.5 | V |
| | | | fc = 4 to 12.5 MHz | | 2.7 | | | |
| Input low voltage | AD0 to AD15 | $V_{IL}$ | $V_{CC} \geq 4.5$ V | | −0.3 | | 0.8 | V |
| | | $V_{IL1}$ | $V_{CC} < 4.5$ V | | | | 0.6 | |
| | Port | $V_{IL1}$ | $V_{CC}$ = 2.7 to 5.5 V | | | | 0.3 $V_{CC}$ | |
| | KEY0 to KEY7, NMI, INT0 to INT4 | $V_{IL2}$ | | | | | 0.25 $V_{CC}$ | |
| | $\overline{EA}$ | $V_{IL3}$ | | | | | 0.3 | |
| | X1 | $V_{IL4}$ | | | | | 0.2 $V_{CC}$ | |
| | $\overline{RESET}$ | $V_{IL5}$ | | | | | 0.1 $V_{CC}$ | |
| Input high voltage | AD0 to AD15 | $V_{IH}$ | $V_{CC} \geq 4.5$ V | | 2.2 | | $V_{CC}$ + 0.3 | |
| | | $V_{IH}$ | $V_{CC} \geq 4.5$ V | | 2.0 | | | |
| | Port | $V_{IH1}$ | $V_{CC}$ = 2.7 to 5.5 V | | 0.7 $V_{CC}$ | | | |
| | KEY0 to KEY7, $\overline{NMI}$, INT0 to INT4 | $V_{IH2}$ | | | 0.75 $V_{CC}$ | | | |
| | $\overline{EA}$ | $V_{IH3}$ | | | Vcc − 0.3 | | | |
| | X1 | $V_{IH4}$ | | | 0.8 $V_{CC}$ | | | |
| | $\overline{RESET}$ | $V_{IH5}$ | | | 0.6 $V_{CC}$ | | | |

Note: Typical values are for Ta = 25°C and $V_{CC}$ = 5 V unless otherwise noted.

## 4.2 DC Characteristics (2/2)

| Parameter | Symbol | Condition | Min | Typ. (Note 1) | Max | Unit |
|---|---|---|---|---|---|---|
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 1.6 mA ($V_{CC}$ = 2.7 to 5.5 V) | | | 0.45 | V |
| Output low current (PA0 to PA7) | $I_{OLA}$ | $V_{OL}$ = 1.0 V ($V_{CC}$ = 5 V ± 10%) | 16 | | | mA |
| | | ($V_{CC}$ = 3 V ± 10%) | 7 | | | |
| Output high voltage | $V_{OH1}$ | $I_{OH}$ = −400 μA ($V_{CC}$ = 3 V ± 10%) | 2.4 | | | V |
| | $V_{OH2}$ | $I_{OH}$ = −400 μA ($V_{CC}$ = 5 V ± 10%) | 4.2 | | | |
| Darlington drive current (8 output pins max) | $I_{DAR}$ (Note 2) | $V_{EXT}$ = 1.5 V, $R_{EXT}$ = 1.1 kΩ ($V_{CC}$ = 5 V ± 10% only) | −1.0 | | −3.5 | mA |
| Input leakage current | $I_{LI}$ | 0.0 ≤ $V_{IN}$ ≤ $V_{CC}$ | | 0.02 | ±5 | μA |
| Output leakage current | $I_{LO}$ | 0.2 ≤ $V_{IN}$ ≤ $V_{CC}$ − 0.2 | | 0.05 | ±10 | |
| Power down voltage (at stop, RAM backup) | $V_{STOP}$ | $V_{IL2}$ = 0.2 $V_{CC}$, $V_{IH2}$ = 0.8 $V_{CC}$ | 2.0 | | 6.0 | V |
| Pin capacitance | $C_{IO}$ | fc = 1 MHz | | | 10 | pF |
| Shumitt width KEYx, $\overline{NMI}$, INT0 to INT4, $\overline{RESET}$ | $V_{TH}$ | | 0.4 | 1.0 | | V |
| Programmable pull-up resistance | $R_{KH}$ | $V_{CC}$ = 5 V ± 10% | 50 | | 150 | kΩ |
| | | $V_{CC}$ = 3 V ± 10% | 100 | | 300 | |
| NORMAL | $I_{CC}$ | $V_{CC}$ = 5 V ± 10% fc = 20 MHz | | 32 | 40 | mA |
| RUN | | | | 24 | 30 | |
| IDLE2 | | | | 17 | 21 | |
| IDLE1 | | | | 4.5 | 7 | |
| NORMAL | | $V_{CC}$ = 3 V ± 10% fc = 12.5 MHz (Typ. $V_{CC}$ = 3.0 V) | | 14 | 20 | mA |
| RUN | | | | 10 | 14 | |
| IDLE2 | | | | 7 | 10 | |
| IDLE1 | | | | 2 | 3 | |
| SLOW | | Vcc = 3 V ± 10% fs = 32.768 kHz (Typ. $V_{CC}$ = 3.0 V) at boosting frequency = 1 kHz | | 40 | 55 | μA |
| RUN | | | | 30 | 42 | |
| IDLE2 | | | | 20 | 33 | |
| IDLE1 | | | | 10 | 24 | |
| STOP | | Ta ≤ 50°C | | 0.2 | 10 | μA |
| | | Ta ≤ 70°C | | | 20 | |
| | | Ta ≤ 85°C | | | 50 | |

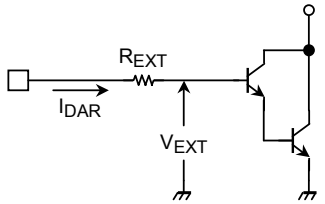
Note 1: Typical values are for Ta = 25°C and $V_{CC}$ = 5 V unless otherwise noted.

Note 2: $I_{DAR}$ is guaranteed for up to eight ports.

Note 3: Segment or common output is not loaded.

Note 4: $I_{CC}$ measurement conditions (NORMAL, SLOW): Only CPU is operational; output pins are open and input pins are fixed.

(e.g.) Diagram of $I_{DAR}$



## 4.3 AC Electrical Characteristics

(1) $V_{CC}$ = 5 V ± 10%

| No. | Parameter | Symbol | Variable | | 16 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| 1 | Osc. period (= x) | $t_{OSC}$ | 50 | 31250 | 62.5 | | 50 | | ns |
| 2 | CLK width | $t_{CLK}$ | 2x – 40 | | 85 | | 60 | | ns |
| 3 | A0 to A23 valid → CLK hold | $t_{AK}$ | 0.5x – 20 | | 11 | | 5 | | ns |
| 4 | CLK valid → A0 to A23 hold | $t_{KA}$ | 1.5x – 70 | | 24 | | 5 | | ns |
| 5 | A0 to A15 valid → ALE fall | $t_{AL}$ | 0.5x – 15 | | 16 | | 10 | | ns |
| 6 | ALE fall → A0 to A15 hold | $t_{LA}$ | 0.5x – 20 | | 11 | | 5 | | ns |
| 7 | ALE high width | $t_{LL}$ | x – 40 | | 23 | | 10 | | ns |
| 8 | ALE fall → $\overline{RD}$ / $\overline{WR}$ fall | $t_{LC}$ | 0.5x – 25 | | 6 | | 0 | | ns |
| 9 | $\overline{RD}$ / $\overline{WR}$ rise → ALE rise | $t_{CL}$ | 0.5x – 20 | | 11 | | 5 | | ns |
| 10 | A0 to A15 valid → $\overline{RD}$ / $\overline{WR}$ fall | $t_{ACL}$ | x – 25 | | 38 | | 25 | | ns |
| 11 | A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall | $t_{ACH}$ | 1.5x – 50 | | 44 | | 25 | | ns |
| 12 | $\overline{RD}$ / $\overline{WR}$ rise → A0 to A23 hold | $t_{CA}$ | 0.5x – 25 | | 6 | | 0 | | ns |
| 13 | A0 to A15 valid → D0 to D15 input | $t_{ADL}$ | | 3.0x – 55 | | 133 | | 95 | ns |
| 14 | A0 to A23 valid → D0 to D15 input | $t_{ADH}$ | | 3.5x – 65 | | 154 | | 110 | ns |
| 15 | $\overline{RD}$ fall → D0 to D15 input | $t_{RD}$ | | 2.0x – 60 | | 65 | | 40 | ns |
| 16 | $\overline{RD}$ low pulse width | $t_{RR}$ | 2.0x – 40 | | 85 | | 60 | | ns |
| 17 | $\overline{RD}$ rise → D0 to D15 hold | $t_{HR}$ | 0 | | 0 | | 0 | | ns |
| 18 | $\overline{RD}$ rise → A0 to A15 output | $t_{RAE}$ | x – 15 | | 48 | | 35 | | ns |
| 19 | $\overline{WR}$ low pulse width | $t_{WW}$ | 2.0x – 40 | | 85 | | 60 | | ns |
| 20 | D0 to D15 valid → $\overline{WR}$ rise | $t_{DW}$ | 2.0x – 55 | | 70 | | 45 | | ns |
| 21 | $\overline{WR}$ rise → D0 to D15 hold | $t_{WD}$ | 0.5x – 15 | | 16 | | 10 | | ns |
| 22 | A0 to A23 valid → $\overline{WAIT}$ input ((1 + N) WAIT mode) | $t_{AWH}$ | | 3.5x – 90 | | 129 | | 85 | ns |
| 23 | A0 to A15 valid → $\overline{WAIT}$ input ((1 + N) WAIT mode) | $t_{AWL}$ | | 3.0x – 80 | | 108 | | 70 | ns |
| 24 | $\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold ((1 + N) WAIT mode) | $t_{CW}$ | 2.0x + 0 | | 125 | | 100 | | ns |
| 25 | A0 to A23 valid → Port input | $t_{APH}$ | | 2.5x – 120 | | 36 | | 5 | ns |
| 26 | A0 to A23 valid → Port hold | $t_{APH2}$ | 2.5x + 50 | | 206 | | 175 | | ns |
| 27 | $\overline{WR}$ rise → Port valid | $t_{CP}$ | | 200 | | 200 | | 200 | ns |

AC measuring conditions

- Output level: High 2.2 V/Low 0.8 V, CL = 50 pF
  (However, CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, CLK)
- Input level: High 2.4 V/Low 0.45 V (AD0 to AD15)
  High 0.8 × $V_{CC}$/Low 0.2 × $V_{CC}$ (except AD0 to AD15)

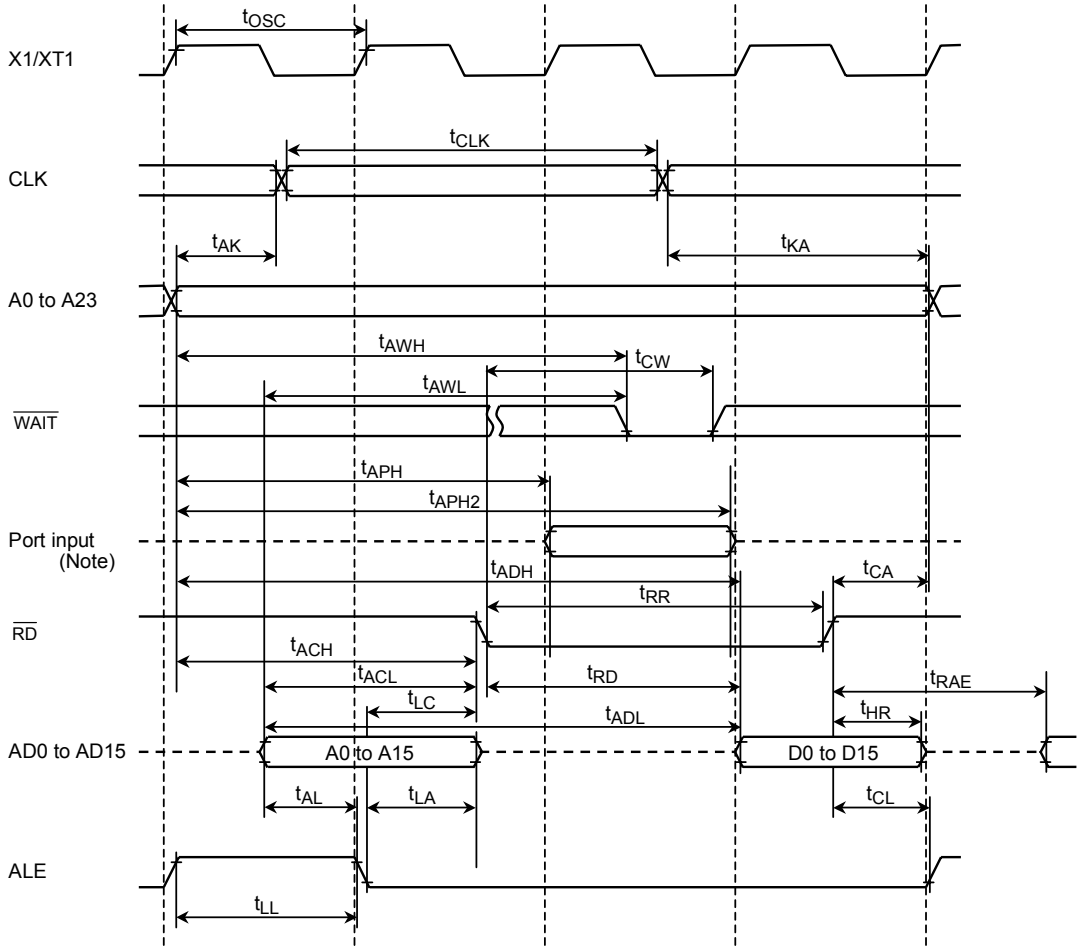
(2) $V_{CC}$ = 3 V ± 10%

| No. | Parameter | Symbol | Variable | | 12.5 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| 1 | Osc. period (= x) | $t_{OSC}$ | 80 | 31250 | 80 | | ns |
| 2 | CLK width | $t_{CLK}$ | 2x – 40 | | 120 | | ns |
| 3 | A0 to A23 valid → CLK hold | $t_{AK}$ | 0.5x – 30 | | 10 | | ns |
| 4 | CLK valid → A0 to A23 hold | $t_{KA}$ | 1.5x – 80 | | 40 | | ns |
| 5 | A0 to A15 valid → ALE fall | $t_{AL}$ | 0.5x – 35 | | 5 | | ns |
| 6 | ALE fall → A0 to A15 hold | $t_{LA}$ | 0.5x – 35 | | 5 | | ns |
| 7 | ALE high width | $t_{LL}$ | x – 60 | | 20 | | ns |
| 8 | ALE fall → $\overline{RD}$ / $\overline{WR}$ fall | $t_{LC}$ | 0.5x – 35 | | 5 | | ns |
| 9 | $\overline{RD}$ / $\overline{WR}$ rise → ALE rise | $t_{CL}$ | 0.5x – 40 | | 0 | | ns |
| 10 | A0 to A15 valid → $\overline{RD}$ / $\overline{WR}$ fall | $t_{ACL}$ | x – 50 | | 30 | | ns |
| 11 | A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall | $t_{ACH}$ | 1.5x – 50 | | 70 | | ns |
| 12 | $\overline{RD}$ / $\overline{WR}$ rise → A0 to A23 hold | $t_{CA}$ | 0.5x – 40 | | 0 | | ns |
| 13 | A0 to A15 valid → D0 to D15 input | $t_{ADL}$ | | 3.0x – 110 | | 130 | ns |
| 14 | A0 to A23 valid → D0 to D15 input | $t_{ADH}$ | | 3.5x – 125 | | 155 | ns |
| 15 | $\overline{RD}$ fall → D0 to D15 input | $t_{RD}$ | | 2.0x – 115 | | 45 | ns |
| 16 | $\overline{RD}$ low pulse width | $t_{RR}$ | 2.0x – 40 | | 120 | | ns |
| 17 | $\overline{RD}$ rise → D0 to D15 hold | $t_{HR}$ | 0 | | 0 | | ns |
| 18 | $\overline{RD}$ rise → A0 to A15 output | $t_{RAE}$ | x – 25 | | 55 | | ns |
| 19 | $\overline{WR}$ low pulse width | $t_{WW}$ | 2.0x – 40 | | 120 | | ns |
| 20 | D0 to D15 valid → $\overline{WR}$ rise | $t_{DW}$ | 2.0x – 120 | | 40 | | ns |
| 21 | $\overline{WR}$ rise → D0 to D15 hold | $t_{WD}$ | 0.5x – 40 | | 0 | | ns |
| 22 | A0 to A23 valid → $\overline{WAIT}$ input (1 + N) WAIT mode | $t_{AWH}$ | | 3.5x – 130 | | 150 | ns |
| 23 | A0 to A15 valid → $\overline{WAIT}$ input (1 + N) WAIT mode | $t_{AWL}$ | | 3.0x – 100 | | 140 | ns |
| 24 | $\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold (1 + N) WAIT mode | $t_{CW}$ | 2.0x + 0 | | 160 | | ns |
| 25 | A0 to A23 valid → Port input | $t_{APH}$ | | 2.5x – 120 | | 80 | ns |
| 26 | A0 to A23 valid → Port hold | $t_{APH2}$ | 2.5x + 50 | | 250 | | ns |
| 27 | $\overline{WR}$ rise → Port valid | $t_{CP}$ | | 200 | | 200 | ns |

AC measuring conditions

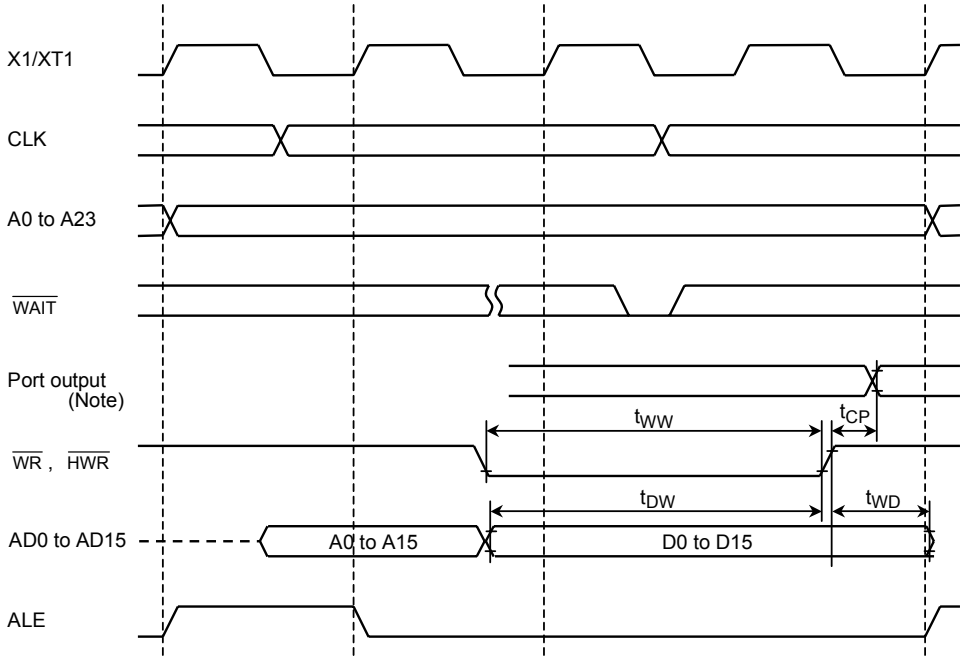
- Output level: High 0.7 × $V_{CC}$/Low 0.3 × $V_{CC}$, CL = 50 pF
- Input level: High 0.9 × $V_{CC}$/Low 0.1 × $V_{CC}$

(1) Read cycle




Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as $\overline{RD}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(2) Write cycle




Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

## 4.4 Serial Channel Timing

### (1) I/O interface mode

#### 1. SCLK input mode

| Parameter | Symbol | Variable | | 32.768 MHz (Note) | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| SCLK cycle | $t_{SCY}$ | 16x | | 488 μs | | 1.28 | | 0.8 | | μs |
| Output data → SCLK rising edge or falling edge* | $t_{OSS}$ | $t_{SCY}/2 - 5x - 50$ | | 91.5 μs | | 190 | | 100 | | ns |
| SCLK rising edge or falling edge* → Output data hold | $t_{OHS}$ | 5x − 100 | | 152 μs | | 300 | | 150 | | ns |
| SCLK rising edge or falling edge* → Input data hold | $t_{HSR}$ | 0 | | 0 | | 0 | | 0 | | ns |
| SCLK rising edge or falling edge* → Effective data input | $t_{SRD}$ | | $t_{SCY} - 5x - 100$ | | 336 μs | | 780 | | 450 | ns |

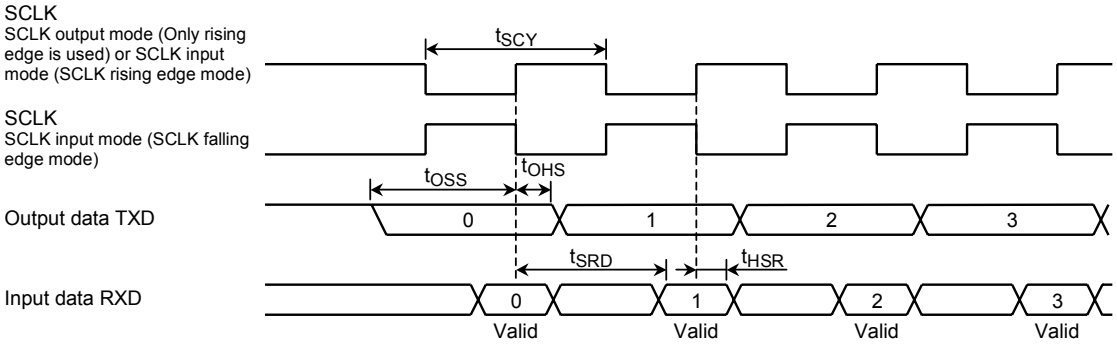
Note: System clock is fs, or input clock to prescaler is divisor clock of fs.

*) The rising edge is used in SCLK Rising mode.
The falling edge is used in SCLK Falling mode.

#### 2. SCLK output mode

| Parameter | Symbol | Variable | | 32.768 kHz (Note) | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| SCLK cycle (Programmable) | $t_{SCY}$ | 16x | 8192x | 488 μs | 250 ms | 1.28 | 655.36 | 0.8 | 409.6 | μs |
| Output data → SCLK rising edge | $t_{OSS}$ | $t_{SCY} - 2x - 150$ | | 427 μs | | 970 | | 550 | | ns |
| SCLK rising edge → Output data hold | $t_{OHS}$ | 2x − 80 | | 60 μs | | 80 | | 20 | | ns |
| SCLK rising edge → Input data hold | $t_{HSR}$ | 0 | | 0 | | 0 | | 0 | | ns |
| SCLK rising edge → Effective data hold | $t_{SRD}$ | | $t_{SCY} - 2x - 150$ | | 428 μs | | 970 | | 550 | ns |

Note: System clock is fs, or input clock to prescaler is divisor clock of fs.




### (2) UART mode (SCLK0 and SCLK1 external input)

| Parameter | Symbol | Variable | | 32.768 kHz (Note) | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| SCLK cycle | $t_{SCY}$ | 4x + 20 | | 122 μs | | 340 | | 220 | | ns |
| SCLK low level pulse width | $t_{SCYL}$ | 2x + 5 | | 6 μs | | 165 | | 105 | | ns |
| SCLK high level pulse width | $t_{SCYH}$ | 2x + 5 | | 6 μs | | 165 | | 105 | | ns |

Note: System clock is fs, or input clock to prescaler is divisor clock of fs.

## 4.5 AD Converter Characteristics

($V_{SS}$ = 0 V, $AV_{CC}$ = $V_{CC}$, $AV_{SS}$ = $V_{SS}$, Ta = –40 to 85°C)

$AV_{CC}$ = $V_{CC}$, $AV_{SS}$ = $V_{SS}$

| Parameter | Symbol | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Analog reference voltage (+) | $V_{REFH}$ | $V_{CC}$ = 5 V ± 10% | $V_{CC}$ – 1.5 V | $V_{CC}$ | $V_{CC}$ | V |
| | | $V_{CC}$ = 3 V ± 10% | $V_{CC}$ – 0.2 V | $V_{CC}$ | $V_{CC}$ | |
| Analog reference voltage (–) | $V_{REFL}$ | $V_{CC}$ = 5 V ± 10% | $V_{SS}$ | | | |
| | | $V_{CC}$ = 3 V ± 10% | $V_{SS}$ | | | |
| Analog input voltage range | $V_{AIN}$ | | $V_{REFL}$ | | $V_{REFH}$ | |
| Analog current for analog reference voltage <VREFON> = 1 | $I_{REF}$ ($V_{REFL}$ = 0 V) | $V_{CC}$ = 5 V ± 10% | | 1.6 | 2.0 | mA |
| | | $V_{CC}$ = 3 V ± 10% | | 1.0 | 1.5 | |
| <VREFON> = 0 | | $V_{CC}$ = 2.7~5.5 V | | 0.02 | 5.0 | μA |
| Error (Not including quantizing errors) | – | $V_{CC}$ = 5 V ± 10% | | ±1.0 | ±3.0 | LSB |
| | | $V_{CC}$ = 3 V ± 10% | | ±1.0 | ±5.0 | |

Note 1: 1LSB = $(V_{REFH} - V_{REFL})/2^{10}$ [V]

Note 2: Minimum operation frequency.

The operation of the AD converter is guaranteed only when fc (High-frequency oscillator) is used. (It is not guaranteed when fs is used.) Additionally, it is guaranteed when the clock frequency which is selected by the clock gear is 4 MHz or more.

Note 3: The value $I_{CC}$ includes the current which flows through the $AV_{CC}$ pin.

## 4.6 LCD Driver Characteristics

| Charge and Pump Characteristics | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|
| Reference input voltage | $V_{L1}$ | 0.9 | | 1.83 | V |
| Output voltage V2 pin | $V_{L2}$ | | 2 × $V_{L1}$ | | |
| V3 pin | $V_{L3}$ | | 3 × $V_{L1}$ | | |
| External capacity C0, C1 | $C_{PMP}$ | 0.1 | | 1.0 | μF |
| V1 pin | $C_{VL1}$ | 0.1 | | 1.0 | |
| V2 pin | $C_{VL2}$ | 0.1 | | 1.0 | |
| V3 pin | $C_{VL3}$ | 0.1 | | 1.0 | |

Note: Output voltage and External capacity are not loaded.

## 4.7 Event Counter (TI0, TI2, TI4, TI6, TI8 to TIB)

| Parameter | Symbol | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Clock cycle | $t_{VCK}$ | 8X + 100 | | 740 | | 500 | | ns |
| Low level clock pulse width | $t_{VCKL}$ | 4X + 40 | | 360 | | 240 | | ns |
| High level clock pulse width | $t_{VCKH}$ | 4X + 40 | | 360 | | 240 | | ns |

## 4.8 Interrupt and Capture

(1) $\overline{NMI}$, INT0 to INT4 interrupts and INTKEY interrupt

| Parameter | Symbol | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Low level pulse width | $t_{INTAL}$ | 4X | | 320 | | 200 | | ns |
| High level pulse width | $t_{INTAH}$ | 4X | | 320 | | 200 | | ns |

(2) INT7 to INTB interrupts and capture

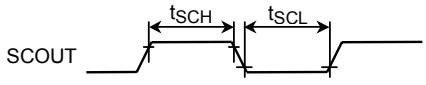
| Parameter | Symbol | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Low level pulse width | $t_{INTBL}$ | 4X + 100 | | 420 | | 300 | | ns |
| High level pulse width | $t_{INTBH}$ | 4X + 100 | | 420 | | 300 | | ns |

## 4.9 SCOUT Pin AC Characteristics

| Parameter | Symbol | Variable | | 12.5 MHz | | 20 MHz | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| High level pulse width $V_{CC}$ = 5 V ± 10% | $t_{SCH}$ | 0.5X – 10 | | 30 | | 15 | | ns |
| High level pulse width $V_{CC}$ = 3 V ± 10% | | 0.5X – 20 | | 20 | | – | – | |
| Low level pulse width $V_{CC}$ = 5 V ± 10% | $t_{SCL}$ | 0.5X – 10 | | 30 | | 15 | | ns |
| Low level pulse width $V_{CC}$ = 3 V ± 10% | | 0.5X – 20 | | 20 | | – | – | |

Measurement condition

- Output level: High 2.2 V/Low 0.8 V, CL = 10 pF

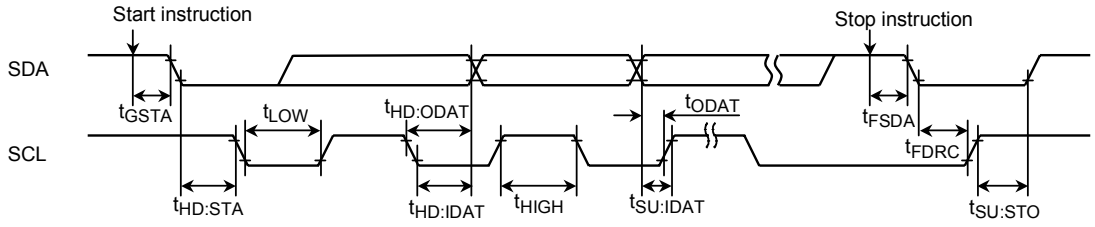


## 4.10 Timing Chart for Serial Bus Interface

(1) I²C bus mode

| Parameter | Symbol | Variable | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ. | Max | |
| START instruction → SDA falling edge | $t_{GSTA}$ | 3X | | | s |
| Start condition hold time | $t_{HD:STA}$ | $2^nX$ | | | s |
| SCL low level pulse width | $t_{LOW}$ | $2^nX$ | | | s |
| SCL high level pulse width | $t_{HIGH}$ | $2^nX + 12X$ | | | s |
| Data hold time (Input) | $t_{HD:IDAT}$ | 0 | | | ns |
| Data setup time (Input) | $t_{SU:IDAT}$ | 250 | | | ns |
| Data hold time (Output) | $t_{HD:ODAT}$ | 7X | | 11X | s |
| Data valid → SCL rising edge | $t_{ODAT}$ | | $2^nX - t_{HD:ODAT}$ | | s |
| STOP instruction → SDA falling edge | $t_{FSDA}$ | 3X | | | s |
| SDA falling edge → SCL rising edge | $t_{FDRC}$ | $2^nX$ | | | s |
| Stop condition hold time | $t_{SU:STO}$ | $2^nX + 16X$ | | | s |

Note: SBICR1<SCK2:0> sets n.



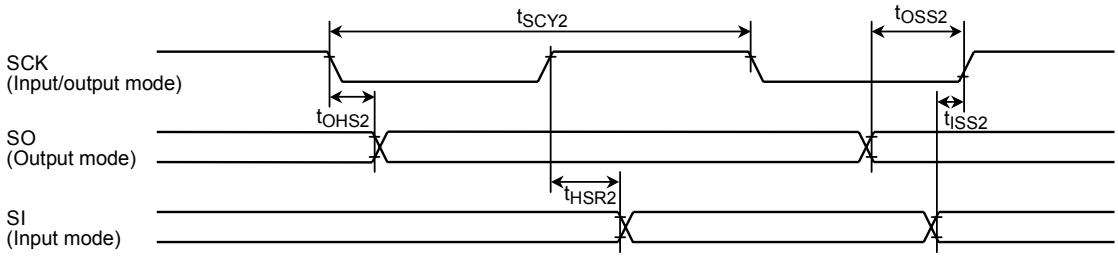
(2) Clock-synchronous 8-bit SIO mode (Serial bus interface) clock

1. SCK input mode

| Parameter | Symbol | Variable | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SCK cycle | $t_{SCY2}$ | $2^5X$ | | s |
| SCK falling edge → Output data hold | $t_{OHS2}$ | 6X | | s |
| Output data → SCK rising edge | $t_{OSS2}$ | $t_{SCY2}$ − 6X | | s |
| SCK rising edge → Input data hold | $t_{HSR2}$ | 6X | | ns |
| Input data → SCK rising edge | $t_{ISS2}$ | 0 | | ns |

2. SCK output mode

| Parameter | Symbol | Variable | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| SCK cycle | $t_{SCY2}$ | $2^5X$ | $2^{11}X$ | s |
| SCK falling edge → Output data hold | $t_{OHS2}$ | 2X | | s |
| Output data → SCK rising edge | $t_{OSS2}$ | $t_{SCY2}$ − 2X | | s |
| SCK rising edge → Input data hold | $t_{HSR2}$ | 2X | | s |
| Input data → SCK rising edge | $t_{ISS2}$ | 0 | | ns |



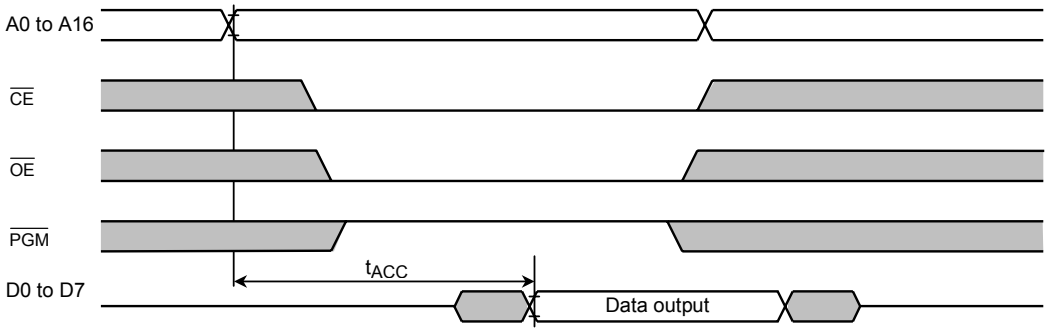
## 4.11 Operation in PROM Mode

(1) DC and AC characteristics in read operation

Ta = 25 ± 5°C $V_{CC}$ = 5 V ± 10%

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{PP}$ read voltage | $V_{PP}$ | – | 4.5 | 5.5 | V |
| Input high voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$) | $V_{IH1}$ | – | 2.2 | $V_{CC}$ + 0.3 | |
| Input low voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$) | $V_{IL1}$ | – | –0.3 | 0.8 | |
| Address to output delay | $t_{ACC}$ | $C_L$ = 50 pF | – | 2.25 $T_{CYC}$ + α | ns |

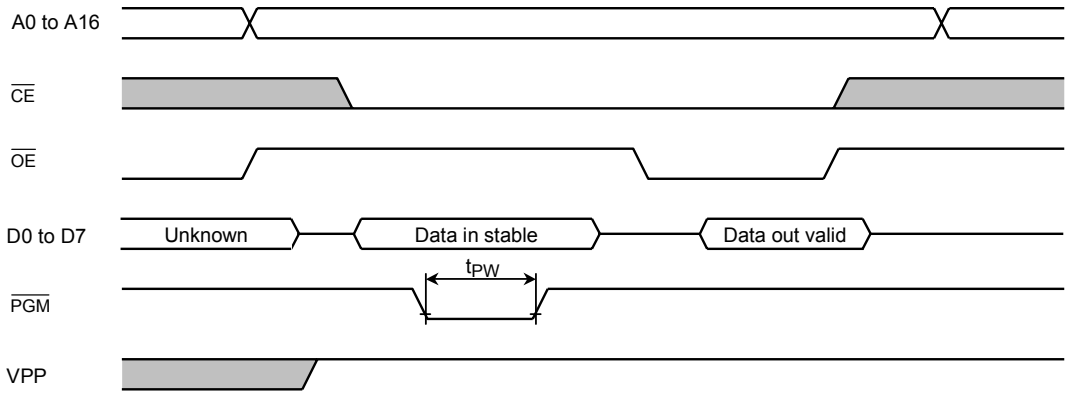
$T_{CYC}$ = 400 ns (10 MHz clock)
α = 200 ns



(2) DC and AC characteristics in programming

Ta = 25 ± 5°C $V_{CC}$ = 6.25 V ± 0.25 V

| Parameter | Symbol | Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| Programming supply voltage | $V_{PP}$ | – | 12.50 | 12.75 | 13.00 | V |
| Input high voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$) | $V_{IH}$ | – | 2.6 | | $V_{CC}$ + 0.3 | |
| Input low voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$) | $V_{IL}$ | – | –0.3 | | 0.8 | |
| $V_{CC}$ supply current | $I_{CC}$ | fc = 10 MHz | – | | 50 | mA |
| $V_{PP}$ supply current | $I_{PP}$ | $V_{PP}$ = 13.00 V | – | | 50 | |
| $\overline{PGM}$ program pulse width | $t_{PW}$ | $C_L$ = 50 pF | 0.095 | 0.1 | 0.105 | ms |




Note 1: The power supply of $V_{PP}$ (12.75 V) must be turned on at the same time or the later time for a power supply of $V_{CC}$ and must be turned off at the same time or early time for a power supply of $V_{CC}$.

Note 2: The device suffers a damage taking out and putting in on the condition of $V_{PP}$ = 12.75 V.

Note 3: The maximum spec of $V_{PP}$ pin is 14.0 V. Be carefull a overshoot at the programming.

# 5. Port Section Equivalent Circuit Diagram

- Reading the circuit diagram

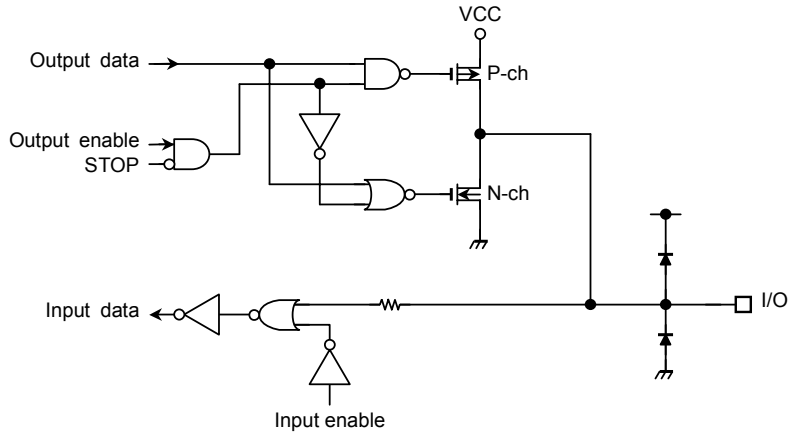
  Basically, the gate symbols written are the same as those used for the standard CMOS logic IC [74HCXX] series.

  The dedicated signal is described below.

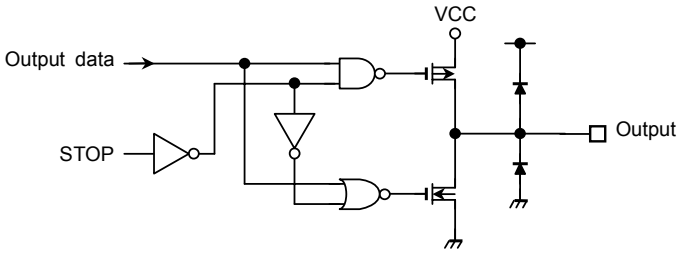
  Stop: This signal becomes active 1 when the HALT mode setting register is set to the Stop mode and the CPU executes the HALT instruction. When the drive enable bit [DRVE] is set to 1, however, Stop remains at 0.

- The input protection resistance ranges from several tens of ohms to several hundreds of ohms.

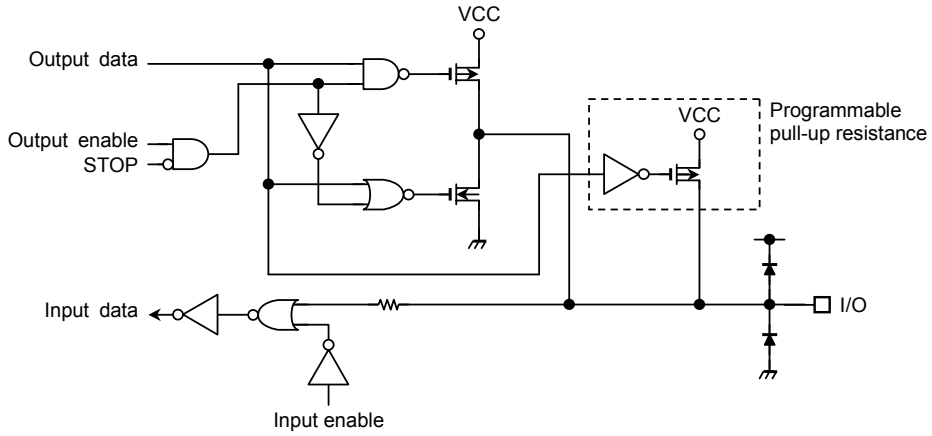
  ■ P0 (AD0 to AD7), P1 (AD8 to AD15, A8 to A15), and P67 (TO1)



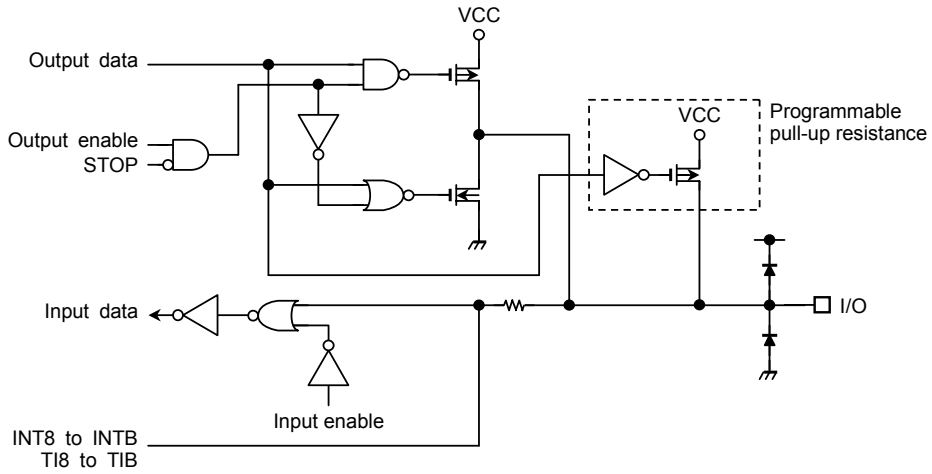

  ■ P30 ($\overline{RD}$) and P31 ($\overline{WR}$)



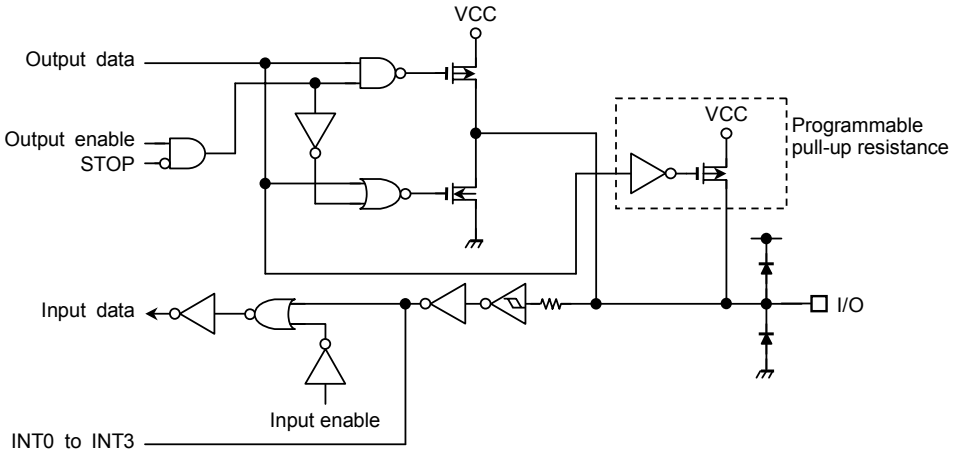
■ P2 (A16 to A23, A0 to A7), P32 (HWR), P72 (TO8), P73 (SCOUT), and P76 (TOA)



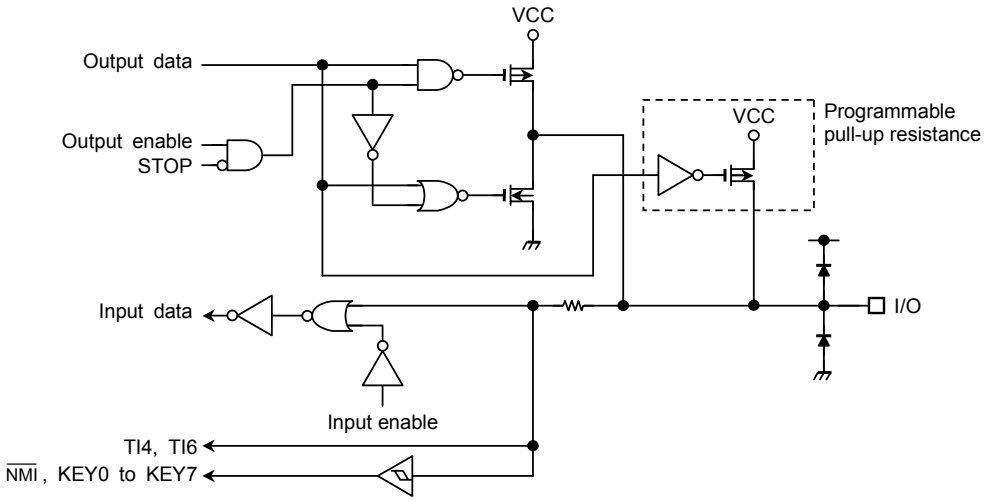

■ P70 (TI8/INT8), P71 (TI9/INT9), P74 (TIA/INTA), and P75 (TIB/INTB)



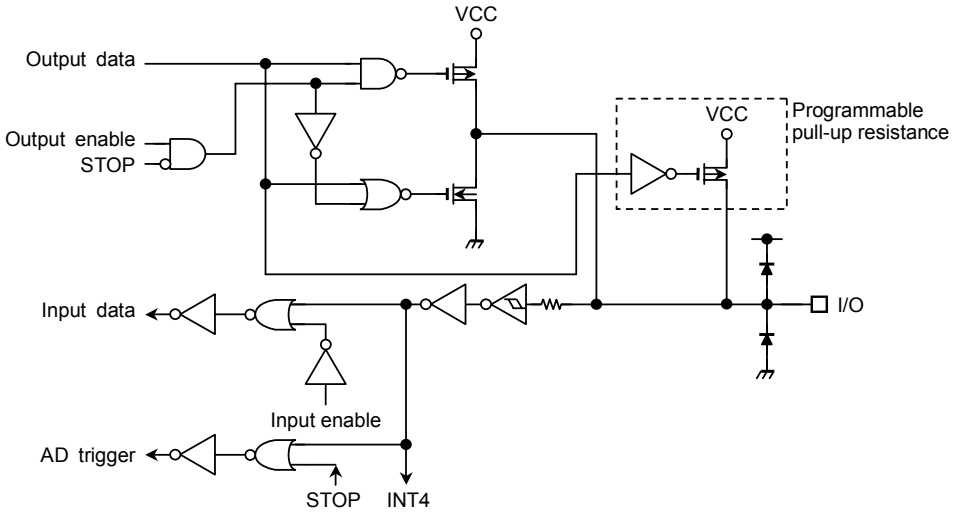

■ P33 to P36 (INT0 to INT3)



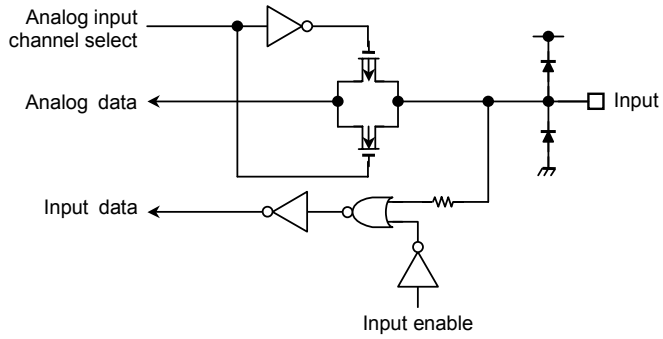
■ P4 (TIx, TOx, KEYx) and P77 ($\overline{\text{NMI}}$)



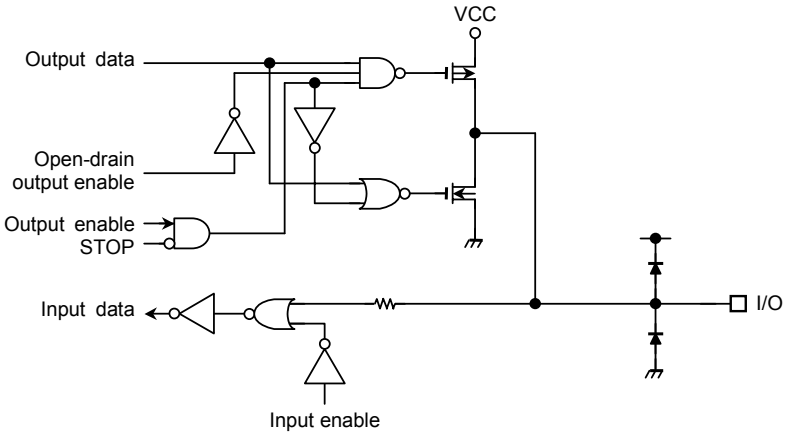

■ P37 (INT4/$\overline{\text{ADTRG}}$)



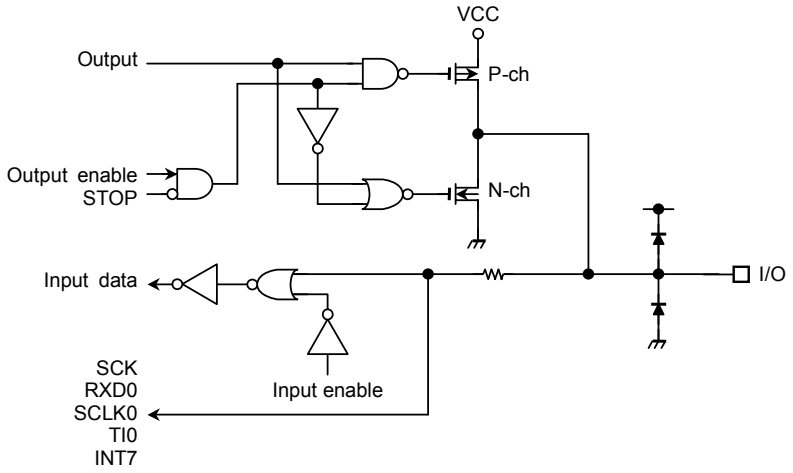

■ P5 (AN0 to AN7)



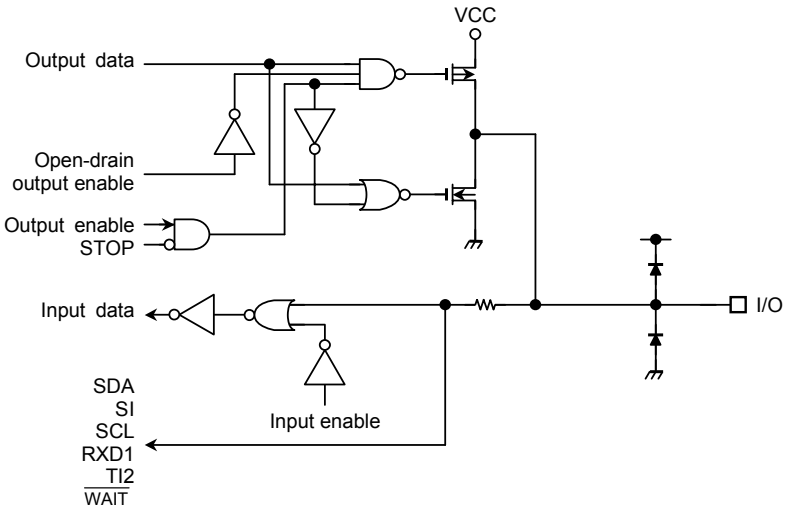
■ P63 (TXD0), P80 (TXD1), P83 (TO3), and P85



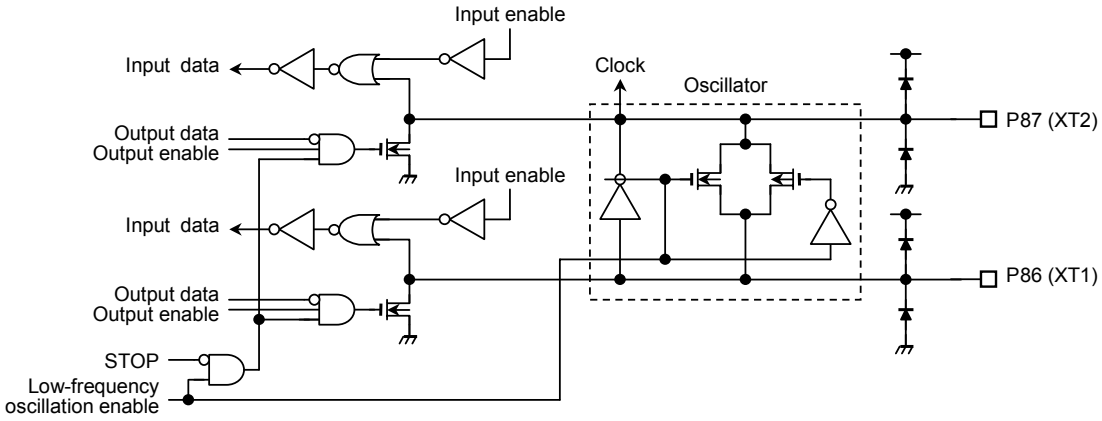

■ P60 (SCK), P64 (RXD0), P65 (SCLK0), and P66 (TI0/INT7)



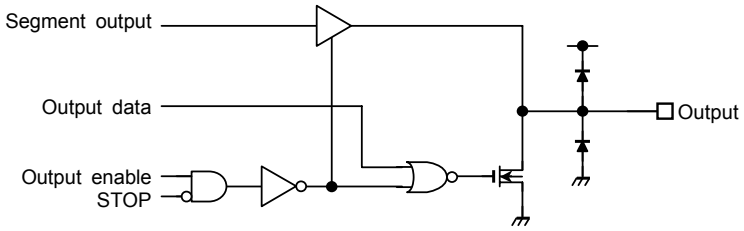
■ P61 (SO/SDA), P62 (SI/SCL), P81 (RXD1), P82 (TI2), and P84 ($\overline{\text{WAIT}}$)



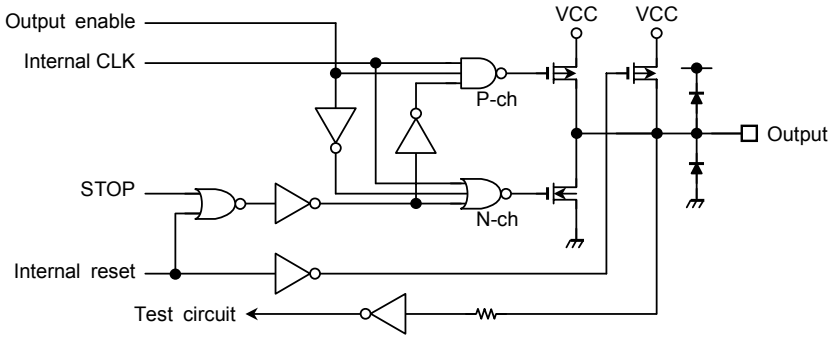

■ P86 (XT1) and P87 (XT2)



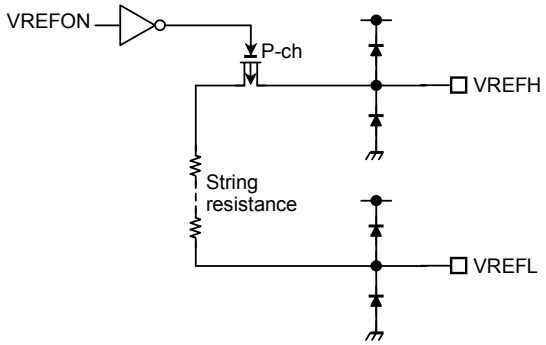
■ P90 to P97 (SEG24 to SEG31), PA0 to PA7 (SEG32 to SEG39)



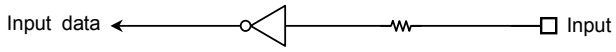

■ CLK



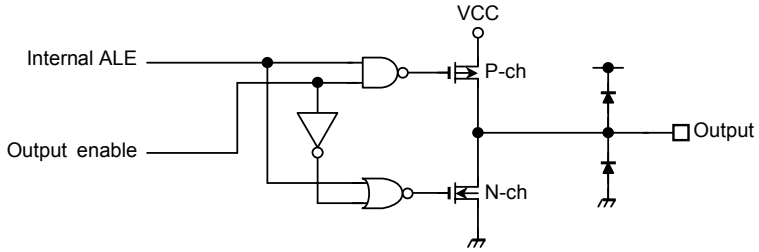

■ VREFH and VREFL



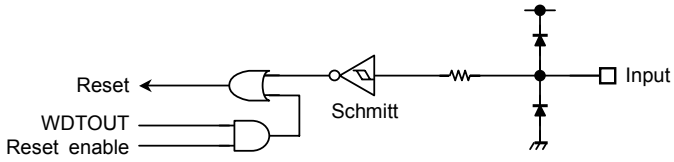
■ $\overline{EA}$



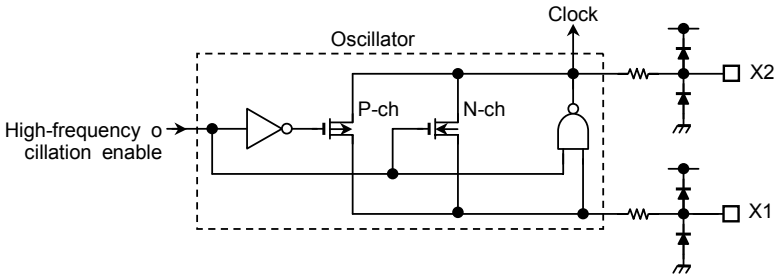

■ ALE




■ $\overline{RESET}$




■ X1 and X2



# 6. Package Dimensions

P-LQFP144-1616-0.40

Unit: mm