MF1393-05

S1D15E06 Series

Rev. 2.1

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Contents

1. DESCRIPTION

The S1D15E06 series is a single chip MLS driver for dot matrix liquid crystal displays which can be directly connected to the microcomputer bus. It accepts the 8-bit parallel or serial display data from the microcomputer to store the data in the on-chip display data RAM, and issues liquid crystal drive signals independently of the microcomputer.

The S1D15E06 series provides both 4 gray-scale display and binary display. It incorporates a display data RAM ($132 \times 160 \times 2$ bits). In the case of 4 gray-scale display, 2 bits of the on-chip RAM respond to one-dot pixels, while in the case of binary display, 1 bit of the on-chip RAM respond to one-dot pixels.

The S1D15E06 series features 132 common output circuits and 160 segment output circuits. A single chip provides a display of 10 characters by 8 lines with 132 $\times$ 160 dots (16×16 dots) and display of 13 characters by 11 lines by the 12×12 dot-character font.

Display data RAM read/write operations do not require operation clock from outside, thereby ensuring operation with the minimum current consumption. Furthermore, it incorporates a LCD-drive power supply characterized by low power consumption and a CR oscillator circuit for display clock; therefore, the display system of a handy and high-performance instrument can be realized by use of the minimum current consumption and minimum chip configuration.

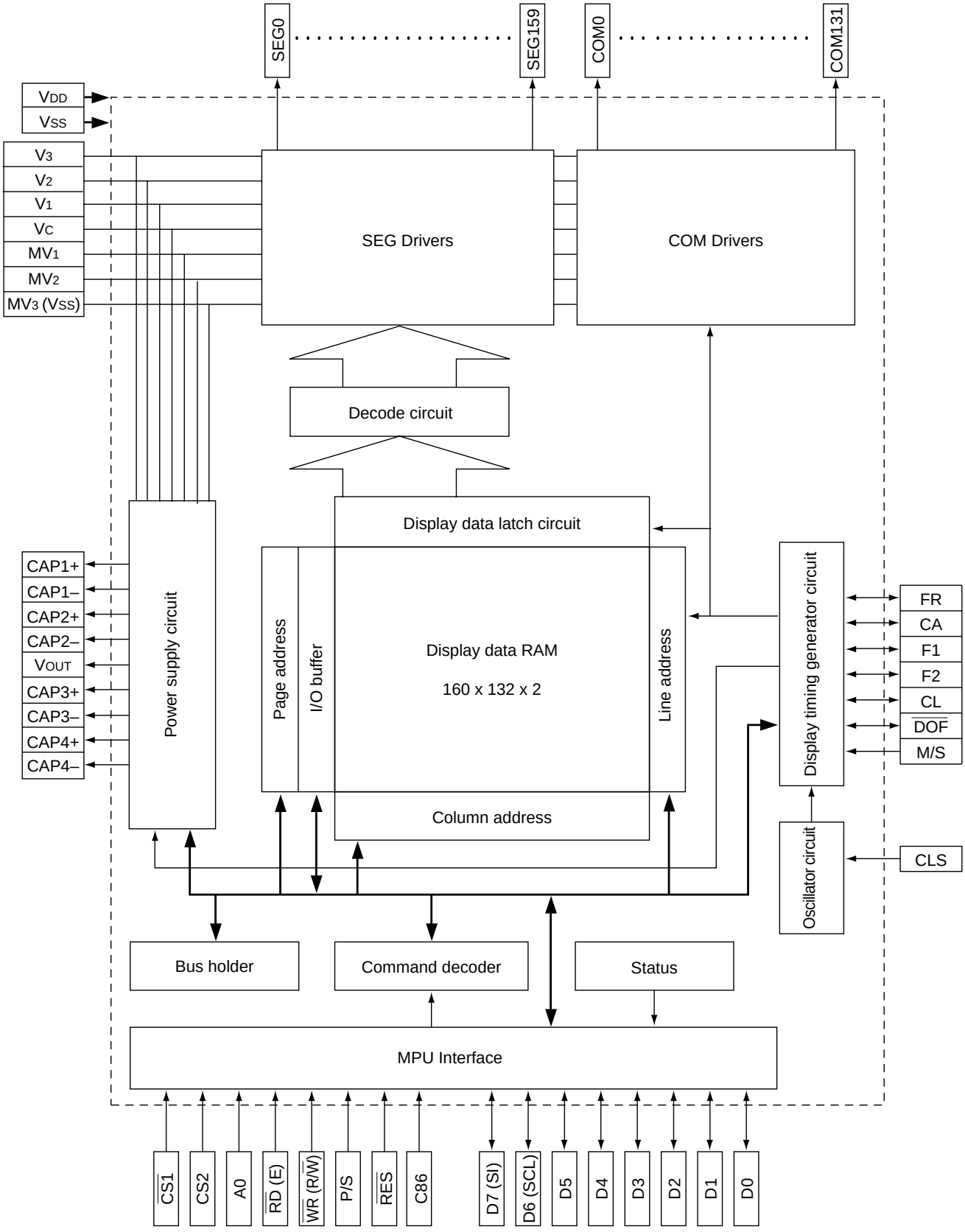
2. FEATURES

- Direct RAM data display by display data RAM
  - 4 gray-scale display
    (Normally white in normal display mode)
    RAM bit data (high order and low order)
    (1,1) : gray-scale 3, black
    (1,0) : gray-scale 2
    (0,1) : gray-scale 1
    (0,0) : gray-scale 0, white
  - Binary display
    (Normally white display is in normal mode)
    RAM bit data
    "1" : On and black
    "0" : Off and white
- RAM capacity
  $132 \times 160 \times 2 = 42{,}240$ bits
- Liquid crystal drive circuit
  132 common outputs and 160 segment outputs
- High-speed 8-bit MPU interface (directly connectable to the MPUs of both 80/68 series) /serial interface possible
- A variety of command functions
  Area scroll display, partial display, n-line reversal, display data RAM address control, contrast control, display ON/OFF, display normal/reverse rotation, display all lighting ON/OFF, liquid crystal drive power supply circuit control, display clock built-in oscillator circuit control
- Lower power MLS drive technology
  Built-in high precision voltage regulation function
- High precision CR oscillator circuit incorporated
- Very low power consumption
- Power supply
  Logic power supply: $V_{DD} - V_{SS}$ = 1.7 to 3.6 V
  Liquid crystal drive power supply:
  $V_3 - V_{SS}$ = 3.4 to 14.0 V (S1D15E06D01****),
  $V_3 - V_{SS}$ = 3.4 to 16.0 V (S1D15E06D03****)
- Wide operation temperature range: –40 to 85°C
- CMOS process
- Shipping form : Bare chips, TCP
- Light and radiation proof measures are not taken in designing.

Series specifications

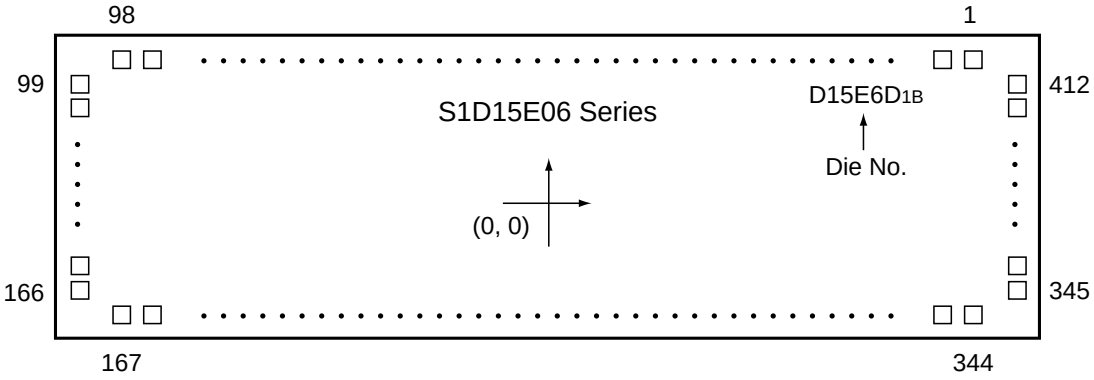
Product name	Bias	LCD driving voltage range	Duty (Max.)	Form of shipping	Chip thickness
S1D15E06D01B000	1/7	3.4V~14.0V	1/132	Bare chip	0.400mm
S1D15E06D03B000	1/7	3.4V~16.0V	1/132	Bare chip	0.400mm
S1D15E06D01E000	1/7	3.4V~14.0V	1/132	Bare chip	0.625mm
S1D15E06D03E000	1/7	3.4V~16.0V	1/132	Bare chip	0.625mm
S1D15E06T00A00A	1/7	3.4V~14.0V	1/132	TCP	—

3. BLOCK DIAGRAM



4. PIN ASSIGNMENT

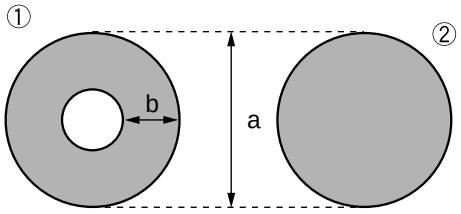
4.1 Chip Assignment



Item		Size X	Size Y	Unit
Chip size		10.26	3.98	mm
Chip thickness		0.4/0.625		mm
Bump pitch		50 (Min.)		µm
Bump size	PAD No.1 to 98	70	92	µm
	PAD No.99 to 166, 345 to 412	116	33	µm
	PAD No.167 to 175, 336 to 344	61	61	µm
	PAD No.176 to 335	33	116	µm
Bump height		22.5 (Typ.)		µm

4.2 Alignment mark

Alignment coordinate
① (–4761.4, 1830.0) µm
② (4926.0, –1819.1) µm
Mark size
a = 80 µm
b = 20 µm



4.3 Pad Center Coordinates

Unit: µm

PAD No.	Pin Name	X	Y
1	NC	4494	1830
2	NC	4402	↓
3	TEST0	4310	
4	TEST1	4218	
5	TEST2	4126	
6	TEST3	4034	
7	TEST4	3942	
8	TEST5	3850	
9	V_{SS}	3742	
10	TEST6	3634	
11	TEST7	3542	
12	TEST8	3450	
13	TEST9	3358	
14	TEST10	3266	
15	TEST11	3174	
16	TEST12	3082	
17	TEST13	2990	
18	TEST14	2898	
19	TEST15	2806	
20	TEST16	2714	
21	TEST17	2622	
22	TEST18	2530	
23	V_{SS}	2422	
24	FR	2314	
25	$\overline{CL}$	2222	
26	$\overline{DOF}$	2130	
27	F1	2038	
28	F2	1946	
29	CA	1854	
30	V_{SS}	1762	
31	$\overline{TEST}$	1670	
32	$\overline{CS1}$	1578	
33	$\overline{RES}$	1486	
34	$\overline{A0}$	1394	
35	$\overline{WR}$, R/$\overline{W}$	1302	
36	$\overline{RD}$, E	1210	
37	CS2	1118	
38	V_{DD}	1026	
39	M/S	934	
40	V_{SS}	842	
41	CLS	750	
42	V_{DD}	658	
43	C86	566	
44	V_{SS}	474	
45	P/S	382	
46	V_{DD}	290	
47	D0	198	
48	D1	106	
49	D2	14	
50	D3	–78	↓

PAD No.	Pin Name	X	Y
51	D4	–170	1830
52	D5	–262	↓
53	D6, SCL	–354	
54	D7, SI	–446	
55	V_{SS}	–538	
56	V_{SS}	–630	
57	V_{SS}	–722	
58	V_{DD}	–814	
59	V_{DD}	–906	
60	V_{DD}	–998	
61	V_{OUT}	–1090	
62	V_{OUT}	–1182	
63	CAP1+	–1274	
64	CAP1+	–1366	
65	CAP1–	–1458	
66	CAP1–	–1550	
67	CAP2–	–1642	
68	CAP2–	–1734	
69	CAP2+	–1826	
70	CAP2+	–1918	
71	CAP3+	–2010	
72	CAP3+	–2102	
73	CAP3–	–2194	
74	CAP3–	–2286	
75	CAP4–	–2378	
76	CAP4–	–2470	
77	CAP4+	–2562	
78	CAP4+	–2654	
79	V_3	–2746	
80	V_3	–2838	
81	V_2	–2930	
82	V_2	–3022	
83	V_1	–3114	
84	V_1	–3206	
85	V_C	–3298	
86	V_C	–3390	
87	MV_1	–3482	
88	MV_1	–3574	
89	MV_2	–3666	
90	MV_2	–3758	
91	MV_3	–3850	
92	MV_3	–3942	
93	CPP+	–4034	
94	CPP–	–4126	
95	CPM+	–4218	
96	CPM–	–4310	
97	NC	–4402	
98	NC	–4494	↓
99	NC	–4958	1675
100	COM65	↓	1625

PAD No.	Pin Name	X	Y
101	COM64	–4958	1575
102	COM63	↓	1525
103	COM62		1475
104	COM61		1425
105	COM60		1375
106	COM59		1325
107	COM58		1275
108	COM57		1225
109	COM56		1175
110	COM55		1125
111	COM54		1075
112	COM53		1025
113	COM52		975
114	COM51		925
115	COM50		875
116	COM49		825
117	COM48		775
118	COM47		725
119	COM46		675
120	COM45		625
121	COM44		575
122	COM43		525
123	COM42		475
124	COM41		425
125	COM40		375
126	COM39		325
127	COM38		275
128	COM37		225
129	COM36		175
130	COM35		125
131	COM34		75
132	COM33		25
133	COM32		–25
134	COM31		–75
135	COM30		–125
136	COM29		–175
137	COM28		–225
138	COM27		–275
139	COM26		–325
140	COM25		–375
141	COM24		–425
142	COM23		–475
143	COM22		–525
144	COM21		–575
145	COM20		–625
146	COM19		–675
147	COM18		–725
148	COM17		–775
149	COM16		–825
150	COM15	↓	–875

Unit: µm

PAD No.	Pin Name	X	Y
151	COM14	–4958	–925
152	COM13		–975
153	COM12		–1025
154	COM11		–1075
155	COM10		–1125
156	COM9		–1175
157	COM8		–1225
158	COM7		–1275
159	COM6		–1325
160	COM5		–1375
161	COM4		–1425
162	COM3		–1475
163	COM2		–1525
164	COM1		–1575
165	COM0		–1625
166	NC		–1675
167	NC	–4704	–1846
168	NC	–4621	
169	NC	–4539	
170	NC	–4456	
171	NC	–4374	
172	NC	–4291	
173	NC	–4209	
174	NC	–4126	
175	NC	–4044	
176	SEG0	–3975	–1818
177	SEG1	–3925	
178	SEG2	–3875	
179	SEG3	–3825	
180	SEG4	–3775	
181	SEG5	–3725	
182	SEG6	–3675	
183	SEG7	–3625	
184	SEG8	–3575	
185	SEG9	–3525	
186	SEG10	–3475	
187	SEG11	–3425	
188	SEG12	–3375	
189	SEG13	–3325	
190	SEG14	–3275	
191	SEG15	–3225	
192	SEG16	–3175	
193	SEG17	–3125	
194	SEG18	–3075	
195	SEG19	–3025	
196	SEG20	–2975	
197	SEG21	–2925	
198	SEG22	–2875	
199	SEG23	–2825	
200	SEG24	–2775	

PAD No.	Pin Name	X	Y
201	SEG25	–2725	–1818
202	SEG26	–2675	
203	SEG27	–2625	
204	SEG28	–2575	
205	SEG29	–2525	
206	SEG30	–2475	
207	SEG31	–2425	
208	SEG32	–2375	
209	SEG33	–2325	
210	SEG34	–2275	
211	SEG35	–2225	
212	SEG36	–2175	
213	SEG37	–2125	
214	SEG38	–2075	
215	SEG39	–2025	
216	SEG40	–1975	
217	SEG41	–1925	
218	SEG42	–1875	
219	SEG43	–1825	
220	SEG44	–1775	
221	SEG45	–1725	
222	SEG46	–1675	
223	SEG47	–1625	
224	SEG48	–1575	
225	SEG49	–1525	
226	SEG50	–1475	
227	SEG51	–1425	
228	SEG52	–1375	
229	SEG53	–1325	
230	SEG54	–1275	
231	SEG55	–1225	
232	SEG56	–1175	
233	SEG57	–1125	
234	SEG58	–1075	
235	SEG59	–1025	
236	SEG60	–975	
237	SEG61	–925	
238	SEG62	–875	
239	SEG63	–825	
240	SEG64	–775	
241	SEG65	–725	
242	SEG66	–675	
243	SEG67	–625	
244	SEG68	–575	
245	SEG69	–525	
246	SEG70	–475	
247	SEG71	–425	
248	SEG72	–375	
249	SEG73	–325	
250	SEG74	–275	

PAD No.	Pin Name	X	Y
251	SEG75	–225	–1818
252	SEG76	–175	
253	SEG77	–125	
254	SEG78	–75	
255	SEG79	–25	
256	SEG80	25	
257	SEG81	75	
258	SEG82	125	
259	SEG83	175	
260	SEG84	225	
261	SEG85	275	
262	SEG86	325	
263	SEG87	375	
264	SEG88	425	
265	SEG89	475	
266	SEG90	525	
267	SEG91	575	
268	SEG92	625	
269	SEG93	675	
270	SEG94	725	
271	SEG95	775	
272	SEG96	825	
273	SEG97	875	
274	SEG98	925	
275	SEG99	975	
276	SEG100	1025	
277	SEG101	1075	
278	SEG102	1125	
279	SEG103	1175	
280	SEG104	1225	
281	SEG105	1275	
282	SEG106	1325	
283	SEG107	1375	
284	SEG108	1425	
285	SEG109	1475	
286	SEG110	1525	
287	SEG111	1575	
288	SEG112	1625	
289	SEG113	1675	
290	SEG114	1725	
291	SEG115	1775	
292	SEG116	1825	
293	SEG117	1875	
294	SEG118	1925	
295	SEG119	1975	
296	SEG120	2025	
297	SEG121	2075	
298	SEG122	2125	
299	SEG123	2175	
300	SEG124	2225	

Unit: µm

PAD No.	Pin Name	X	Y
301	SEG125	2275	–1818
302	SEG126	2325	
303	SEG127	2375	
304	SEG128	2425	
305	SEG129	2475	
306	SEG130	2525	
307	SEG131	2575	
308	SEG132	2625	
309	SEG133	2675	
310	SEG134	2725	
311	SEG135	2775	
312	SEG136	2825	
313	SEG137	2875	
314	SEG138	2925	
315	SEG139	2975	
316	SEG140	3025	
317	SEG141	3075	
318	SEG142	3125	
319	SEG143	3175	
320	SEG144	3225	
321	SEG145	3275	
322	SEG146	3325	
323	SEG147	3375	
324	SEG148	3425	
325	SEG149	3475	
326	SEG150	3525	
327	SEG151	3575	
328	SEG152	3625	
329	SEG153	3675	
330	SEG154	3725	
331	SEG155	3775	
332	SEG156	3825	
333	SEG157	3875	
334	SEG158	3925	
335	SEG159	3975	
336	NC	4044	–1846
337	NC	4126	
338	NC	4209	
339	NC	4291	
340	NC	4374	
341	NC	4456	
342	NC	4539	
343	NC	4621	
344	NC	4704	
345	NC	4958	–1675
346	COM66		–1625
347	COM67		–1575
348	COM68		–1525
349	COM69		–1475
350	COM70		–1425

PAD No.	Pin Name	X	Y
351	COM71	4958	–1375
352	COM72		–1325
353	COM73		–1275
354	COM74		–1225
355	COM75		–1175
356	COM76		–1125
357	COM77		–1075
358	COM78		–1025
359	COM79		–975
360	COM80		–925
361	COM81		–875
362	COM82		–825
363	COM83		–775
364	COM84		–725
365	COM85		–675
366	COM86		–625
367	COM87		–575
368	COM88		–525
369	COM89		–475
370	COM90		–425
371	COM91		–375
372	COM92		–325
373	COM93		–275
374	COM94		–225
375	COM95		–175
376	COM96		–125
377	COM97		–75
378	COM98		–25
379	COM99		25
380	COM100		75
381	COM101		125
382	COM102		175
383	COM103		225
384	COM104		275
385	COM105		325
386	COM106		375
387	COM107		425
388	COM108		475
389	COM109		525
390	COM110		575
391	COM111		625
392	COM112		675
393	COM113		725
394	COM114		775
395	COM115		825
396	COM116		875
397	COM117		925
398	COM118		975
399	COM119		1025
400	COM120		1075

PAD No.	Pin Name	X	Y
401	COM121	4958	1125
402	COM122		1175
403	COM123		1225
404	COM124		1275
405	COM125		1325
406	COM126		1375
407	COM127		1425
408	COM128		1475
409	COM129		1525
410	COM130		1575
411	COM131		1625
412	NC		1675

5. PIN DESCRIPTION

5.1 Power Pin

Pin name	I/O	Description	Number of pins
V_{DD}	Power supply	Connect to system MPU power supply pin V_{CC}.	6
V_{SS}	Power supply	Connect to the system GND. MV_3 is short circuited with M_{V3} inside the IC chip.	8
V_3, V_2, V_1, V_C, MV_1, MV_2, MV_3, (=V_{SS})	Power supply	A liquid crystal drive multi-level power supply. The voltages determined by the liquid crystal cell are impedance-converted by resistive divider and operational amplifier for application. The following order must be maintained: $V_3 \geq V_2 \geq V_1 \geq V_C \geq MV_1 \geq MV_2 \geq MV_3$ (=V_{SS}) Master operation: When power supply is turned on, the following voltage is applied to each pin by the built-in power supply circuit. MV_3 is connected to with V_{SS} inside the IC chip. V_2 11/14 • V_3 V_1 9/14 • V_3 V_C 7/14 • V_3 MV_1 5/14 • V_3 MV_2 3/14 • V_3	14 (2 each)

5.2 LCD Power Supply Circuit Pin

Pin name	I/O	Description	Number of pins
CAP1+	O	Pin connected to the positive side of the step-up capacitor. Connect the capacitor between this pin and CAP1– pin.	2
CAP1–	O	Pin connected to the negative side of the step-up capacitor. Connect the capacitor between this pin and CAP1+ pin.	2
CAP2+	O	Pin connected to the positive side of the step-up capacitor. Connect the capacitor between this pin and CAP2– pin.	2
CAP2–	O	Pin connected to the negative side of the step-up capacitor. Connect the capacitor between this pin and CAP2+ pin.	2
V_{OUT}	O	Output pin for step-up. Connect the capacitor between this pin and V_{DD}.	2
CAP3+	O	Pin connected to the positive side of the step-up capacitor. Connect the capacitor between this pin and CAP3– pin.	2
CAP3–	O	Pin connected to the negative side of the step-up capacitor. Connect the capacitor between this pin and CAP3+ pin.	2
CAP4+	O	Pin connected to the positive side of the step-up capacitor. Connect the capacitor between this pin and CAP4– pin.	2
CAP4–	O	Pin connected to the negative side of the step-up capacitor. Connect the capacitor between this pin and CAP4+ pin.	2
CPP+	O	Keep it open.	1
CPP–	O	Keep it open.	1
CPM+	O	Keep it open.	1
CPM–	O	Keep it open.	1

5.3 System Bus Connection Pin

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>D7 to D0

(SI)
(SCL)</td><td>I/O</td><td>Connects to the 8-bit or 16-bit MPU data bus via the 8-bit bi-directional data bus.
When the serial interface is selected (P/S = LOW), D7 serves as the serial data input (SI) and D6 serves as the serial clock input (SCL), In this case, D0 through D5 go to a high impedance state. When the Chip select is inactive, D0 through D7 go to a high impedance state.</td><td>8</td></tr>
<tr><td>A0</td><td>I</td><td>Normally, the least significant bit MPU address bus is connected to distinguish between data and command.
A0 = HIGH : indicates that D0 to D7 are display data or command parameters.
A0 = LOW : indicates that D0 to D7 are control commands.</td><td>1</td></tr>
<tr><td>$\overline{RES}$</td><td>I</td><td>When the $\overline{RES}$ is LOW, initialization is achieved.
Resetting operation is done on the level of the RES signal.</td><td>1</td></tr>
<tr><td>$\overline{CS1}$
CS2</td><td>I</td><td>A chip select signal. When $\overline{CS1}$ = LOW and CS2 = HIGH, signals are active, and data/command input/output are enabled.</td><td>2</td></tr>
<tr><td>$\overline{RD}$
(E)</td><td>I</td><td>• When the 80 series MPU is connected.
A pin for connection of the $\overline{RD}$ signal of the 80 series MPU. When this signal is LOW, the data bus of the S1D15E06 series is in the output state.
• When the 68 series MPU is connected.
Serves as a 68 series MPU enable clock input pin.</td><td>1</td></tr>
<tr><td>$\overline{WR}$
(R/$\overline{W}$)</td><td>I</td><td>• When the 80 series MPU is connected.
A pin for connection of the $\overline{WR}$ signal of the 80 series MPU. Signals on the data bus are latched at the leading edge of the $\overline{WR}$ signal.
• Serves as a read/write control signal input pin when the 68 series MPU is connected.
R/$\overline{W}$ = HIGH : Read
R/$\overline{W}$ = LOW : Write</td><td>1</td></tr>
<tr><td>C86</td><td>I</td><td>A MPU interface switching pin.
C86 = HIGH : 68 series MPU interface
C86 = LOW : 80 series MPU interface</td><td>1</td></tr>
<tr><td>P/S</td><td>I</td><td>Parallel data input/serial data input select pin
P/S = HIGH : Parallel data input
P/S = LOW : Serial data input
The following Table shows the summary:
<table>
<tr><th>P/S</th><th>Data/Command</th><th>Data</th><th>Read/Write</th><th>Serial clock</th></tr>
<tr><td>HIGH</td><td>A0</td><td>D0 to D7</td><td>$\overline{RD}$, $\overline{WR}$</td><td></td></tr>
<tr><td>LOW</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
When P/S = LOW, D0 to D5 are high impedance.
D0 to D5 can be HIGH, LOW or open.
$\overline{RD}$(E) and $\overline{WR}$(R/$\overline{W}$) are locked to HIGH or LOW.
The serial data input does not allow the RAM display data to be read.</td><td>1</td></tr>
</table>

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th><th>Number of pins</th></tr>
<tr><td>CLS</td><td>I</td><td>A pin used to select Enable/Disable state of the built-in oscillator circuit for display clock.
CLS = HIGH : Built-in oscillator circuit Enabled
CLS = LOW : Built-in oscillator circuit Disabled (External input)
When CLS is LOW, display clock is input from the CL pin. When the S1D15E06 series is used in the master/slave mode, each CLS pins must be set to the same level.
<table><tr><th>Display clock</th><th>Master</th><th>Slave</th></tr><tr><td>Built-in oscillator circuit used</td><td>HIGH</td><td>HIGH</td></tr><tr><td>External input</td><td>LOW</td><td>LOW</td></tr></table></td><td>1</td></tr>
<tr><td>M/S</td><td>I</td><td>A pin used to select the master/slave operation for S1D15E06 series. Liquid crystal display system is synchronized when the master operation outputs the timing signal required for liquid crystal display, while the slave operation inputs the timing signal required for liquid crystal display.
M/S = HIGH : Master operation
M/S = LOW : Slave operation
The following Table shows the relation in conformance to the M/S and CLS:
<table><tr><th>M/S</th><th>CLS</th><th>Oscillation circuit</th><th>Power circuit</th><th>CL</th><th>FR, $\overline{\text{DOF}}$, F1, F2, CA</th></tr><tr><td>HIGH</td><td>HIGH
LOW</td><td>Enabled
Disabled</td><td>Enabled
Enabled</td><td>Output
Input</td><td>Output
Output</td></tr><tr><td>LOW</td><td>HIGH
LOW</td><td>Disabled
Disabled</td><td>Disabled
Disabled</td><td>Input
Input</td><td>Input
Input</td></tr></table>The slave power supply circuit can also operate, but do not use it.</td><td>1</td></tr>
<tr><td>CL</td><td>I/O</td><td>Display clock input/output pin.
The following Table shows the relation in conformance to the M/S and CLS state:
<table><tr><th>M/S</th><th>CLS</th><th>CL</th></tr><tr><td>HIGH</td><td>HIGH
LOW</td><td>Output
Input</td></tr><tr><td>LOW</td><td>HIGH
LOW</td><td>Input
Input</td></tr></table>When you want to use the S1D15E06 series in the master/slave mode, connect each CL pin.</td><td>1</td></tr>
<tr><td>FR</td><td>I/O</td><td>A liquid crystal alternating current input/output pin.
M/S = HIGH : Output
M/S = LOW : Input
When you want to use the S1D15E06 series in the master/slave mode, connect each FR pin.</td><td>1</td></tr>
<tr><td>F1, F2, CA</td><td>I/O</td><td>A liquid crystal sync signal input/output pin.
M/S = HIGH : Output
M/S = LOW : Input
When you want to use the S1D15E06 series in the master/slave mode, connect each F1, F2 and CA pins.</td><td>3
(1 each)</td></tr>
<tr><td>$\overline{\text{DOF}}$</td><td>I/O</td><td>A liquid crystal blanking control pin.
M/S = HIGH : Output
M/S = LOW : Input
When you want to use the S1D15E06 series in the master/slave mode, connect each $\overline{\text{DOF}}$ pin.</td><td>1</td></tr>
</table>

5.4 Liquid crystal drive pin

Pin name	I/O	Description	Number of pins
SEG0 to SEG159	O	Liquid crystal segment drive output pins. One of the V_2, V_1, V_C, MV_1, and MV_2 levels is selected by a combination of the display RAM content and FR/F1/F2 signals.	160
COM0 to COM131	O	Liquid crystal common drive output pins. One of the V_3, V_C, MV_3 (V_{SS}) levels is selected by a combination of the scan data and FR/F1/F2 signals.	132

5.5 Test pins

Pin name	I/O	Description	Number of pins
TEST, TEST2 to 5	I	IC chip test pins. Lock them to LOW.	5
TEST0, 1, 6 to 18	I/O	IC chip test pins. Open them and make sure that the capacity is not consumed by wiring, etc.	15

6. FUNCTIONAL DESCRIPTION

6.1 MPU Interface

6.1.1 Selection of Interface Type

S1D15E06 series allows data to be sent via the 8-bit bi-directional data buses (D7 to D0) or serial data input (SI). By setting the polarity of the P/S pin to HIGH or LOW, you can select either 8-bit parallel data input or serial data input, as shown in Table 6.1.

Table 6.1

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
HIGH : Parallel input	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	C86	D7	D6	D5 to D0
LOW : Serial input	$\overline{CS1}$	CS2	A0	—	—	—	SI	SCL	(HZ)

—: Fixed to HIGH or LOW HZ: High impedance state

6.1.2 parallel interface

When the parallel interface is selected (P/S = HIGH), direction connection to the MPU bus of either 80 series MPU or 68 series MPU is performed by setting the 86 pin to either HIGH or LOW, as shown in Table 6.2.

Table 6.2

P/S	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0
HIGH : 68 series MPU bus	$\overline{CS1}$	CS2	A0	E	R/$\overline{W}$	D7 to D0
LOW : 80 series MPU bus	$\overline{CS1}$	CS2	A0	$\overline{RD}$	$\overline{WR}$	D7 to D0

The data bus signals are identified by a combination of A0, $\overline{RD}$ (E), and $\overline{WR}$ (R/$\overline{W}$) signals as shown in Table 6.3.

Table 6.3

Common	68 series	80 series		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Display data read, status read
1	0	1	0	Display data write, command parameter write
0	1	1	0	Command write

6.1.3 Serial interface

When the serial interface is selected (P/S =LOW), the chip is active ($\overline{CS1}$ = LOW, CS2 = HIGH), and reception of serial data input (SI) and serial clock input (SCL) is enabled. Serial interface comprises a 8-bit shift register and 3-bit counter. The serial data are latched by the rising edge of serial clock signals in the order of D7, D6, ... and D0 starting from the serial data input pin. On the rising edge of 8th serial clock signal, they are converted into 8-bit parallel data to be processed.

Whether serial data input is a display data or command is identified by A0 input. A0 = HIGH indicates display data, while A0 = LOW shows command data. The A0 input is read and identified at every 8 × n-th rising edge of the serial clock after the chip has turned active.

Fig. 6.1 shows the serial interface signal chart.

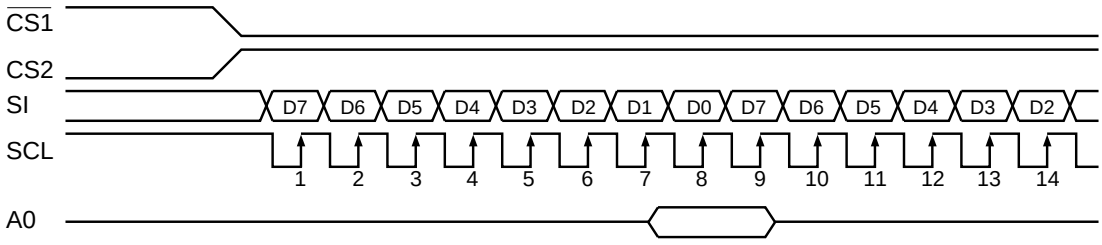


Fig. 6.1

* When the chip is inactive, the counter is reset to the initials state.
* Reading is not performed in the case of serial interface.
* For the SCL signal, a sufficient care must be taken against terminal reflection of the wiring and external noise. Recommend to use an actual equipment to verify the operation.

6.1.4 Chip Selection

The S1D15E06 series has two chip select pins; $\overline{CS1}$ and CS2. MPU interface or serial interface is enabled only when $\overline{CS1}$ = LOW and CS2 = HIGH.
When the chip select pin is inactive, D0 to D5 are in the state of high impedance, while A0, $\overline{RD}$ and $\overline{WR}$ inputs are disabled. When serial interface is selected, the shift register and counter are reset.

6.1.5 Access to display data RAM and internal register

Access to S1D15E06 series viewed from the MPU side is enabled only if the cycle time requirements are kept. This does not required waiting time; hence, high-speed data transfer is allowed.
Furthermore, at the time of data transfer with the MPU, S1D15E06 series provides a kind of inter-LSI pipe line processing via the bus holder accompanying the internal data bus.
For example, when data is written to the display data RAM by the MPU, the data is once held by the bus holder. It is written to the display data RAM before the next data write cycle comes.
On the other hand, when the MPU reads the content of the display data RAM, it is read in the first data read cycle (dummy), and the data is held in the bus holder. Then it is read onto on the system bus from the bus holder in the next data read cycle. Restrictions are imposed on the display data RAM read sequence. When the address has been set, specified address data is not output to the Read command immediately after that. The specified address data is output in the second data reading. This must be carefully noted. Therefore, one dummy read operation is mandatory subsequent to address setting or write cycle. Fig. 6.2 illustrates this relationship.

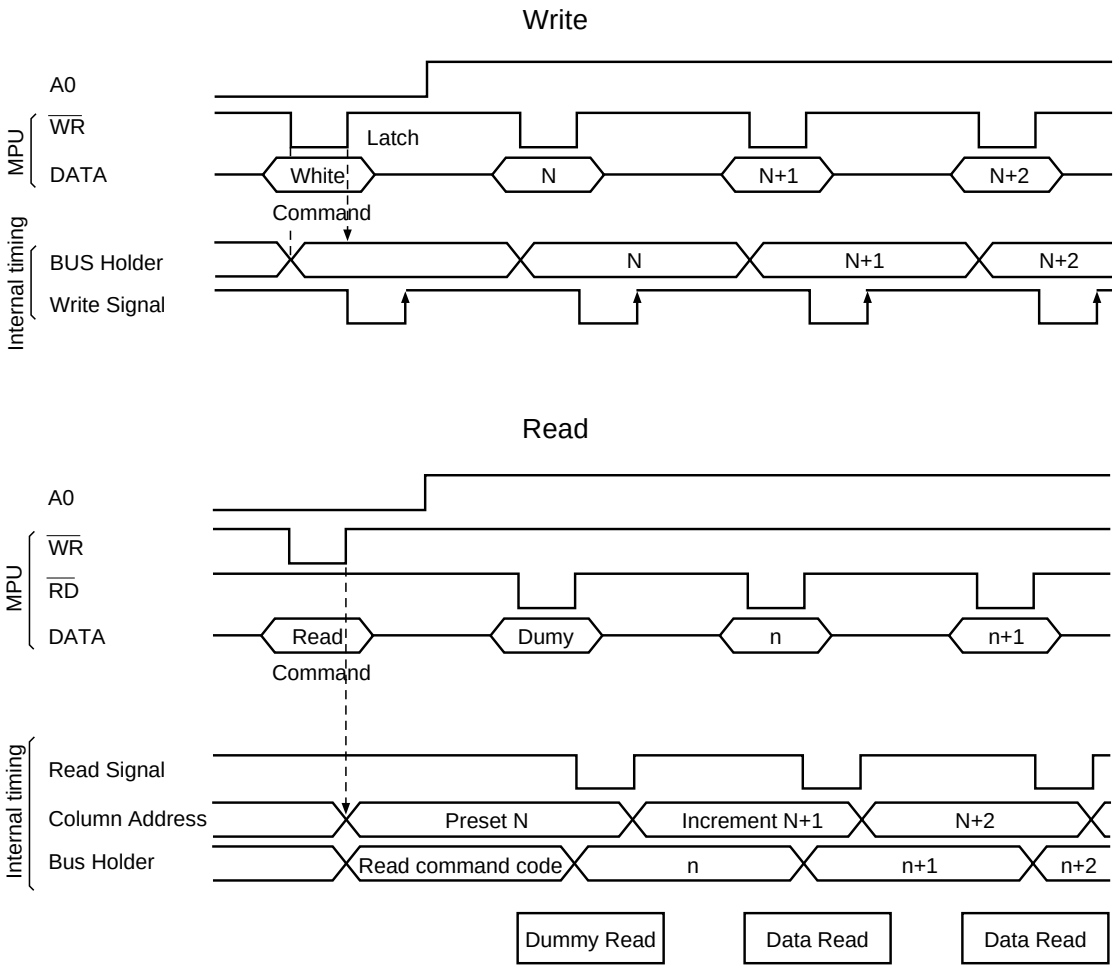


Fig. 6.2

6.2 Display data RAM

6.2.1 Display Data RAM

This is a RAM to store the display dot data, and comprises $132 \times 160 \times 2$ bits. Access to the desired bit is enabled by specifying the page address and column address. When the 4 gray-scale is selected by the Display Mode command, display data input for gray-scale display are processed as a two-bit pair. Combination is as follows:

(MSB, LSB) = (D1,D0), (D3,D2), (DS,D4), (D7,D6)

When the RAM bit data is gray-scale 1 and 2, gray-scale display is realized according to the parameter of the Gray-scale Pattern Set command.

RAM bit data (high order and low order)

(1,1) : gray-scale 3	Black (when display is in normal mode)
(1,0) : gray-scale 2	
(0,1) : gray-scale 1	
(0,0) : gray-scale 0	White (when display is in normal mode)

When binary display is selected by the Display Mode command, the RAM 1 bit built in the one-dot pixel responds to it. When the RAM bit data is “1”, the display is black. If it is “0”, the display is given in white.

RAM bit data

“1” : Light On	Black (when display is in normal mode)
“0” : Light Off	White (when display is in normal mode)

Display data D7 to D0 from the MPU correspond to LCD common direction, as shown in Fig. 6.3 and 6.4. Therefore, less restrictions when multi-chip usage. Furthermore, read/write operations from the MPU to the RAM are carried out via the input/output buffer.

The read operation from Display data RAM is designed as an independent operation. Accordingly, even if the MPU accesses the RAM asynchronously during LCD display, no adverse effect is given to display.

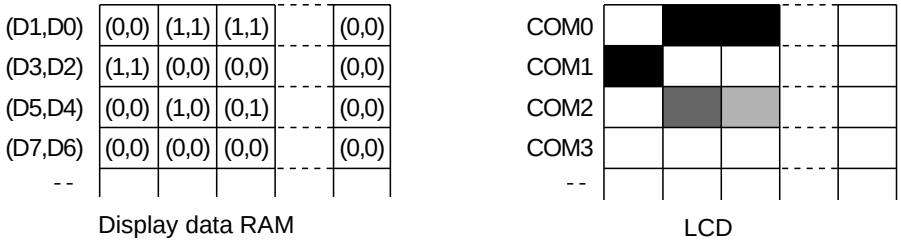


Fig. 6.3 4 gray-scale

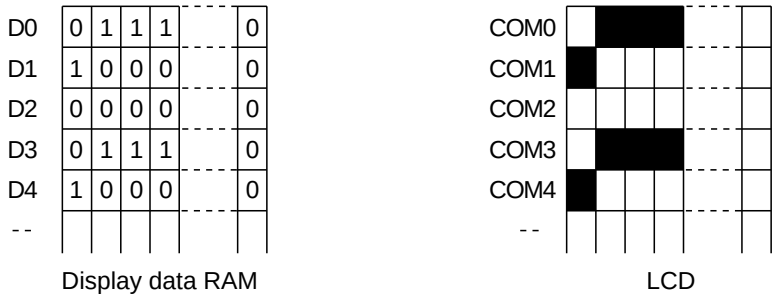


Fig. 6.4 Binary

6.2.2 Gray-scale display

When the 4 gray-scale is selected by the Display Mode command, gray-scale is represented by the FRM control carried out according to the gray-scale data written in the display data RAM.

Of the 4 gray-scale, 2 gray-scale of halftones (gray-scale 2 and 1) has its level of contrast specified by the Gray-scale Set command. Gray-scale can be selected from 6 levels of contrast.

6.2.3 Page address circuit/column address circuit

The address of the display data RAM to be accessed is specified by the Page Address Set command and Column Address Set command, as shown in Fig. 6.5 and Fig. 6.6. For Address incremental direction, either the column direction or page direction can be selected by the Address Direction command. Whichever direction is chosen, increment is carried out by positive one (+1) after write or read operation.

When the column direction is selected for address increment, the column address is increased by +1 for every write or read operation. After the column address has accessed up to 9FH, the page address is incremented by +1 and the column address shifts to 0H.

When the page direction is selected for address increment, the page address is increased with the column address locked in position. When the page address has accessed up to 32H, the column address is incremented by +1, and the page address goes to 0H.

Whichever direction is selected for address increment, the page address goes back to 0H and the column address to 0H after access up to the column address 9FH of page address 32H.

As shown in Fig. 6.4, relationship between the display data RAM column address and segment output can be reversed by the Column Address Set Direction command. This will reduce restrictions on IC layout during LCD module assembling.

Table 6.4

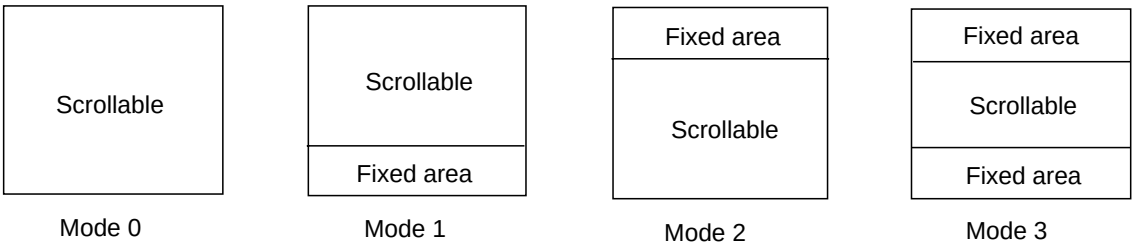
SEG output		SEG0		SEG159
ADC	"0"	0(H)→	Column Address	→9F(H)
(D0)	"1"	9F(H)←	Column Address	←0(H)

6.2.4 Line address circuit

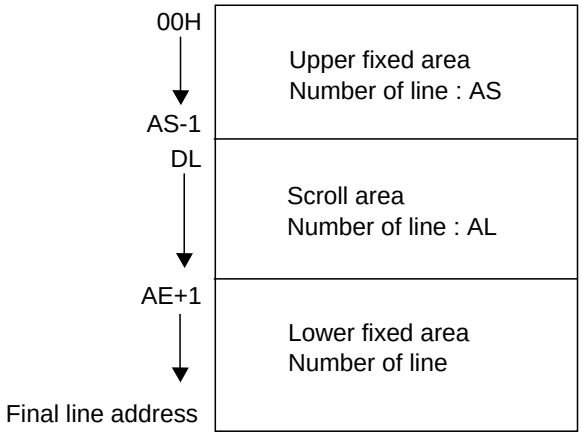
The line address circuit specifies the line address corresponding to COM output when the contents of the display data RAM is displayed, as shown in Fig. 6.5 and 6.6. Normally, the top line of the display (COM0 output in the case of normal rotation of the common output status and COM131 output in the case of reverse rotation) is specified by the Display Start Line Address Set command. The display area starts from the specified display start line address to cover the area corresponding to the lines specified by the DUTY Set command in the direction where the line address increments.
If the display start line address set command is used for dynamic modification of the line address, screen scroll and page change are enabled.

6.2.5 Area scroll

The display area can be divided into the display area fixed in the COM direction and scrollable area by the area scroll command. The scroll area is set by a scroll mode, scroll start line address (AS), scroll end address (AE), and scroll display line count (AL) as parameters for the area scroll command. Display start line address (DL) in the scroll area can be specified by the display start line address set command.



Scroll mode



6.2.5.1 Mode 0 (full screen scroll)

This mode releases the area scroll. Parameters AS, AE and AL are disabled,

6.2.5.2 Mode 1 (Upper scroll)

Reading starts from the line address DL to read AL lines as a scroll area. If the line address AE is read in the middle of reading the scroll area, the line address to be read next will be 00H. When all the AL lines have been read, the address to be read next will be AE + 1. When reading is completed up to the final line address, the control goes back to the line address DL, and parameter AS is disabled. DL can be specified in the range from 00H to AE.

6.2.5.3 Mode 2 (lower scroll)

Reading starts from line address 00H to reach the line address AS-1 in the continuous reading mode. Upon completion of reading of line address AS-1, the line address moves to the DL to read the area corresponding to AL lines from the line address DL as a scroll area. If the final line address is read in the middle of reading the scroll area, the line address to be read next will be AS. When all AL lines have been read, the control goes back to the line address 00H, and parameter AE is disabled. DL can be specified in the range from AS to the final line address.

6.2.5.4 Mode 3 (Center scroll)

Reading starts from line address 00H to reach the line address AS-1 in the continuous reading mode.
Upon completion of reading of line address AS-1, the line address moves to the DL to read the area corresponding to AL lines from the line address DL as a scroll area. If the final line address is read in the middle of reading the scroll area, the line address to be read next will be AS. When all AL lines have been read, the line address will be AE+1. When up to the final line address has been read, the control goes back to the line address 00H, DL can be specified in the range from AS to AE.

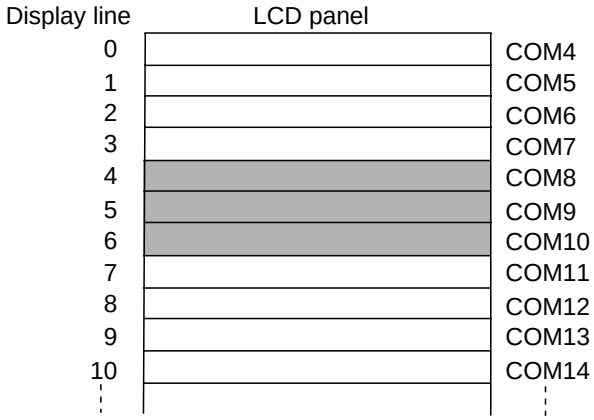
6.2.6 Display data latch circuit

The display data latch circuit is a latch to temporarily latch the display data output from then display data RAM to the liquid crystal drive circuit. Display normal/reverse, display ON/OFF, and display all lighting ON/OFF commands control the data in this latch, without the data in the display data RAM being controlled.

6.2.7 Partial display

Partial display of the screen is provided by the partial display ON/OFF command. The partial area (display start line, number of display lines) are set by the partial display set command.
The display start line of the parameter shows the line assigned in the COM direction of the liquid crystal screen. It is different from the line address given in Fig. 6.5 and 6.6.

Example: When the point is set at 1 (COM4 to 7) by the Duty Reset command, the display line is assigned as shown below. If the display start line 4 and display line count 3 are specified by the partial display set command, the display area is COM8 to COM10.



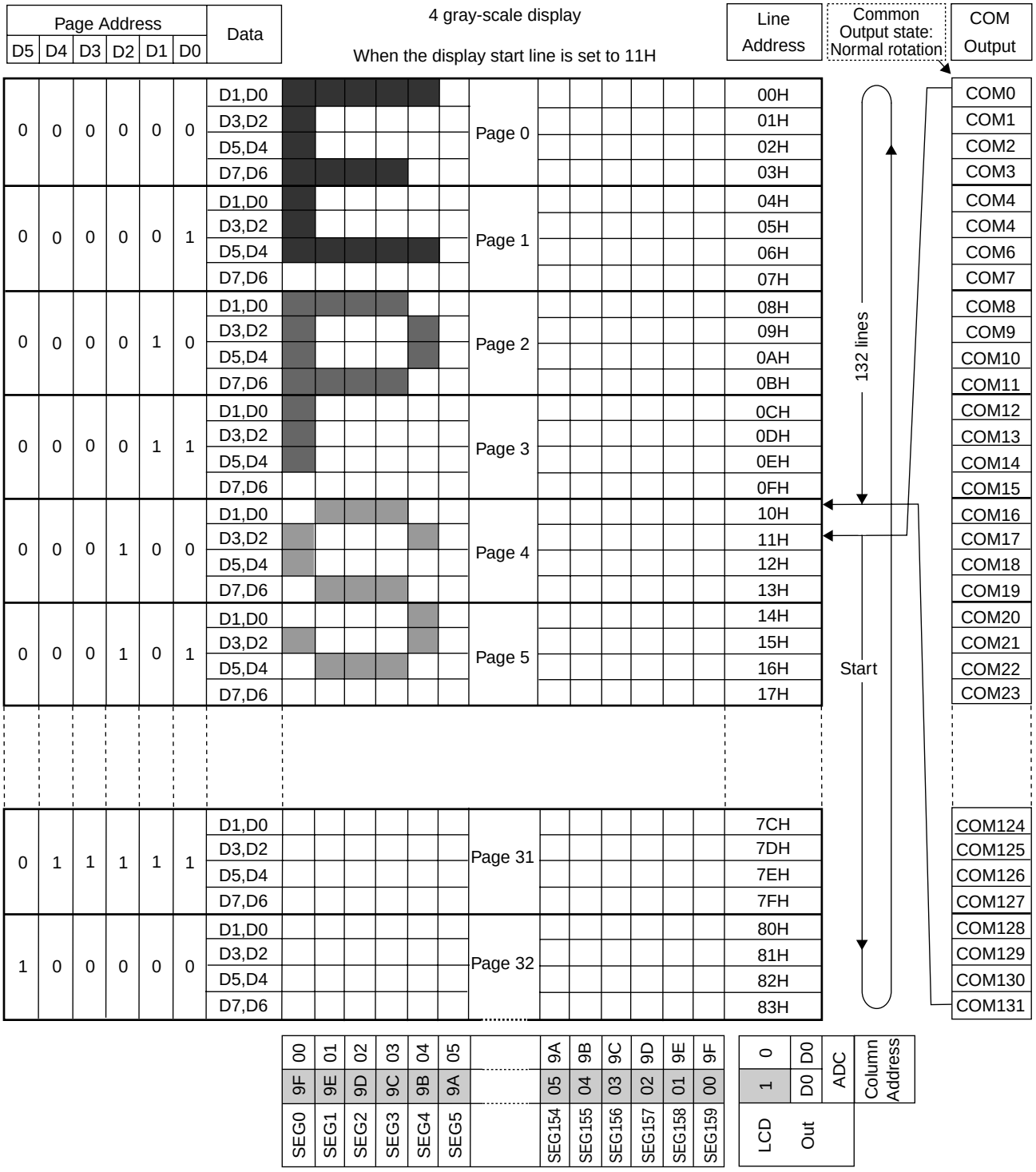


Fig. 6.5 4 gray-scale

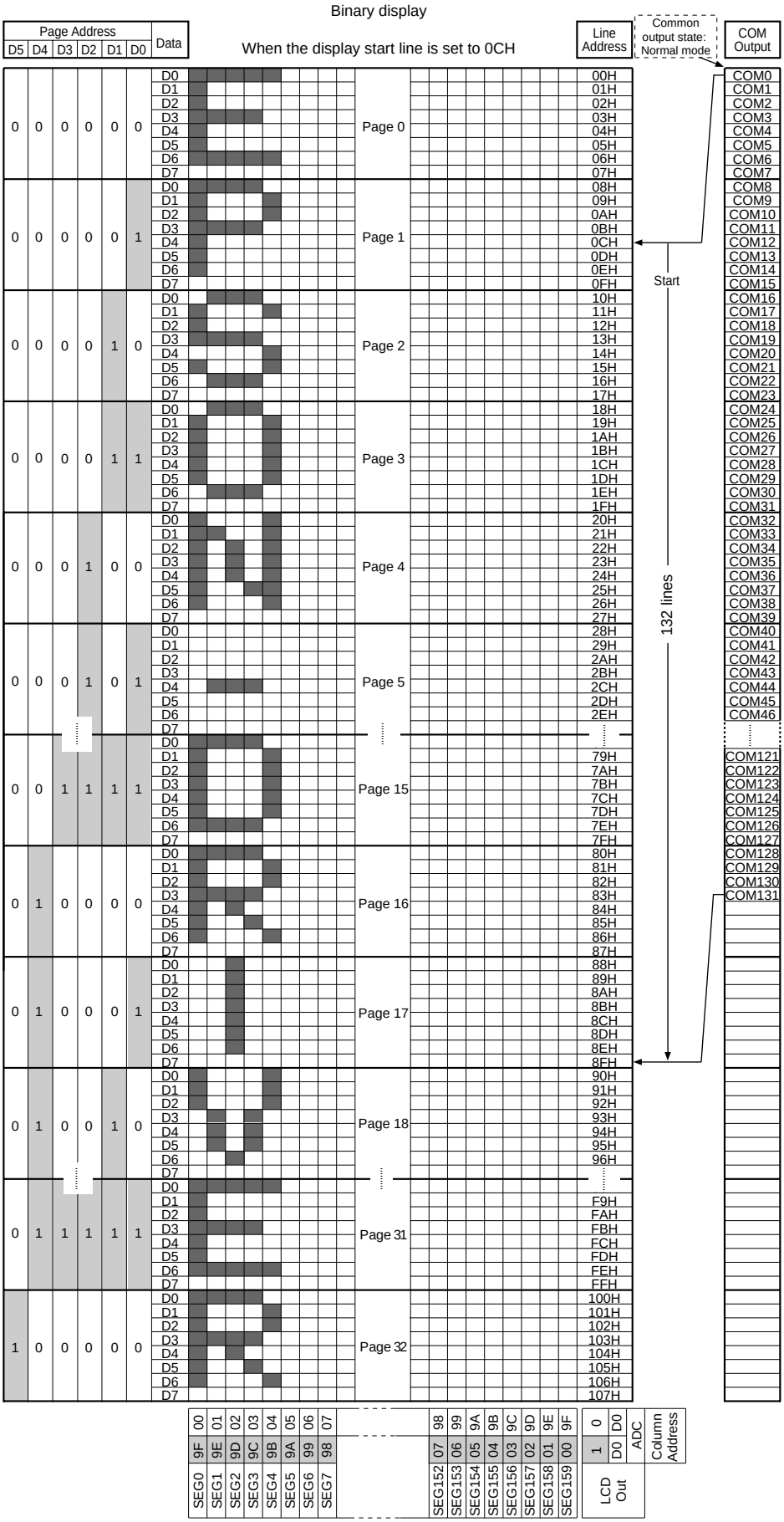


Fig. 6.6 Binary display

6.3 Oscillator circuit

A display clock is generated by the CR oscillator. The oscillator circuit is enabled only when M/S = HIGH and CLS = HIGH. Oscillation starts after input of the built-in oscillator circuit ON command input.
When CLS = LOW, oscillation stops, and display clock is input from the CL pin.

6.4 Display timing generation circuit

Timing signals are generated from the display clock to the line address circuit and display data latch circuit. Synchronized with display clock, display data is latched in display data latch circuit, and is output to the segment drive output pin. Reading of the display data into the LCD drive circuit is completely independent of access from the MPU to the display data RAM. Accordingly, asynchronous access to the display data RAM during LCD display does not give any adverse effect; like as flicker.
Furthermore, the display clock generates internal common timing, liquid crystal alternating signal(FR), field start signal (CA) and drive pattern signal (Fl and F2).
The FR normally generates 2-frame alternating drive system drive waveform to the liquid crystal drive circuit. The n-line reverse alternating drive waveform is generated for each $4 \times (a+1)$ line by setting data on the n-line reverse drive register. When there is a display quality problem including crosstalk,the problem may be solved using the n-line reverse alternating drive.
Execute liquid crystal display to determine the number of lines “n” for alternation.
When you want to use the S1D15E06 series in multi-chip configuration, supply display timing signal (FR, CA, F1, F2, CL, $\overline{DOF}$) to the slave side from the master side. Table 6.5 shows the statuses of FR, CA, F1, F2, CL, $\overline{DOF}$.

Table 6.5

Operating mode		CL	FR, CA, F1, F2, $\overline{DOF}$
Master (M/S = HIGH)	Built-in oscillator circuit enabled (CLS = HIGH)	Output	Output
	Built-in oscillator circuit disabled (CLS = LOW)	Input	Output
Slave (M/S = LOW)	Built-in oscillator circuit enabled (CLS = HIGH)	Input	Input
	Built-in oscillator circuit disabled (CLS = LOW)	Input	Input

6.5 Liquid crystal drive circuit

6.5.1 SEG Drivers

This is a SEG output circuit. It selects the five values of V_2, V_1, V_C, MV_1 and MV_2 using the driver control signal determined by the decoder, and output them.

6.5.2 COM Drivers

This is a COM output circuit. It selects three values of V_3, V_C and MV_3(V_{SS}) using the driver control signal determined by the decoder, and output them.
S1D15E06 series allows the COM output scanning direction to be set by the common output status select command. (See Table 6.6). This will reduce restrictions on IC layout during LCD module assembling.

Table 6.6

Status	Direction of COM scanning		
Normal	COM 0	→	COM 131
Reverse	COM 131	→	COM 0

6.6 Power supply circuit

This is a power supply circuit to generate voltage required for liquid crystal drive, and is characterized by a low power consumption. It consists of a step-up circuit, voltage regulating circuit and liquid crystal drive voltage generating circuit, and is enabled only during master operation. The power supply circuit uses the power control set command to provide an on/off control of step-up circuit, voltage regulating circuit and liquid crystal drive potential generating circuit. This allows a combined use of the external power supply and part of built-in power supply functions. Table 6.7 shows functions controlled by the 5-bit data of the control set command, and Table 6.8 shows reference combinations. The power supply circuit is enabled only during master operation.

Table 6.7 Control by 5-bit data of the control set command

Item	State		Triple	Double	Single
	"1"	"0"			
D4 Step-cut circuit scaling factor select bit 1	–	–	1	1	0
D3 Step-cut circuit scaling factor select bit 2	–	–	1	0	1
D2 Step-cut circuit control bit	ON	OFF	–	–	–
D1 Voltage regulator circuit (V_C regulator circuit) control bit	ON	OFF	–	–	–
D0 LCD driving potential generating circuit (LCDV circuit) control bit	ON	OFF	–	–	–

Table 6.8 Reference combination

Circuits used	D4	D3	D2	D1	D0	Step-up circuit	V_C regulator circuit	LCDV circuit	Eternal input power supply
① Use of all built-in power supplies									
Triple step-up	1	1	1	1	1	○ "1"	○ "1"	○ "1"	–
Double step-up	1	0	1	1	1	○ "1"	○ "1"	○ "1"	–
$V_{OUT} = V_{DD}$	0	1	1	1	1	○ "1"	○ "1"	○ "1"	–
② V_C regulating circuit and LCDV circuit only	0	0	0	1	1	× "0"	○ "1"	○ "1"	V_{OUT}
③ LCDV circuit only	0	0	0	0	1	× "0"	× "0"	○ "1"	V_C
④ External power supply only (S1D15E06D00B*)	0	0	0	0	0	× "0"	× "0"	× "0"	V_3, V_2, V_1, V_C, MV_1, MV_2

* Any combinations other than the above are not available.

*100ms or more should be kept from V_C regulator circuit ON to LCDV circuit ON.

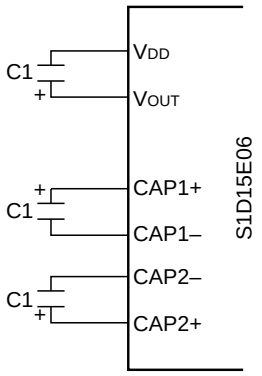
6.6.1 Step-up circuit

VDD-VSS potential can be triple and double step-up by the step-up circuit built in the S1D15E06 series. The status of VOUT = VDD can be selected by stopping the operation of the triple and double step-up circuit using the command

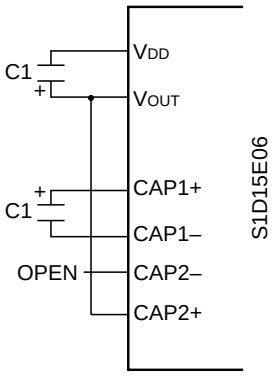
① When used by switching between the triple, double step-up and VOUT = VDD using a command:
Capacitors C1 are connected between CAP1+ <-> CAP1, between CAP2+ <-> CAP2 and between VDD <-> VOUT for use.

② When used by switching between the double step-up and VOUT = VDD using a command:
Capacitors C1 are connected between CAP1+ <-> CAP1 and between VDD <-> VOUT for use.

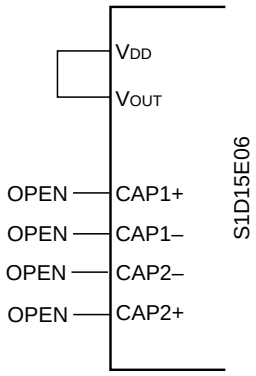
③ Only VOUT = VDD is used.
VDD pin and VOUT pin are connected for use.



① Triple, double step-up or VOUT = VDD

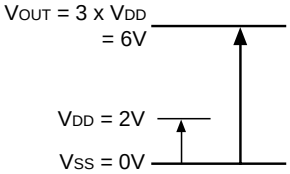


② Double step-up or VOUT = VDD

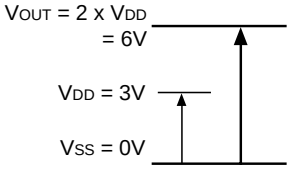


③ VOUT = VDD (without step-up)

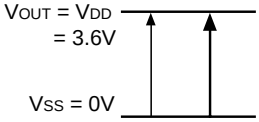
Fig.6.7 shows the potential relationship for boosting.



Triple step-up potential relationship



Double step-up potential relationship



VOUT = VDD potential relationship

Fig. 6.7

* Set the VDD voltage range so that the VOUT pin voltage does not exceed the absolute maximum rating.

6.6.2 Voltage Regulating Circuit

VOUT generated from the step-up circuit or VOUT input from the outside produces liquid crystal drive voltage VC via the voltage regulating circuit. The voltage regulating circuit is controlled by liquid crystal drive voltage change command and electronic volume.
The S1D15E06 series has a high precision constant voltage source, and incorporates 4-step liquid crystal drive voltage change command and 128-step electronic volume functions. This makes it possible to provide a high precision liquid crystal drive voltage regulation only by the command without adding any external parts. The variable range of the VC voltage is from about 1.6 to 7.0 [V]. When the internal step-up is used, or VOUT is input for use, the VOUT potential should be, in principle, the voltage 20% or more higher than the maximum voltage of the VC to be used, giving consideration to temperature characteristics.

Example: When VC output is 7 [V], VOUT ≥ 8.4 [V] (three times 2.8 [V], etc.)
When VC output is 4 [V], VOUT ≥ 4.8 [V] (two times 2.4 [V], three times 1.8 [V])

• Electronic volume

α of Table 6.9 indicates an electronic volume command value. It takes one of 128 states when the data is set in the 7-bit electronic volume register.
Table 6.9 shows the value of α by setting the data in the electronic volume register.

Table 6.9

D6	D5	D4	D3	D2	D1	D0	α	Voltage VC
0	0	0	0	0	0	0	0	Small
0	0	0	0	0	0	1	1	↑
0	0	0	0	0	1	0	2	↑
								↑
								↑
1	1	1	1	1	0	1	125	↑
1	1	1	1	1	1	0	126	↓
1	1	1	1	1	1	1	127	Large

• Liquid crystal drive voltage selection

The liquid drive voltage range can be selected from 3 states by the liquid crystal drive voltage select command using the two-bit crystal drive voltage select command register.

Table 6.10

D1	D0	VC voltage output range
0	0	1.77V to 3.50V
1	0	2.53V to 5.00V
1	1	3.54V to 7.00V

Equation A-1 represents V_C logical values. For the output voltage of V_C, a manufacturing dispersion of up to ± 3% should be taken into account.

Equation A-1

Unit [V]

Electronic	**LCD voltage selection**					
V_R	D1	D0	D1	D0	D1	D0
α	0	0	1	0	1	1
	V_C (Max.) = 3.50V		V_C (Max.) = 5.00V		V_C (Max.) = 7.00V	
0 to 31	1.77 + 0.0195 × α		2.53 + 0.028 × α		3.54 + 0.039 × α	
32 to 63	2.39 + 0.0156 × (α–32)		3.42 + 0.0223 × (α–32)		4.78 + 0.0313 × (α–32)	
64 to 95	2.89 + 0.0117 × (α–64)		4.12 + 0.0167 × (α–64)		5.77 + 0.0234 × (α–64)	
96 to 127	3.26 + 0.0078 × (α–96)		4.65 + 0.0112 × (α–96)		6.52 + 0.0156 × (α–96)	

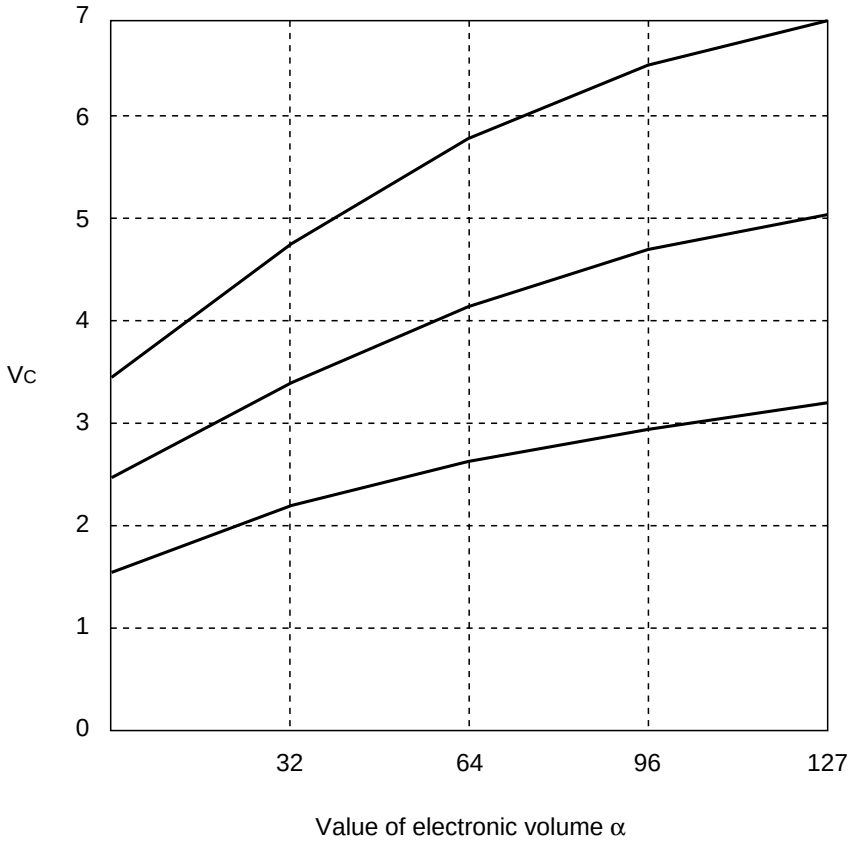


Figure 6.8

6.6.3 Liquid crystal drive voltage generation circuit

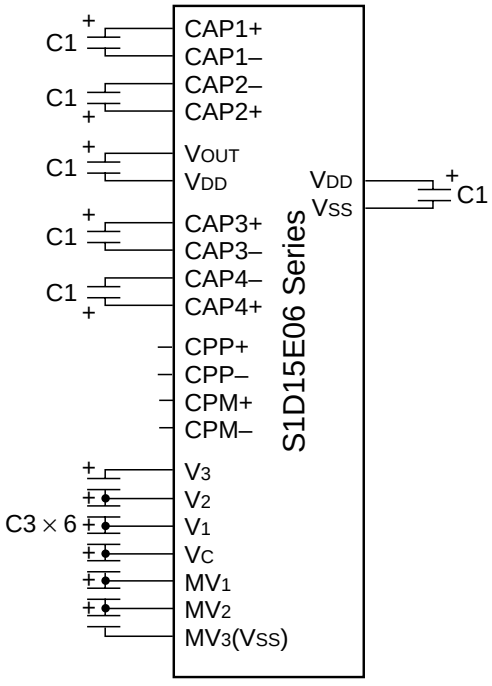
Voltage V_C is boosting in the IC to generate potential V_3. Furthermore, voltages V_3 and V_C are converted by resistive divider to produce V_2, V_1, MV_1 and MV_2 voltages. V_2, V_2, MV_1 and MV_2 voltages are impedance-converted by the voltage follower, and is supplied to the liquid crystal drive circuit.

V_2	11/14 • V_3
V_1	9/14 • V_3
V_C	7/14 • V_3
MV_1	5/14 • V_3
MV_2	3/14 • V_3

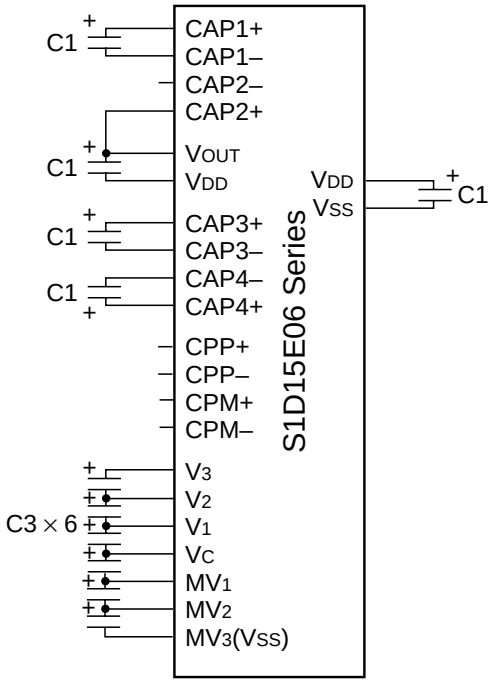
An example of circuit around the power supply circuit

① Use of all built-in power supplies

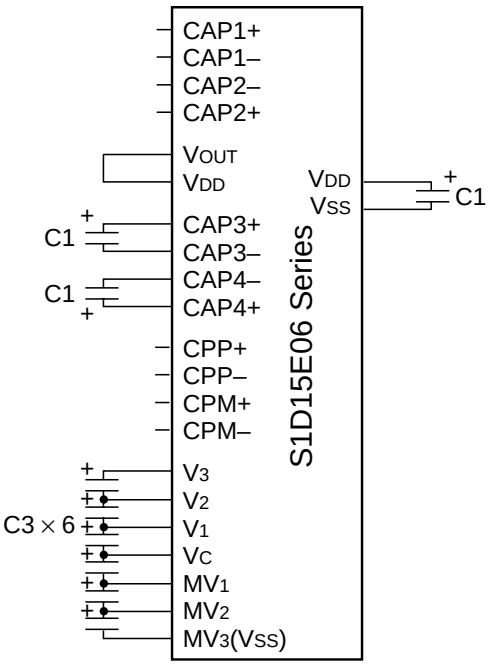
When used by switching between the triple, double boosting and $V_{OUT} = V_{DD}$: (12 C's)



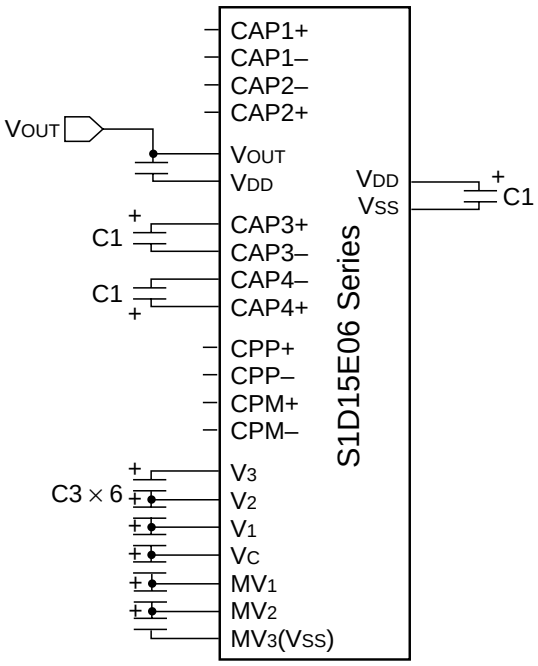
When used by switching between the double boosting and $V_{OUT} = V_{DD}$: (11 C's)



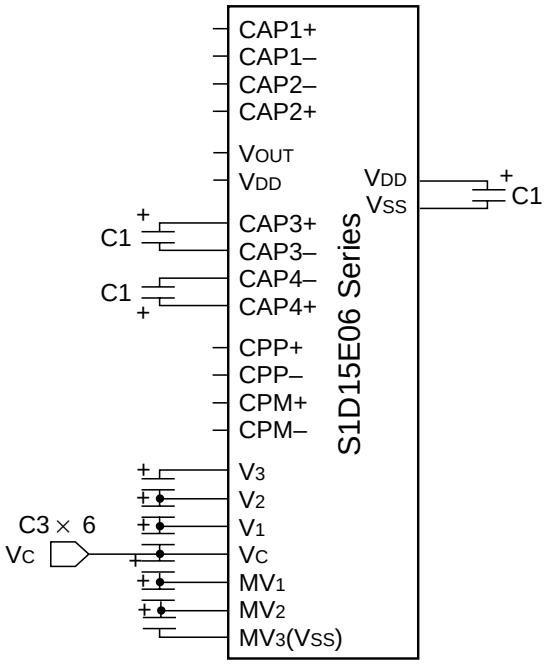
Only V_{OUT} = V_{DD} is used: (9 C's)



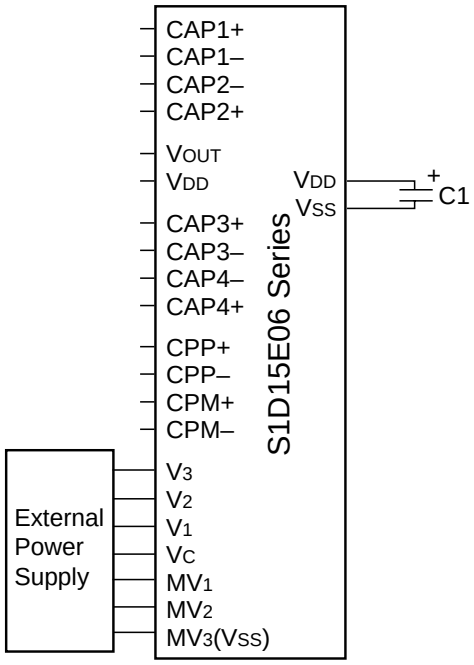
② V_C regulating circuit and LCDV circuit
V_{OUT} external input (10 C's)



③ LCDV circuit only
V_C external input (9 C's)



④ External power supply only
external input (1 C)



Examples of common reference settings

Item	Settings	Unit
C1	1.0 to 4.7	µF
C2	0.47 to 1.0	
C3	0.47 to 1.0	

*5 Precautions when installing the COG
When installing the COG, it is necessary to duly consider the fact that there exists a resistance of the ITO wiring occurring between the driver chip and the externally connected parts (such as capacitors and resistors). By the influence of this resistance, non-conformity may occur with the indications on the liquid crystal display. When installing the COG, we recommend to use the "④ External power supply only"

6.6.4 Temperature gradient select circuit

This is a circuit to select the temperature gradient characteristics of the liquid crystal drive power supply voltage. Temperature gradient characteristics can be selected from eight states by the Temperature Gradient command. Selection of temperature gradient characteristics conforming to the temperature characteristics of the liquid crystal to be used makes it possible to configure a system without providing an external element for temperature characteristics compensation.

6.7 Reset circuit

When the $\overline{RES}$ input becomes LOW, this LSI is set to the initialized state.
The following shows the initially set state:

1. Display : OFF
2. Display OFF mode : V_{SS} output
3. Display : normal mode
4. Display all lighting : OFF
5. Common output status : normal
6. Display start line : Set to 1st line
7. Page address : Set to 0 page
8. Column address : Set to 0 address
9. Display data input direction : Column direction
10. Column address direction : forward
11. n-line a.c. reverse drive : OFF (reverse drive for each frame)
12. n-line reverse drive register : (D4, D3, D2, D1, D0) = (0, 1, 1, 0, 0)
13. Display mode : 4 gray-scale display
14. Gray-scale pattern register : (D7, D6, D5, D4, D3, D2, D1, D0) = (∗, 1, 0, 1, ∗, 0, 1, 0)
15. Area scroll :
    Scroll mode : (D1, D0) = (0, 0)
    Scroll start address : (D7, D6, D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0, 0, 0)
    Scroll terminating address : (D7, D6, D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0, 0, 0)
    Number of display lines : (D7, D6, D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0, 0, 0)
16. DUTY register : (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0) (1/132 duty)
    Start spot (block) register : (D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0) (COM0)
17. Partial display : OFF
18. Partial display start line : (D7, D6, D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0, 0, 0)
    Number of partial display lines : (D7, D6, D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0, 0, 0)
19. Read modify write : OFF
20. Built-in oscillation circuit : stop
21. Oscillation frequency register : (D3, D2, D1,D0) = (0, 0, 0, 0) (120 kHz)
22. Power control register : (D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0)
23. Clock frequency for step-up/step-down
    Step-up : (D2, D1, D0) = (1, 0, 1)
    Step-down : (D6, D5, D4) = (1, 0, 1)
24. Liquid crystal drive voltage selection register : (D1,D0) = (0, 0)
25. Electronic volume register : (D6, D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0, 0, 0)
26. Discharge : ON (only for when $\overline{RES}$ = LOW)
27. Power save : OFF
28. Temperature gradient resistor : (D2, D1, D0) = (0, 0, 0) (–0.06/°C)
29. Register data in the serial interface : Clear

When the Reset command is used, only the above-mentioned inilialized items 7, 8 and 19 are executed.

When power is turned on, initialization by the $\overline{RES}$ pin is necessary. After initialization by the $\overline{RES}$ pin, each input pin must be controlled correctly.
Furthermore, when control signals from the MPU have a high impedance, the excessive current may flow to the IC.
After V_{DD} is applied, measures should be taken to ensure that the input pin does not have a high impedance. The S1D15E06 series discharges the electric charge of V_{OUT} and liquid crystal drive voltage (V_3, V_2, V_1, V_C, MV_1, MV_2) at the level of $\overline{RES}$ pin = LOW. When liquid crystal drive external power supply is used, external power supply should not be supplied during the period of $\overline{RES}$ = LOW to prevent external power supply and V_{DD} from being short circuited.

The optimum values for above-mentioned Cl, C2 and C3 vary according to the LCD panel to drive. Use the above-mentioned values as references. Actually verify the display of a pattern with big load to make a decision.

7. COMMAND

The S1D15E06 series identifies data bus signals by a combination of A0, $\overline{RD}$(E) and $\overline{WR}$(R/$\overline{W}$). Interpretation and execution of the command are executed by the internal timing alone which is independent of the external clock. This allows high-speed processing.
The 80 series MPU interface allows the command to be started by entering the low pulse in the $\overline{RD}$ pin during reading and by entering the low pulse in the $\overline{WR}$ pin during writing.
The 68 series MPU interface allows a read state to occur by entering HIGH in the R/$\overline{W}$ pin, and permits a write state to occur by entering LOW. It also allows the command to be started by entering the high pulse in the pin E. (For timing, see the description of "10. Timing characteristics").

Accordingly, the 68 series MPU interface is different from 80 series MPU interface in that $\overline{RD}$(E) is "1(H)" in the case of display data/read shown in the Command Description and Command Table. The following describes the commands, based on the example of the 80 series MPU interface:
When the serial interface is selected, enter data sequentially starting from D7.

Command Description

(1) Display ON/OFF

This command sets the display ON/OFF.
When display OFF is specified, segment and common drivers outputs the level selected by the display OFF Mode Select command.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Output level
0	1	0	1	0	1	0	1	1	1	0	Display OFF
										1	Display ON

(2) Display OFF Mode Select

This command is used to set the output level of the segment and common driver when the display is off.
In the initial setting state, it becomes "D0 = 0".
* When D0 = 0 is selected in the case of S1D15E06D00B∗, the MV_2 and common driver V_{SS} level is output by segment driver when display is off. Select D0 = 1 to use the S1D15E06D00B∗.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Output level
0	1	0	1	0	1	1	1	1	1	0	V_{SS}
										1	V_C

(3) Display Normal/Reverse

This command allows the display ON/OFF state to be reversed, without having to rewrite the contents of the display data RAM. In this case, contents of the display data RAM are maintained.

A0	E / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	1	0	RAM data = HIGH LCD ON Voltage (normal)
										1	RAM data = LOW LCD ON Voltage (reverse)

(4) Display All Lighting ON/OFF

This command forces all the displays to be turned on independently of the contents of the display data RAM. In this case, the contents of the display data RAM are maintained. Fully white display can also be made by a combination of the Display Reverse command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	1	0	0	Normal display status
										1	Display all lighting

(5) Common Output Status Select

This command allows the scanning direction of the COM output pin to be selected. For details, see the description of "6.5.2 COM Drivers" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Selected state	
0	1	0	1	1	0	0	0	1	0	0	Normal	COM0 → COM131
										1	Reverse	COM131 → COM0

(6) Display Start Line set (Parameter: 1 byte (4 gray-scale) and 2 bytes (binary))

The parameter following this command specifies the display start line address of the display data RAM shown in Fig. 6.5 and 6.6. When the Display Mode command is used to select 4 gray-scale display, a 1-byte parameter must be entered. When the binary display is selected, a 2-byte parameter must be entered.
The display area is indicated in the direction where line address numbers are incremented, starting from the specified line address. If a dynamic change of the line address is made by this command, smooth scrolling in the longitudinal direction and page breaking are enabled. For details, see the description of "6.2.4 Line address circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	0	0	1	0	1	0	Mode setting
1	1	0	P7	P6	P5	P4	P3	P2	P1	P0	Register setting 1
1	1	0	*	*	*	*	*	*	*	P8	Register setting 2 (only binary display required)

*: denote invalid bits.

• Display Start Line Set command parameter

(i) When the display mode is a 4 gray-scale mode:
The one-byte parameter is used to specify the address.

P7	P6	P5	P4	P3	P2	P1	P0	Line address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
0	0	0	0	0	0	1	0	02H
				↓				↓
1	0	0	0	0	0	1	0	82H
1	0	0	0	0	0	1	1	83H

Set to the line address 00H at the time of resetting.

(ii) When the display mode is binary:

To specify the address, continuous 2-byte data is necessary. The first byte D0 is LSB, and the second byte D0 is MLB.

	P7	P6	P5	P4	P3	P2	P1	P0 P8	Line address
1st byte 2nd byte	0 *	0 *	0 *	0 *	0 *	0 *	0 *	0 0	00H
	0 *	0 *	0 *	0 *	0 *	0 *	0 *	1 0	01H
	0 *	0 *	0 *	0 *	0 *	0 *	1 *	0 0	02H
					↓				↓
	0 *	0 *	0 *	0 *	0 *	1 *	1 *	0 1	106H
	0 *	0 *	0 *	0 *	0 *	1 *	1 *	1 1	107H

Set to line address 000H at the time of resetting. *: denote invalid bits.

• Line address setting sequence

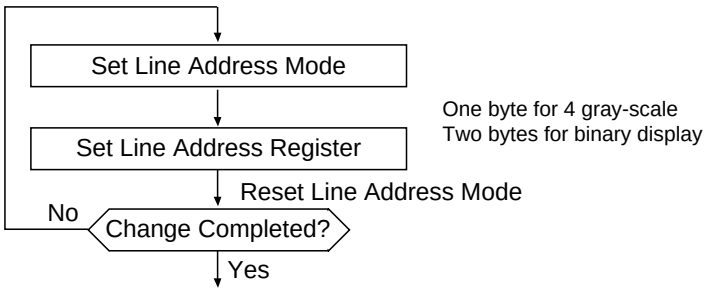


Fig. 7.1

(7) Page Address Set

This command specifies the page address corresponding to row address when MPU access to the display data RAM shown in Fig. 6.5 and 6.6. For details, see the description of "6.2.2 Page address circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Page address
0	1	0	1	0	1	1	0	0	0	1	Command
1	1	0	*	*	P5	P4	P3	P2	P1	P0	Page address setting

*: denote invalid bits.

P5	P4	P3	P2	P1	P0	Page address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
		↓				↓
0	1	1	1	1	1	31
1	0	0	0	0	0	32

(8) Column Address Set

This command sets the display data RAM column address given in Fig. 6.5 and 6.6. For details, see the description of "6.2.3 Column address circuit" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	0	0	1	1
1	1	0	P7	P6	P5	P4	P3	P2	P1	P0

P7	P6	P5	P4	P3	P2	P1	P0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
				↓				↓
1	0	0	0	0	0	1	0	158
1	0	0	1	1	1	1	1	159

(9) Display Data Write

This command allows the 8-bit data to be written to the address specified by the display data RAM. After writing, column address or page address is automatically incremented +1 by the Display Data Input Direction Select command. This enables the MPU to write the display data continuously.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	1	1	0	1
1	1	0	Write Data							

(10) Display Data Read

This command allows the 8-bit data to be read from the address specified by the display data RAM. After reading, column address or page address is automatically incremented +1 by the Display Data Input Direction select command. This enables the MPU to read multiple word data continuously.
It should be noted that one dummy reading is essential immediately after the column address or page address has been set. For details, see the description of "6.1.5 Access to display data RAM and internal register" in the Function Description. When the serial interface is used, display data cannot be read.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	1	1	1	0	0
1	0	1	Read Data							

(11) Display Data Input Direction Select

This command sets the direction where the display RAM address number is automatically incremented. For details, see the description of "6.2.3 Column address circuit" in the Function Description.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Direction
0	1	0	1	0	0	0	0	1	0	0	Column
										1	Page

(12) Column Address Set Direction

This command can reverse the relationship between the display RAM data column address and segment driver output shown in Fig. 6.5 and 6.6. So you can reverse the sequence of segment driver output pins using this command. When the display data is written or read, the column address is incremented by (+1) according to the column address given in Fig. 6.4 and 6.5. For details, see the description of "6.2.3 Column address circuit" in the Function Description.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	0	1	0	0	0	0	0	Normal
										1	Reverse

(13) n-line Inversion Drive Register Set

This command sets the liquid crystal alternating drive reverse line count in the register to start line reverse driving operation. The line count to be set is 4 to 128 (32 states for each 4 lines. For details, see the description of "6.4 Display timing generation circuit" in the Function Description.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Reverse line count
0	1	0	0	0	1	1	0	1	1	0	Command
1	1	0	*	*	*	P4	P3	P2	P1	P0	Reverse line count

*: denote invalid bits.

P4	P3	P2	P1	P0	Reverse line count
0	0	0	0	0	4 (1 × 4)
0	0	0	0	1	8 (2 × 4)
			↓		↓
1	1	1	1	0	124 (31 × 4)
1	1	1	1	1	128 (32 × 4)

(14) n-line ON/OFF

This command provides ON/OFF control of n-line inverting drive.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	n-line
0	1	0	1	1	1	0	0	1	0	0	OFF
										1	ON

(15) Display Mode

This command sets the display mode. 4 gray-scale and binary display each have a different RAM configuration. For details, see the description of "6.2.1 Display Data RAM" in the Function Description.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Display mode
0	1	0	0	1	1	0	0	1	1	0	Command
1	1	0	*	*	*	*	*	*	P1	P0	Display mode

*: denote invalid bits.

P1	P0	Display mode
0	0	4gray-scale
0	1	Binary value

Set to 4 gray-scale (D1, D0) = (0, 0) at the time of resetting.

(16) Gray-scale Pattern Set

This command sets the level of gray-scale.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Gray-scale pattern
0	1	0	0	0	1	1	1	0	0	1	Command
1	1	0	*	P6	P5	P4	*	P2	P1	P0	Selection of gray-scale level

* (P6, P5, P4) : Selects the level of gray-scale bit (1, 0)
* (P2, P1, P0) : Selects the level of gray-scale bit (0, 1)

Gray-scale bit (1, 0)

	P6	P5	P4		P2	P1	P0	Level of gray-scale
–	0	0	1	–	–	–	–	White
–	0	1	0	–	–	–	–	
						↓		↓
–	1	1	0	–	–	–	–	Black

Gray-scale bit (0, 1)

	P6	P5	P4		P2	P1	P0	Level of gray-scale
–	–	–	–	–	0	0	1	White
–	–	–	–	–	0	1	0	
						↓		↓
–	–	–	–	–	1	1	0	Black

(17) Area Scroll Set

This command sets the area scroll. When the binary display is selected by the Display Mode Set command, the scroll end line address becomes a two-byte parameter.

① 4 gray-scale display

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Area scroll
0	1	0	0	0	0	1	0	0	0	0	Command
1	1	0	*	*	*	*	*	*	P11	P10	Scroll mode
1	1	0	P27	P26	P25	P24	P23	P22	P21	P20	Scroll start line address
1	1	0	P37	P36	P35	P34	P33	P32	P31	P30	Scroll end line address
1	1	0	P47	P46	P45	P44	P43	P42	P41	P40	Scroll display line count

*: denote invalid bits.

P11	P10	Scroll mode
0	0	0 (full screen)
0	1	1 (Upper)
1	0	2 (Lower)
1	1	3 (Central)

P27	P26	P25	P24	P23	P22	P21	P20	Scroll start line address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
						↓		↓
1	0	0	0	0	0	1	0	82H
1	0	0	0	0	0	1	1	83H

P37	P36	P35	P34	P33	P32	P31	P30	Scroll end line address
0	0	0	0	0	0	0	0	00H
0	0	0	0	0	0	0	1	01H
						↓		↓
1	0	0	0	0	0	1	0	82H
1	0	0	0	0	0	1	1	83H

P47	P46	P45	P44	P43	P42	P41	P40	Scroll display line count
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
						↓		↓
1	0	0	0	0	0	1	1	131
1	0	0	0	0	1	0	0	132

② Binary display

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Area scroll
0	1	0	0	0	0	1	0	0	0	0	Command
1	1	0	*	*	*	*	*	*	P11	P10	Scroll mode
1	1	0	P27	P26	P25	P24	P23	P22	P21	P20	Scroll start line address
1	1	0	P37	P36	P35	P34	P33	P32	P31	P30	Scroll end line address
1	1	0	*	*	*	*	*	*	*	P38	
1	1	0	P47	P46	P45	P44	P43	P42	P41	P40	Scroll display line count

*: denote invalid bits.

- Specifications on the parameters for scroll mode, scroll start line address and scroll display line count are the same as those on 4 gray-scale display.

	P37	P36	P35	P34	P33	P32	P31	P30 P38	Scroll end line address Binary value
1st byte 2nd byte	0 *	0 *	0 *	0 *	0 *	0 *	0 *	0 0	00H
	0 *	0 *	0 *	0 *	0 *	0 *	0 *	1 0	01H
							↓		↓
	0 *	0 *	0 *	0 *	0 *	1 *	1 *	0 1	106H
	0 *	0 *	0 *	0 *	0 *	1 *	1 *	1 1	107H

(18) Duty Set Command

Liquid crystal drive at a lower power consumption is ensured by using this command to change the duty. Use of this command also allows display at a desired position on the panel (continuous COM pins on a 4-line basis).
This command is used with a pair of the duty set parameter and start point (block) parameter, so be sure to set both parameters so that one of them will immediately follow the other.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected state
0	1	0	0	1	1	0	1	1	0	1	Duty set command
1	1	0	*	*	P15	P14	P13	P12	P11	P10	Duty set
1	1	0	*	*	P25	P24	P23	P22	P21	P20	Start point set

*: denote invalid bits.

• Duty set

Duty can be set in the range from 1/4 duty to 1/132 duty by 4 steps.
Set to 1/132 duty after resetting.

P15	P14	P13	P12	P11	P10	Duty set
0	0	0	0	0	0	1/4 duty set
0	0	0	0	0	1	1/8 duty set
0	0	0	0	1	0	1/12 duty set
0	0	0	0	1	1	1/16 duty set
			↓			↓
0	1	1	1	1	1	1/128 duty set
1	0	0	0	0	0	1/132 duty set

• Start point (block) register set parameter

Use this parameter to set 6-bit data in the start point (block) register. Then one of 33 start point blocks will be determined.
* Use the Display Start Line Set command (6) for display scroll. Do not use this command for display scroll.

P25	P24	P23	P22	P21	P20	Start piont setting
0	0	0	0	0	0	0 (COM0 to 3)
0	0	0	0	0	1	1 (COM4 to 7)
0	0	0	0	1	0	2 (COM8 to 11)
		↓				↓
0	1	1	1	1	1	31 (COM124 to 127)
1	0	0	0	0	0	32 (COM128 to 131)

Set to 0 block (D7 to D0: ***00000) at the time of resetting

* Voltage optimum to liquid crystal drive is changed when the duty is changed. Use the electronic volume and set the voltage to get the optimum display.

• Duty command setup example

1. Duty 1/88 When 1 (COM4 to COM7) is specified as the start point (block)
   Display area COM4 to COM91
2. Duty 1/68 When 26 (COM104 to COM107) is specified as the start point (block)
   Display area COM104 to COM131 and COM0 to COM39

* If the COM pin is not shared by the master and slave in the master/slave 2-chip operation (for vertical drive such as SEG132, COM80+COM80), the same duty must be used on the master and slave. Otherwise, display contrast will be different on the master and slave. When you want to disable display on either the master and slave, use the display OFF Mode Select command to set the side you want to disable, so that V_C level is output.

(19) Partial Display ON/OFF

The LCD partial display is turned on or off by this command.

A0	$\overline{E}$ / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Partial display
0	1	0	1	0	0	1	0	1	1	0	OFF
										1	ON

(20) Partial Display Set

This command sets the LCD partial display area. Duty is placed in the state selected by the Duty Set command. When partial display is switched by this command, liquid crystal drive voltage need not be changed. For details, see the description of “6.2.7 Partial Display” in the Function Description.

A0	$\overline{E}$ / $\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Partial display
0	1	0	0	0	1	1	0	0	1	0	Command
1	1	0	P17	P16	P15	P14	P13	P12	P11	P10	Display start line
1	1	0	P27	P26	P25	P24	P23	P22	P21	P20	Display line count

P17	P16	P15	P14	P13	P12	P11	P10	Display start line
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
						↓		↓
1	0	0	0	0	0	1	0	131
1	0	0	0	0	0	1	1	132

P17	P16	P15	P14	P13	P12	P11	P10	Display start line
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
						↓		↓
1	0	0	0	0	0	1	1	131
1	0	0	0	0	1	0	0	132

* The result of display start line added to display line count exceeding 132 should be disregarded.

(21) Read Modify Write

This command is paired with end command for use. If this command is entered, the column address is not changed by the Display Data Read command. It can be incremented +1 by the Display Data Read command alone. This state s retained until the End command is input. If the End command is input, the column address goes back to the address when the Read Modify Write command is input. This function reduces the MPU loads when changing the data repeated in the specific display area such as blinking cursor.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	0	0

* A command other than display data Read/Write command can be used in the Read Modify Write mode. However, you cannot use the column address set command.

• Sequence for cursor display

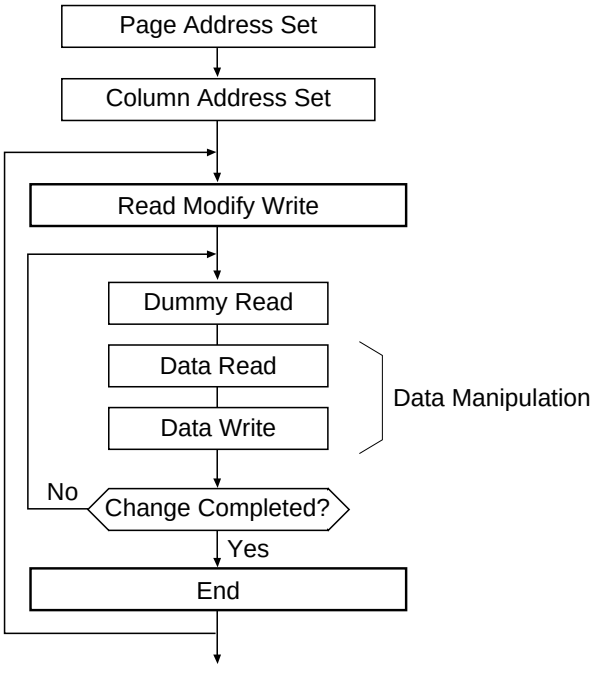


Fig. 7.2

(22) End

This command releases the read modify write mode and gets column address back to the initial address of the mode.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	1	1	1	0

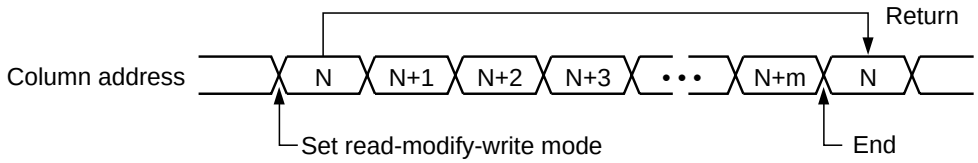


Fig. 7.3

(23) Built-in Oscillator Circuit ON/OFF

This command starts the built-in oscillator circuit operation. It is enabled only in the master operation mode (M/S = HIGH) when built-in oscillator circuit is valid (CLS = HIGH).
When the built-in power supply is used, the Oscillator Circuit ON command must be executed before the Power Control Set command. (See the description of "(16) power control command"). If the built-in oscillator circuit is turned off when the built-in power supply is used, display failure may occur.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Built-in oscillator circuit
0	1	0	1	0	1	0	1	0	1	0	OFF
										1	ON

(24) Built-in Oscillator Circuit Frequency Select

This command sets the built-in oscillator circuit frequency. The frequency can be selected whether the built-in oscillator circuit is turned on or off.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	fosc kHz	fCL kHz
0	1	0	0	1	0	1	1	1	1	1	Command	Command
1	1	0	*	*	*	*	P3	P2	P1	P0	Oscillation frequency	CL frequency

P3	P2	P1	P0	Oscillation frequency fosc kHz	CL frequency fCL kHz
0	0	0	0	120.0	fosc 120.0
0	0	0	1	100.0	fosc 100.0
0	0	1	0	88.0	fosc 88.0
0	0	1	1	76.0	fosc 76.0
0	1	0	0	120.0	fosc/2 = 60.0
0	1	0	1	100.0	fosc/2 = 50.0
0	1	1	0	88.0	fosc/2 = 44.0
0	1	1	1	76.0	fosc/2 = 38.0
1	0	0	0	120.0	fosc/4 = 30.0
1	0	0	1	100.0	fosc/4 = 25.0
1	0	1	0	88.0	fosc/4 = 22.0
1	0	1	1	76.0	fosc/4 = 19.0
1	1	0	0	120.0	fosc/8 = 15.0
1	1	0	1	100.0	fosc/8 = 12.5
1	1	1	0	88.0	fosc/8 = 11.0
1	1	1	1	76.0	fosc/8 = 9.5

(D7 to D0: ****0000) is set after resetting.

* The above-mentioned value is a Typ. value at 25°C. There is a tolerance of ±12% at 25°C.

(25) Power Control Set

This command sets the built-in power supply circuit function. For details, see the description of "6.7 Power supply circuit" in the Function Description.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	Selected state
0	1	0	0	0	1	0	0	1	0	1	Command
1	1	0	0	0	0	P4	P3	P2	P1	P0	Register set

P4	P3	P2	P1	P0	Selected state
1	1				Triple step-up
1	0				Double step-up
0	1				$V_{OUT} = V_{DD}$
		0			Step-up: OFF
		1			Step-up: ON
			0		V_C: OFF
			1		V_C: ON
				0	LCD voltage: OFF
				1	LCD voltage: ON

S1D15E06D00B∗: (LCD voltage: V_2, V_1, MV_1)
S1D15E06D00B∗: (LCD voltage: V_3, V_2, V_1, MV_1, MV_2)

An internal clock is required to operate the built-in power supply circuit. During the operation of the built-in power supply circuit, be sure that the internal clock is present inside.
If the built-in oscillator circuit is used, execute the built-in oscillator circuit ON command before the power control set command. If an external oscillator circuit is used, operate the external oscillator circuit before the power control set command.
If the internal clock is cut off during the operation of the built-in power supply circuit, display failure may occur. To avoid this, do not cut it off.
In the slave operation mode, only the parameters (D7 to D0 : ***00000) can be used with the power control set command. Do not use any other parameter.
100ms or more should be kept from V_C regulator circuit ON to LCDV circuit ON.

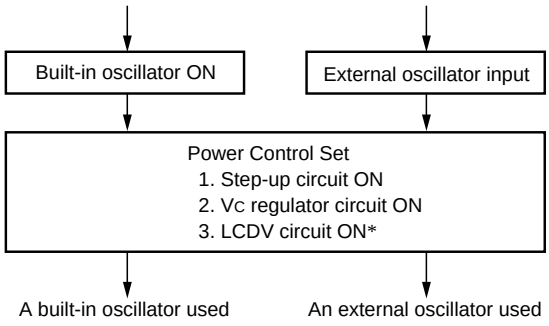


Fig. 7.4

(26) Step-up CK Frequency Select

This command selects the step-up CK and step-down CK frequencies.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	1	0	0	0	0	0	1	Command
1	1	0	*	P6	P5	P4	*	P2	P1	P0	Register

*: denote invalid bits.

(fosc/32) is set after resetting.

Step-up CK

	P6	P5	P4		P2	P1	P0	Step-up CK
–	–	–	–	–	0	1	1	fosc/8
–	–	–	–	–	1	0	0	fosc/16
–	–	–	–	–	1	0	1	fosc/32
		↓			1	1	0	fosc/64
–	–	–	–	–	1	1	1	fosc/128

It should not use the following. (P2, P1, P0) = (0, 0, 0) , (0, 0, 1) , (0, 1, 0)

Step-down CK

*	P6	P5	P4	*000	P2	P1	P0	Step-down CK
–	0	1	1	–	–	–	–	fosc/8
–	1	0	0	–	–	–	–	fosc/16
–	1	0	1	–	–	–	–	fosc/32
	1	1	0			↓		fosc/64
–	1	1	1	–	–	–	–	fosc/128

It should not use the following. (P6, P5, P4) = (0, 0, 0) , (0, 0, 1) , (0, 1, 0)

* For S1D15E06D00B∗, the step-down CK register is disabled.

(27) Liquid Crystal Drive Voltage Select

The liquid crystal drive voltage range issued from the liquid crystal drive voltage regulating circuit is selected from 3 states by this command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Vc voltage output range
0	1	0	0	0	1	0	1	0	1	1	Command
1	1	0	*	*	*	*	*	*	P1	P0	Register

*: denote invalid bits.

P1	P0	Vc voltage output range
0	0	1.77 to 3.50 V
1	0	2.53 to 5.00 V
1	1	3.54 to 7.00 V

VC voltage output range, 1.77 to 3.50V, (D1, D0) = (0, 0) is set after resetting.

(28) Electronic Volume

This command controls liquid crystal drive voltage VC issued from the built-in liquid crystal power supply voltage regulating circuit, and adjusts the liquid crystal display density. For details, see the description of "6.6.2 Voltage Regulating Circuit" in the Function Description.

A0	E / RD	R/W / WR	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	0	0	0	0	0	1	Command
1	1	0	*	P6	P5	P4	P3	P2	P1	P0	Register

*: denote invalid bits.

• Electronic Volume Register Set

When a 7-bit data to the electronic volume register is set by this command, liquid crystal drive voltage VC assumes one state out of voltage values in 128 states.
After this command is input, and the electronic volume register is set, the electronic volume mode is reset.

P6	P5	P4	P3	P2	P1	P0	Vc
0	0	0	0	0	0	0	Smaller
0	0	0	0	0	0	1	
0	0	0	0	0	1	0	
		↓					↓
1	1	1	1	1	1	0	
1	1	1	1	1	1	1	Larger

*: denote invalid bits.

• Electronic volume register set sequence

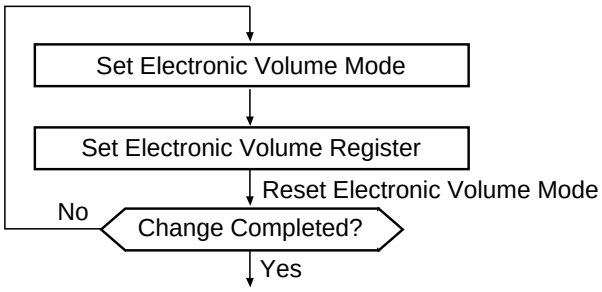


Fig. 7.5

(29) Discharge ON/OFF

This command discharges the capacitors connected to the power supply circuit. This command is used when the system power of this IC (S1D15E06 series) is turned off, and the duty is changed. See the description of (3) Power Supply OFF and (4) Changing the Duty in the Instruction Setup: Reference.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Setting
0	1	0	1	1	1	0	1	0	1	0	Discharge OFF
										1	Discharge ON

* If this command is executed when the external power supply is used, a large current may flow to damage the IC. If external power supply is used to drive liquid crystal, be sure to turn off the external power supply before executing this command.

(30) Power Saving

This command establishes the power save mode, thereby ensuring a substantial reduction of current consumption.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Power save mode
0	1	0	1	0	1	0	1	0	0	0	OFF
										1	ON

In the power save mode, display data and operation before power saving are maintained. Access to the display data RAM from the MPU is also possible. The current consumption is reduced to the value close to static current if all operations of the LCD display system are stopped and there is no access from the MPU.

In the power save mode, the following occurs:

Stop of oscillator circuit
Stop of LCD power supply circuit
Stop of all liquid crystal drive circuit (V_{SS} level output is issued as the segment and common driver output).

The power save OFF command releases the power save mode. The system goes back to the state before the power save mode.

* When the external power supply is used, it is recommended to stop the external power supply circuit function when the power save mode is started. For example, when each level of the liquid crystal drive voltage is given from the external resistive divider circuit, it is recommended to add a circuit to cut off the current flowing to the resistive divider circuit when power save function is started. The S1D15E06 series has a liquid crystal display blanking control control pin $\overline{DOF}$, and the level goes LOW when power save function is started. You can use the $\overline{DOF}$ output to stop the external power supply circuit function.

(31) Temperature Gradient Set

The 3-bit data of this command is used to set the temperature gradient characteristics of the liquid crystal drive voltage output from the built-in power supply circuit from eight states to one state. The temperature gradient of the liquid crystal drive voltage can be set according to the liquid crystal temperature gradient to be used. This eliminates the need of a temperature characteristics regulating circuit to be installed outside this IC (S1D15E06 series).

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Temperature gradient [%/°C]
0	1	0	0	1	0	0	1	1	1	0	Command
1	1	0	*	*	*	*	*	P2	P1	P0	Register

*: denote invalid bits.

P2	P1	P0	Temperature gradient [%/°C]
0	0	0	–0.06
0	0	1	–0.08
0	1	0	–0.10
0	1	1	–0.11
1	0	0	–0.13
1	0	1	–0.15
1	1	0	–0.17
1	1	1	–0.18

(D7 to D0: *****000) is set after resetting. *: denote invalid bits.

(32) Status Read

This command reads out the temperature gradient select bit set on the register.

A0	E $\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	Temperature gradient [%/°C]
0	1	0	1	0	0	0	1	1	1	0	Command
1	0	1	*	*	*	*	*	P2	P1	P0	Register

*: denote invalid bits.

P2	P1	P0	Temperature gradient [%/°C]
0	0	0	–0.06
1	0	0	–0.08
0	1	0	–0.10
1	1	0	–0.11
0	0	1	–0.13
1	0	1	–0.15
0	1	1	–0.17
1	1	1	–0.18

(33) Reset

This command resets the column address, page address, read modify write mode and test mode without giving adverse effect to the display data RAM. For details, see the description of "6.8 Reset" in Function Description. Resetting is carried out after the reset command has been input.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	0

Initialization upon application of power supply is carried out by the reset signal to the $\overline{RES}$ pin. The reset command cannot be used for this purpose.

(34) MLS drive selection command

These are the MLS drive selection commands. These commands changes over between the dispersive drive and nondispersive drive.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0	Temperature gradient [%/˚C]
0	1	0	1	0	0	1	1	1	0	0	**Command**
1	1	0	*	*	*	*	P3	P2	P1	P0	**Register**

* indicates the invalid bits.

P3	P2	P1	P0	Temperature gradient [%/˚C]
0	0	0	0	**Dispersive drive**
1	0	0	0	**Nondispersive drive**

After resetting, nondispersive drive will be preset in 4 gradation indications.
In case the B/W indication is selected after resetting, dispersive drive will be preset.

Dispersive drive and nondispersive drive are the LCD drive methods characteristic to the MLS drive.
The S1D15E06 Series is making 4 line MLS drive and, 4 times higher period selection voltage than that of the period being used for indication of 1 line in an ordinary drive (in case of 132 line indication, the period of 1/132 of 1 frame). In case of the dispersive drive, the selection signals will be output for four times, separately, within the period of 1 frame. With this dispersive drive method, it is possible to reduce the frame frequency as compared with the nondispersive drive method. Therefore, when it becomes necessary to reduce the current consumption, we recommend you to use this dive method. However, in case of the drive method where moving pictures are to be indicated, the indication may become flickered and this dispersive drive method is not suitable for indications of moving pictures.

(35) NOP

This is a Non-Operation command.

A0	E (RD)	R/W (WR)	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	0	0	0	1	1

Note: S1D15E06 series maintains the operation status due to the command. However, when exposed to excessive external noise, internal status may be changed. This makes it necessary to take some measures which reduces noise generation in terms of installation or system configuration, or which protects the system against adverse effect of noise. To cope with sudden noise, it is recommended to refresh the operation status on a periodic basis.

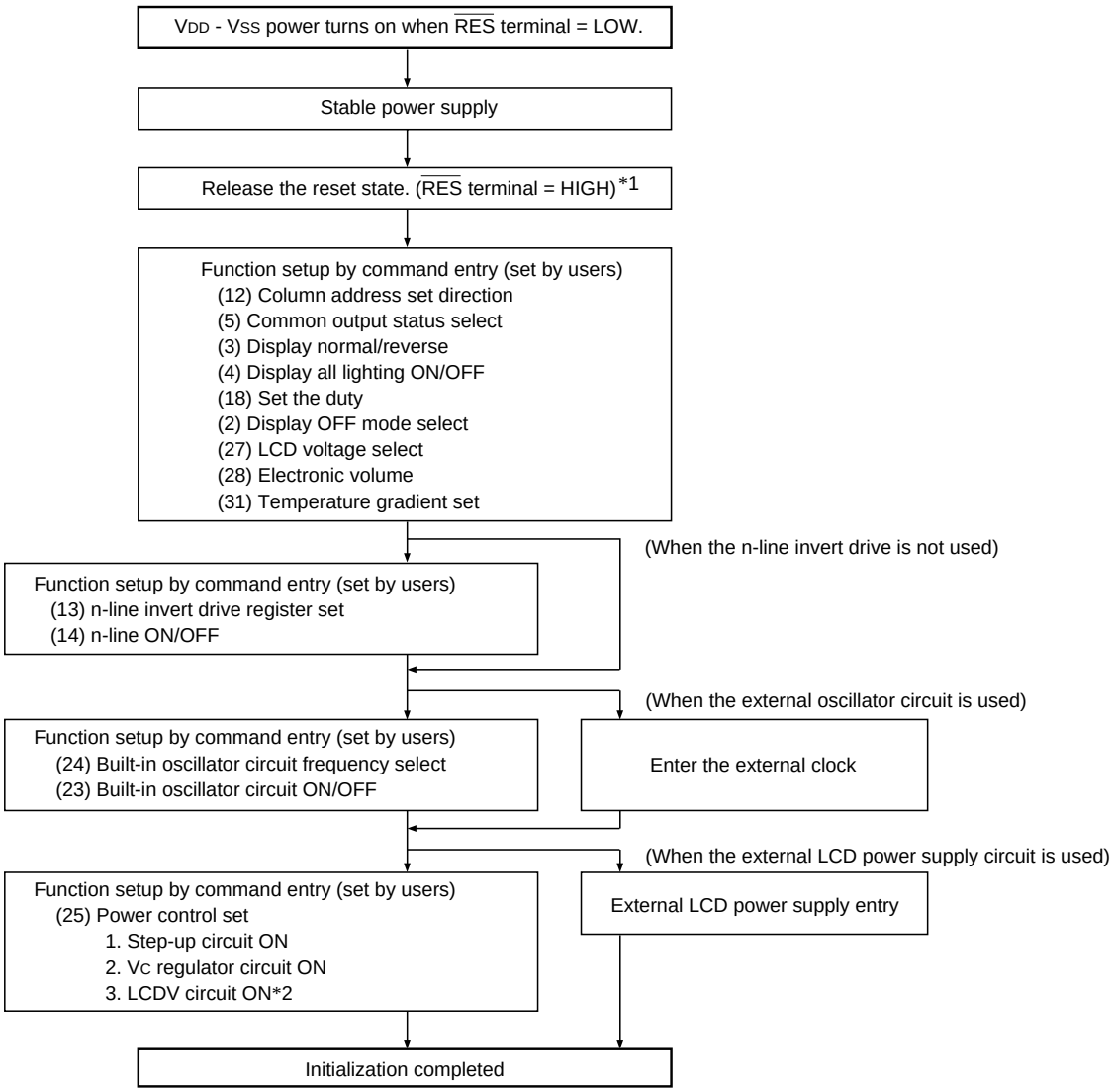
Table 7.1 Table of commands in S1D15E06 series

Command	Command code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	LCD display ON/OFF control. 0: OFF, 1: ON
(2) Display OFF Mode Select	0	1	0	1	0	1	1	1	1	1	0 1	Output level when the display is OFF and in the power save mode 0: V_{SS}, 1: V_C
(3) Display Normal /Reverse	0	1	0	1	0	1	0	0	1	1	0 1	LCD display normal/reverse 0: Normal, 1: Reverse
(4) Display All Lighting ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Display All Lighting 0: Normal display, 1: All ON
(5) Common Output Status Select	0	1	0	1	1	0	0	0	1	0	0 1	Selects COM output scan direction. 0: Normal, 1: Reverse
(6) Display Start Line Set	0 1 1	1 1 1	0 0 0	1 Display start line address *	0 * *	0 * *	0 * *	1 * *	0 * *	1 * *	0 ↓	Sets display start line. When the display mode is binary, the parameter consists of two bytes.
(7) Page Address Set	0	1	0	1 *	0 *	1	1 Page address	0	0	0	1	Sets the display RAM page address.
(8) Column Address Set	0 1	1 1	0 0	0	0 Column Address Set	0	1	0	0	1	1	Sets the display RAM column address.
(9) Display Data Write	0 1	1 1	0 0	0	0	0 Writes data	1	1	1	0	1	Writes data to the display RAM.
(10) Display Data Read	0 1	1 0	0 1	0	0	0 Reads data	1	1	1	0	0	Reads data to the display RAM.
(11) Display Data Input Direction Select	0	1	0	1	0	0	0	0	1	0	0 1	Display RAM data input direction 0: Column direction 1: Page direction
(12) Column Address Set Direction	0	1	0	1	0	1	0	0	0	0	0 1	Compatible with display RAM address SEG output 0: Normal 1: Reverse
(13) N-line inversion Drive Register Set	0 1	1 1	0 0	0 *	0 *	1 *	1 Invert line count	0	1	1	0	Line invert drive. Sets the line count.
(14) N-line ON/OFF	0	1	0	1	1	1	0	0	1	0	0 1	Resets the line invert drive. 0: N-line OFF 1: N-line ON
(15) Display Mode	0 1	1 1	0 0	0 *	1 *	1 *	0 *	0 *	1 *	1 Mode	0	00: 4 gray-scale, 01: binary
(16) Gray-scale Pattern Set	0 1	1 1	0 0	0	0 Gray-scale pattern	1	1	1	0	0	1	Selects the contrast of gray-scale bit (1,0) (0,1).
(17) Area Scroll Scroll Mode Scroll Start address Scroll End address Display page count	0 1 1 1 1	1 1 1 1 1	0 0 0 0 0	0 * Start address End address Display page count	0 * *	0 * *	1 * *	0 * *	0 * *	0 Mode *	0 *	When the display mode is binary, the end address consists of two bytes.
(18) Duty Set Command Duty Set Static spot (block) set	0	1	0	0 * *	1 * *	1 Duty count Static spot (block)	0	1	1	0	1	
(19) Partial Display ON/OFF	0	1	0	1	0	0	1	0	1	1	0 1	Partial display ON/OFF 0: OFF, 1: ON
(20) Partial Display Set Display Start line Display Line count	0	1	0	0	0	1 Start line Line count	1	0	0	1	0	
(21) Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments the column address. Increments +1 in the write mode. Does not increment in the read mode.
(22) End	0	1	0	1	1	1	0	1	1	1	0	Resets read modify write functions.
(23) Built-in Oscillator Circuit ON/OFF	0	1	0	1	0	1	0	1	0	1	0 1	Built-in oscillator circuit operation 0: OFF, 1: ON
(24) Built-in Oscillator Circuit Frequency Select	0 1	1 1	0 0	0 *	1 *	0 *	1 *	1 Frequency	1	1	1	
(25) Power Control Set	0 1	1 1	0 0	0 *	0 *	1	0	0 Operation state	1	0	1	Selects built-in power supply operation state.

Command	Command code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(26) Step-up CK Frequency Select	0	1	0	0	1	0	0	0	0	0	1	
	1	1	0	*		Frequency						
(27) Liquid Crystal Drive Voltage Select	0	1	0	0	0	1	0	1	0	1	1	
	1	1	0	*	*	*	*	*	*	Vc range		
(28) Electronic Volume Mode Set	0	1	0	1	0	0	0	0	0	0	1	
Electronic Volume Register Set	1	1	0	*	Electronic volume							Vc output voltage is set to the electronic volume register. 128 states
(29) Discharge ON/OFF	0	1	0	1	1	1	0	1	0	1	0 1	Discharges Power supply circuit connection capacitor. 0: OFF (normal), 1: ON
(30) Power Save ON/OFF	0	1	0	1	0	1	0	1	0	0	0	Power Save 0: OFF, 1: ON
(31) Temperature Gradient Select	0	1	0	0	1	0	0	1	1	1	0	Sets to 8 steps.
	1	1	0	*	*	*	*	* Temperature gradient				
(32) Stator Read	0	1	0	1	0	0	0	1	1	1	0	Issues the temperature gradient select bit.
	1	0	1	*	*	*	*	*Temperature gradient				
(33) Reset	0	1	0	1	1	1	0	0	0	1	0	Resets the column, page and address registers.Resets the read modify write function.
(34) MLS drive selection	0	1	0	1	0	0	1	1	1	0	0	MLS drive method 0 : Dispersive, 1 : Nondispersive
	1	1	0	*	*	*	*	MLS drive method				
(35) NOP	0	1	0	1	1	1	0	0	0	1	1	Non-operation command

Instruction Setup Example (Reference)

(1) Initial setup

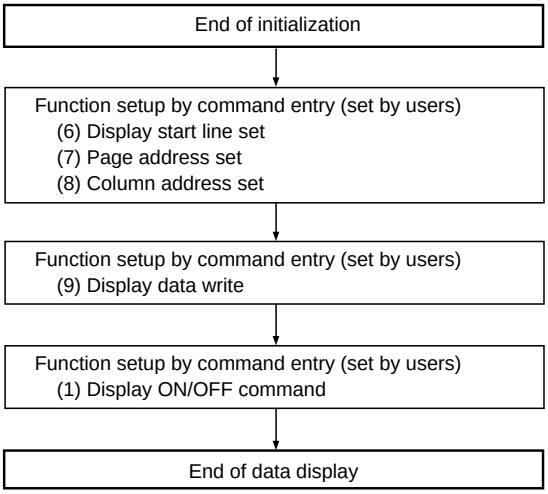


Note: *1 Display data RAM contents are not determined even in the initialized state after resetting. See "6.7 Reset Circuit" in the "6. Function Description".

*2 100ms or more should be kept from VC regulator circuit ON to LCDV circuit ON.

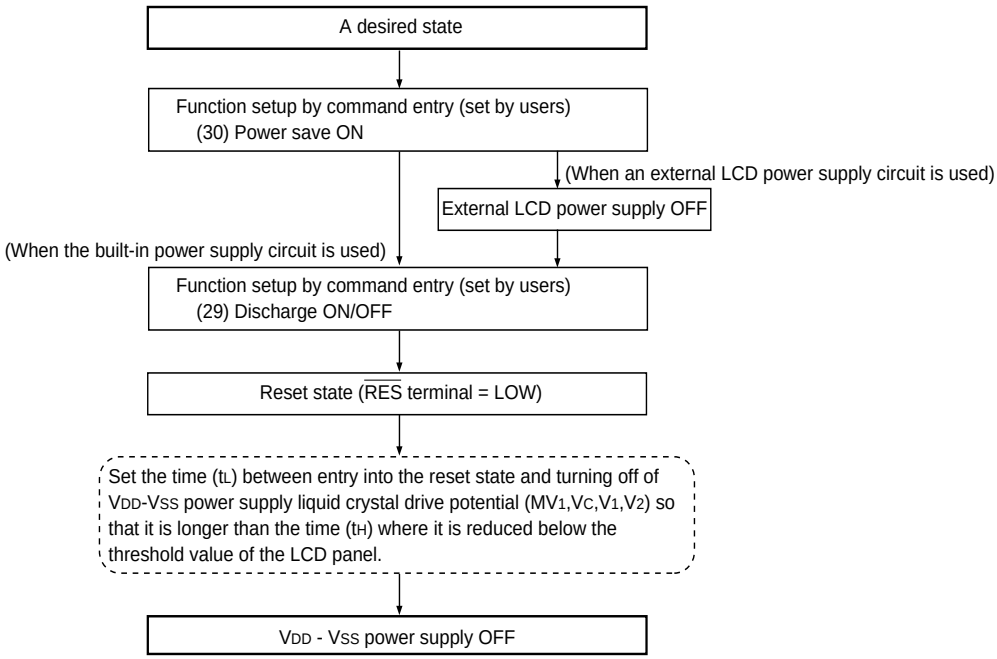
* Numerals in the command parenthesis correspond to the numerals of the items in Command Description.

(2) Data display



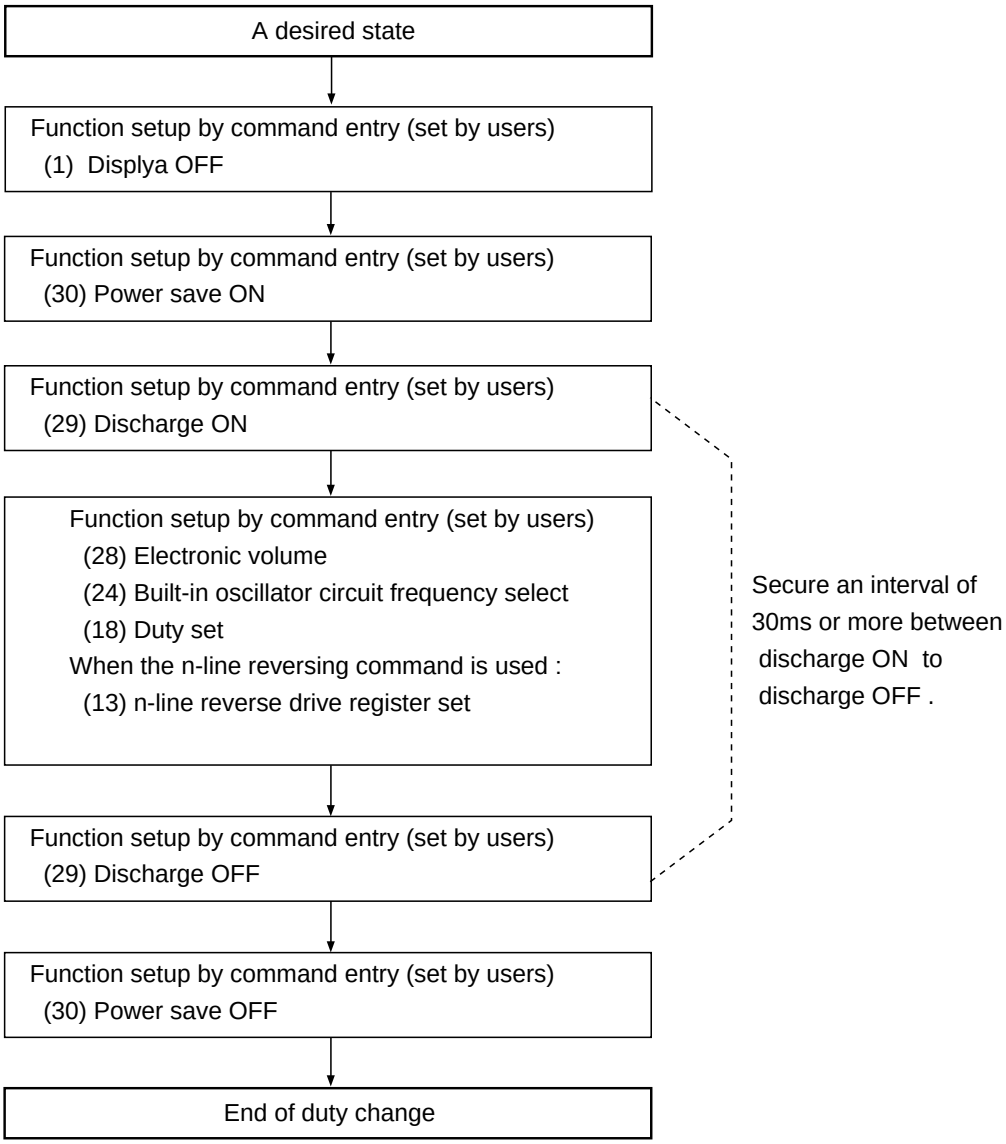
Note: * Display data RAM contents are not determined after end of initialization. Write data to all the Display data RAM used for display. See "9. Display data write" in the "7. Command Description".

(3) Power OFF



Note: * This IC controls the circuit of the liquid crystal drive power supply system using the VDD-VSS power supply circuit. If the VDD-VSS power supply is cut off with voltage remaining in the liquid crystal drive power supply system, voltage not controlled will be issued from the SEG and COM pins, and this may result in display failure. To avoid this, follow the above-mentioned power off sequence.

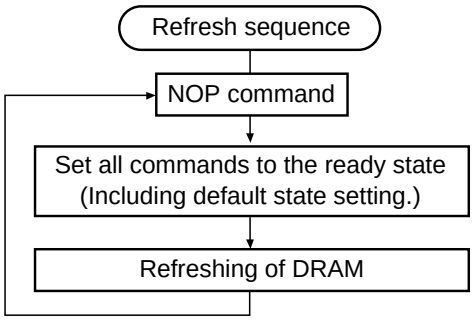
(4) How to change the duty



Note: * Execution of the above sequence causes display to be turned off temporarily (for the time from Power Saving command ON to Power Saving command OFF plus 200 ms (frame frequency 60Hz) upon switching of the duty. Temporary display failure may occur if Duty Change command is executed during liquid crystal display without executing the above-mentioned setup example. Follow the setup example when the duty is changed as discussed above.

(5) Refresh

It is recommended that the operating modes and display contents be refreshed periodically to prevent the effect of unexpected noise.



8. ABSOLUTE MAXIMUM RATINGS

Table 8 V_{SS} = 0V unless otherwise specified.

Item		Symbol	Specified value	Unit
Power voltage (1)		V_{DD}	–0.3 to +4.0	V
Power voltage (2)		V_3, V_{OUT}	–0.3 to +17.0	
Power voltage (3)		V_2, V_1, V_C, MV_1, MV_2	–0.3 to V_3	
Input voltage		V_{IN}	–0.3 to V_{DD}+0.3	
Output voltage		V_O	–0.3 to V_{DD}+0.3	
Operating temperature		T_{OPR}	–40 to +85	°C
Storage temperature	TCP	T_{STR}	–55 to +100	
	bare chip		–55 to +125	

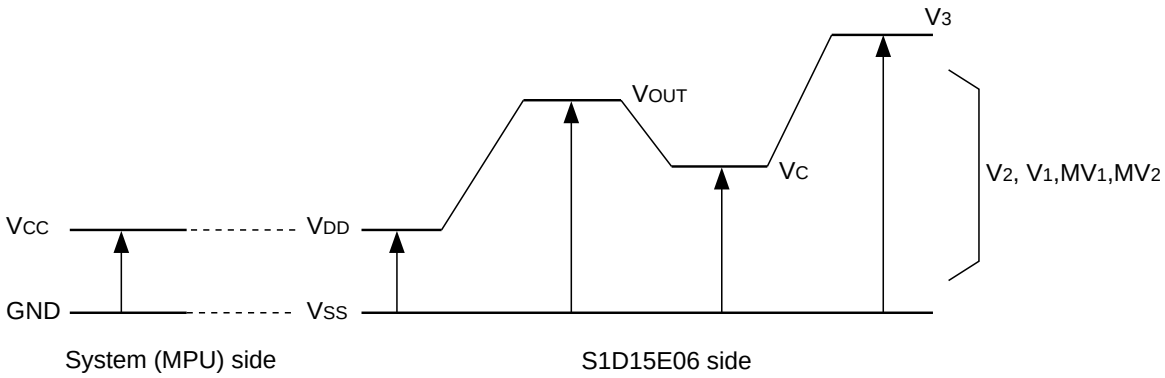


Fig. 8

Notes: 1. Voltages V_3, V_2, V_1, V_C, MV_1, MV_2 and MV_3 (V_{SS}) must always meet the conditions of $V_3 \geq V_2 \geq V_1 \geq V_C \geq MV_1 \geq MV_2 \geq MV_3$ (V_{SS}).
2. Voltage V_{OUT} must always meet the conditions of $V_{OUT} \geq V_{DD}$ and $V_{OUT} \geq V_C$.
3. If the LSI has been used in excess of the absolute maximum rating, it may be subjected to permanent breakdown. So in the normal operation, the LSI is preferred to be used under the condition of electrical characteristics. If this condition is not met, LSI operation error may occur and LSI reliability may be deteriorated.

9. DC CHARACTERISTICS

V_{SS} = 0V, V_{DD} = 2.7V ± 10% and Ta = –40 to +85°C unless otherwise specified.

Table 9.1

Item		Symbol	Conditions		Specified value Min.	Typ.	Max.	Unit	Applicable pin
Working voltage (1)	Operation enabled	V_{DD}			1.7	—	3.6	V	V_{DD} *1
Working voltage (2)	Operation recommended	V_{OUT}			V_{DD}	—	16.0		V_{OUT}
Working voltage (3)	Operation enabled	V_3	Applicable to		3.4	—	14.0		V_3 *2
	Operation enabled	V_C	S1D15E06D01****		1.7	—	7.0		V_C
	Operation enabled	V_2			V_C	—	V_3		V_2
	Operation enabled	V_1			V_C	—	V_3		V_1
	Operation enabled	MV_1			V_{SS}	—	V_C		MV_1
	Operation enabled	MV_2			V_{SS}	—	V_C		MV_2
Working voltage (4)	Operation enabled	V_3	Applicable to		3.4	—	16.0		V_3 *2
	Operation enabled	V_C	S1D15E06D03****		1.7	—	8.0		V_C
	Operation enabled	V_2			V_C	—	V_3		V_2
	Operation enabled	V_1			V_C	—	V_3		V_1
	Operation enabled	MV_1			V_{SS}	—	V_C		MV_1
	Operation enabled	MV_2			V_{SS}	—	V_C		MV_2
High-level input voltage		V_{IHC}	V_{DD}=1.7V to 3.6V		0.8×V_{DD}	—	V_{DD}		*3
Low-level input voltage		V_{ILC}			V_{SS}	—	0.2×V_{DD}		*3
High-level output voltage		V_{OHC}	V_{DD}=1.7V to 3.6V	I_{OH}=–0.25mA	0.8×V_{DD}	—	V_{DD}		*4
Low-level output voltage		V_{OLC}		I_{OL}=0.25mA	V_{SS}	—	0.2×V_{DD}		*4
Input leak current		I_{LI}	V_{IN}=V_{DD} or V_{SS}		–1.0	—	1.0	µA	*5
Output leak current		I_{LO}			–3.0	—	3.0		*6
LCD driver ON resistance		R_{ON}	Ta=25°C	V_3=7.2V	—	1.5	2.3	kΩ	SEGn
				V_3=4.8V	—	3.0	4.6		COMn *7
Static current consumption		I_{DDQ}	Ta=25°C	V_{DD}=3.6V	—	0.2	5.0	µA	V_{DD}
		I_{3Q}		V_3=14.0V	—	1.0	5.0		V_3
Input pin capacity		C_{IN}	Ta=25°C, f=1MHz		—	20	25	pF	
Oscillation frequency	Built-in oscillation	f_{OSC}	Ta=25°C Max. frequency		110	120	130	kHz	*8

[* See the description on P.57.]

Table 9.2

Item		Symbol	Conditions	Specified value			Unit	Applicable pin
				Min.	Typ.	Max.		
Built-in power circuit	Input voltage	V_{DD} V_{DD}	Double boosting Triple boosting	1.7 1.7	— —	3.6 3.6	V	V_{DD}
	Boosted output voltage (1)	V_{OUT}	S1D15E06D01****	—	—	14.0		V_{OUT}
	Boosted output voltage (2)	V_{OUT}	S1D15E06D03****	—	—	16.0		V_{OUT}
	Working voltage for voltage control circuit	V_C		1.8	—	8.0		V_C *9

Dynamic current consumption (1): Built-in power is turned on during display. Ta=25°C
This is the current consumed by the entire IC including the built-in power supply.

Display mode in 4 gray-scale at f_{FR} = 80Hz

Table 9.3 Display entirely in white Code: Iss (1)

V_{DD}	Boosting	V_3 Voltage	1/132 DUTY		1/100 DUTY		Unit	Remarks
			Typ.	Max.	Typ.	Max.		
2.7V	Triple	10V	68	112	67	111	µA	*10
		12V	81	134	71	117		
3.6V	Double	10V	73	121	63	104		
	Triple	12V	93	154	83	137		

Display mode in 4 gray-scale at f_{FR} = 80Hz

Table 9.4 Display: Heavy load display Code: Iss (1)

V_{DD}	Boosting	V_3 Voltage	1/132 DUTY		1/100 DUTY		Unit	Remarks
			Typ.	Max.	Typ.	Max.		
2.7V	Triple	10V	241	400	187	310	µA	*10
		12V	373	619	313	519		
3.6V	Double	10V	189	313	146	242		
	Triple	12V	380	630	314	521		

Display mode in binary at f_{FR} = 60Hz

Table 9.5 Display entirely in white Code: ISS (1)

V_{DD}	Boosting	V_3 Voltage	1/132 DUTY		1/100 DUTY		Unit	Remarks
			Typ.	Max.	Typ.	Max.		
2.7V	Triple	10V	65	108	50	83	µA	*10
		12V	72	120	56	93		
3.6V	Double	10V	57	95	44	73		
	Triple	12V	82	136	63	104		

[* See the description on P.57.]

Display mode in binary at f_{FR} = 60Hz

Table 9.6 Display Heavy load display Code: ISS (1)

V_{DD}	Boosting	V_3 Voltage	1/132 DUTY		1/100 DUTY		Unit	Remarks
			Typ.	Max.	Typ.	Max.		
2.7V	Triple	10V	188	312	135	224	µA	*10
		12V	313	520	226	300		
3.6V	Double	10V	150	249	108	143		
	Triple	12V	322	534	232	308		

Current consumption under power saving mode: V_{SS} = 0V, V_{DD} = 3.3V, Ta = 25°C

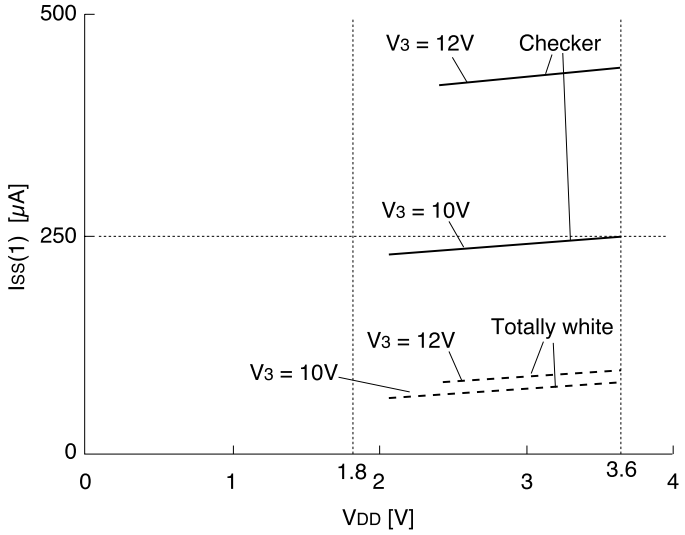
Table 9.7

Item	Symbol	Condition	Specified value			Unit	Remarks
			Min.	Typ.	Max.		
Sleep state	I_{DDS1}		—	0.2	5	µA	

[* See the description on P.57.]

[Reference Data 1]

• Dynamic current consumption (1) during LCD display when internal power is used

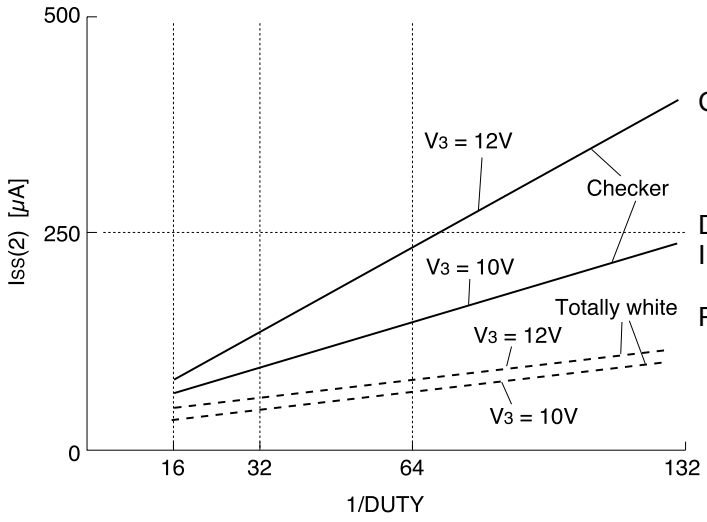


Conditions: Built-in power supply "ON"
1/132DUTY
f_{FR} = 80Hz
Triple boosting
Display mode : 4 gray-scale
Indication pattern: Totally white / Checker
Ta = 25°C
Remarks: *11

Fig. 9.1

[Reference Data 2]

• Dynamic current consumption (2) during LCD display when internal power is used



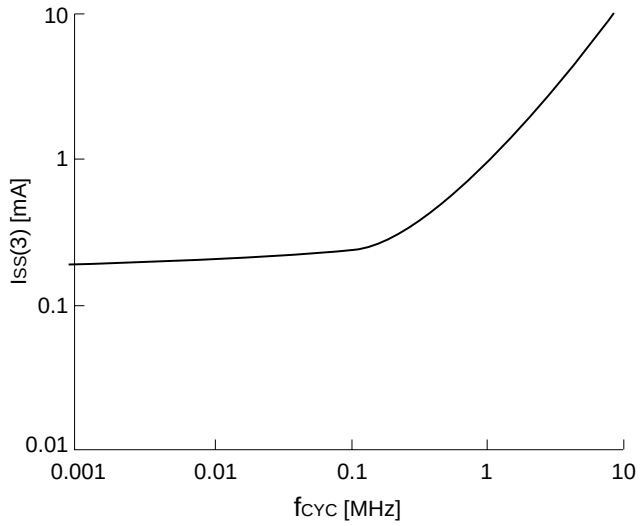
Conditions: V_{DD} = 2.7V
Built-in power supply "ON"
Triple boosting
f_{FR} = 80Hz
Display mode : 4 gray-scale
Indication pattern : Totally white / Checker
Ta = 25°C
Remarks: *11

Fig. 9.2

[* See the description on P.57.]

[Reference Data 3]

- Dynamic current consumption (3) during access



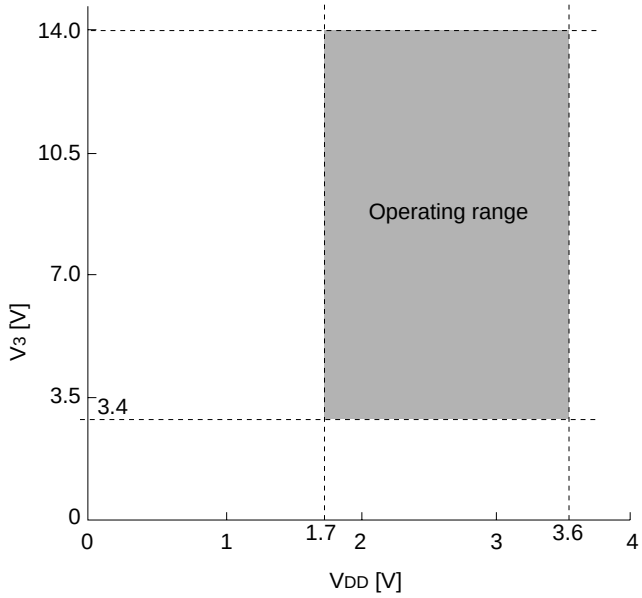
Indicates the current consumption when the checker pattern is always written by f_{CYC}. When not accessed, only $I_{SS}(1)$ remains.

Conditions: Built-in voltage used
Triple boosting
V_3= 12.0V, V_{DD} = 2.7V
Ta = 25°C
f_{FR}=80Hz 1/132 Duty

Fig. 9.3

[Reference Data 4]

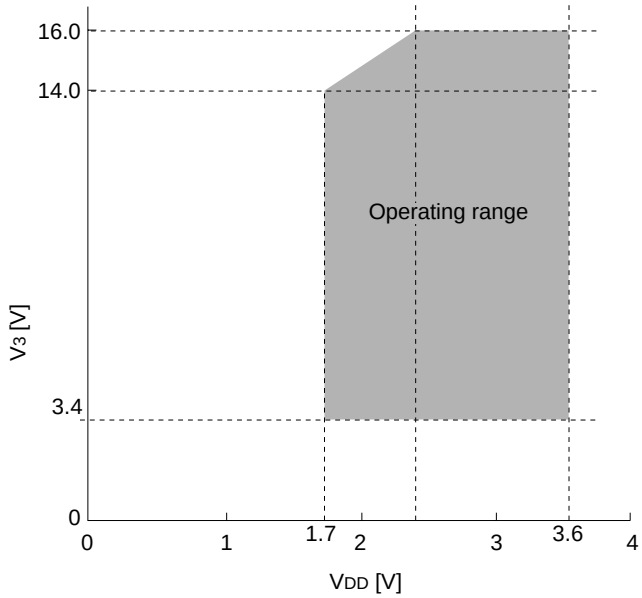
• Operating voltage range (S1D15E06D01∗∗∗∗)



Remarks: *2

Fig. 9.4.1

• Operating voltage range (S1D15E06D03∗∗∗∗)



Remarks: *2

Fig. 9.4.2

[* See the description on P.57.]

• Relationship between oscillation frequency f_{OSC}, display clock frequency f_{CL} and liquid crystal frame f_{FR}

Table 9.8

Item	f_{CL}	Display mode	f_{FR}
Built-in oscillator circuit used	See p. 24	Binary display 4 gray-scale	(f_{CL} × DUTY)/4 (f_{CL} × DUTY)/8
Built-in oscillator circuit not used	External input (f_{CL})	Binary display 4 gray-scale	(f_{CL} × DUTY)/4 (f_{CL} × DUTY)/8

(f_{FR} indicates the cycle of rewriting one screen; it does not indicate FR signal cycle.)

[Asterisked references]

*1. Does not guarantee if there is an abrupt voltage variation during MPU access.
*2. For V_{DD} and V_3 system operating voltage range, see Fig. 9.5.
Applicable when the external power supply is used.
*3. A0, D0 to D5, D6(SCL), D7(SI), $\overline{RD}$(E), $\overline{WR}$(R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, CL, FR, F1, F2, CA, M/S, C86, P/S, $\overline{DOF}$, $\overline{RES}$ and TEST pins
*4. D0 to D7, FR, $\overline{DOF}$, CL, F1, F2 and CA pins
*5. A0, $\overline{RD}$(E), $\overline{WR}$(R/$\overline{W}$), $\overline{CS1}$, CS2, CLS, M/S, C86, P/S, $\overline{RES}$ and TEST pins
*6. Applicable when D0 to D5, D6(SCL), D7(S1), CL, FR, $\overline{DOF}$, F1, F2 and CA pins have a high impedance.
*7. Indicates the resistance when 0.1V voltage is applied between the output pin SEGn or COMn and each power supply (V_2, V_1, V_C, MV_1, MV_2).
R_{ON} =0.1V/ΔI (where ΔI denotes current when 0.1V is applied when power is on).
*8. For the relationship between oscillation frequency and frame frequency, see Table 9.8. The standard values of the external input item are recommended ones.
*9. The V_C voltage regulating circuit should be adjusted within the electronic volume operation range.
*10. Indicates the current consumed by a single IC when display is on. Use the electronic volume for voltage regulation. Also use the internal oscillator circuit. The current due to LCD panel capacity and wiring capacity is not included. Applicable when there is access from the MPU.

10. TIMING CHARACTERISTICS

(1) System path read/write characteristics 1 (80 system MPU)

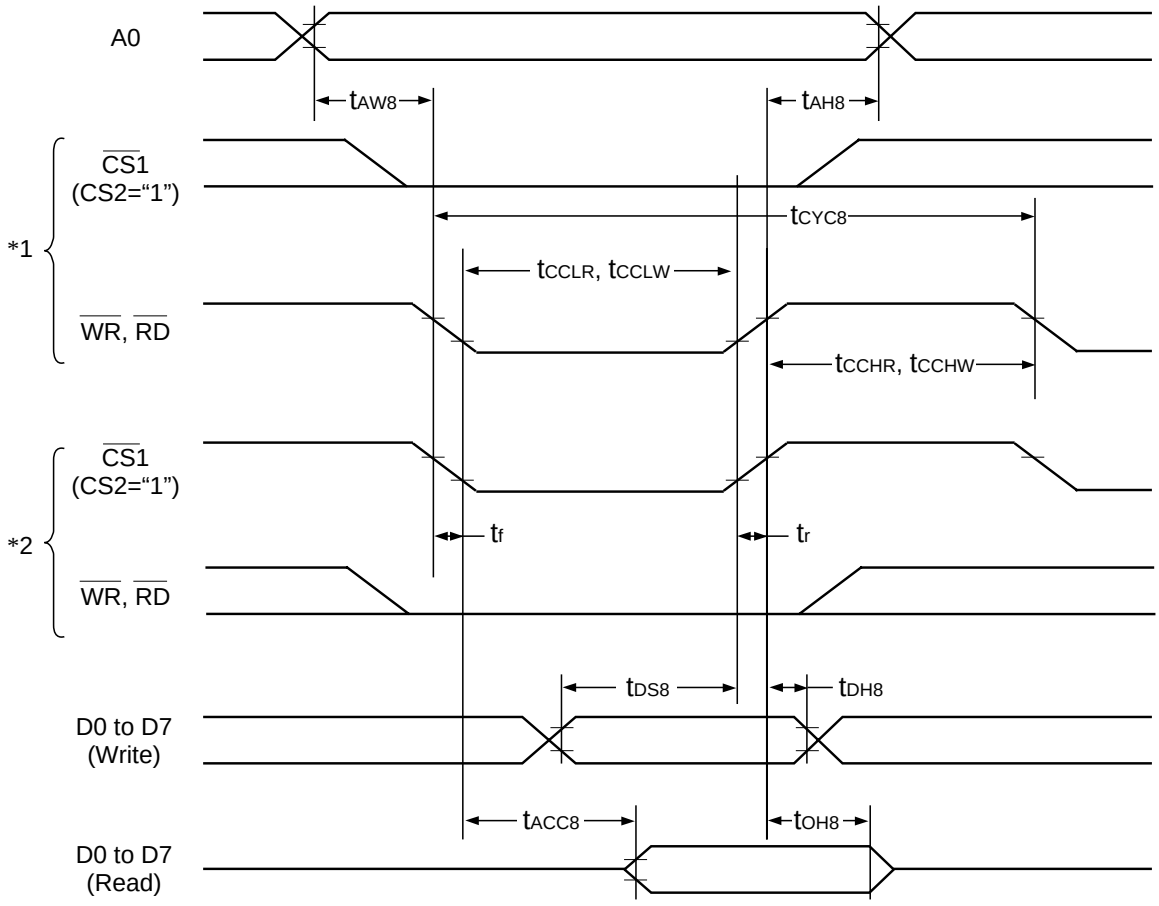


Fig. 10.1

Table 10.1.1

[V_{DD} = 3.0V to 3.6V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System write cycle time	$\overline{WR}$	t_{WCYC8}		200	—	
System read cycle time	$\overline{RD}$	t_{RCYC8}		300	—	
Control LOW-pulse width (Write)	$\overline{WR}$	t_{CCLW}		60	—	
Control LOW-pulse width (Read)	$\overline{RD}$	t_{CCLR}		100	—	
Control HIGH-pulse width (Write)	$\overline{WR}$	t_{CCHW}		60	—	
Control HIGH-pulse width (Read)	$\overline{RD}$	t_{CCHR}		100	—	
Data setup time	D0 to D7	t_{DS8}		20	—	
Data hold time		t_{DH8}		10	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	80	
Output disable time		t_{OH8}		10	80	

Table 10.1.2

[V_{DD} = 2.4V to 3.0V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System write cycle time	$\overline{WR}$	t_{WCYC8}		300	—	
System read cycle time	RD	t_{RCYC8}		400	—	
Control LOW-pulse width (Write)	$\overline{WR}$	t_{CCLW}		80	—	
Control LOW-pulse width (Read)	$\overline{RD}$	t_{CCLR}		200	—	
Control HIGH-pulse width (Write)	$\overline{WR}$	t_{CCHW}		80	—	
Control HIGH-pulse width (Read)	RD	t_{CCHR}		200	—	
Data setup time	D0 to D7	t_{DS8}		30	—	
Data hold time		t_{DH8}		15	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	120	
Output disable time		t_{OH8}		10	120	

Table 10.1.3

[V_{DD} = 1.7V to 2.4V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value		Unit
				Min.	Max.	
Address hold time	A0	t_{AH8}		0	—	ns
Address setup time		t_{AW8}		0	—	
System write cycle time	$\overline{WR}$	t_{WCYC8}		400	—	
System read cycle time	RD	t_{RCYC8}		600	—	
Control LOW-pulse width (Write)	$\overline{WR}$	t_{CCLW}		100	—	
Control LOW-pulse width (Read)	$\overline{RD}$	t_{CCLR}		250	—	
Control HIGH-pulse width (Write)	$\overline{WR}$	t_{CCHW}		140	—	
Control HIGH-pulse width (Read)	RD	t_{CCHR}		250	—	
Data setup time	D0 to D7	t_{DS8}		40	—	
Data hold time		t_{DH8}		20	—	
$\overline{RD}$ access time		t_{ACC8}	C_L=100pF	—	200	
Output disable time		t_{OH8}		10	200	

*1. This is in case of making the access by $\overline{WR}$ and $\overline{RD}$, setting the $\overline{CS1}$ = LOW.
*2. This is in case of making the access by $\overline{CS1}$, setting the $\overline{WR}$, $\overline{RD}$ = LOW.
*3. Input signal rise and fall time (tr, tf) must not exceed 15 ns. When the system cycle time is used at a high speed, it is specified by $(t_r + t_f) \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $(t_r + t_f) \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$.
*4. Timing is entirely specified with reference to 20% or 80% of V_{DD}.
*5. t_{CCLW} and t_{CCLR} are specified in terms of the overlapped period when $\overline{CS1}$ is at LOW (CS2 = HIGH) level and $\overline{WR}$ and $\overline{RD}$ are at LOW level.

(2) System path read/write characteristics 2 (68 system MPU)

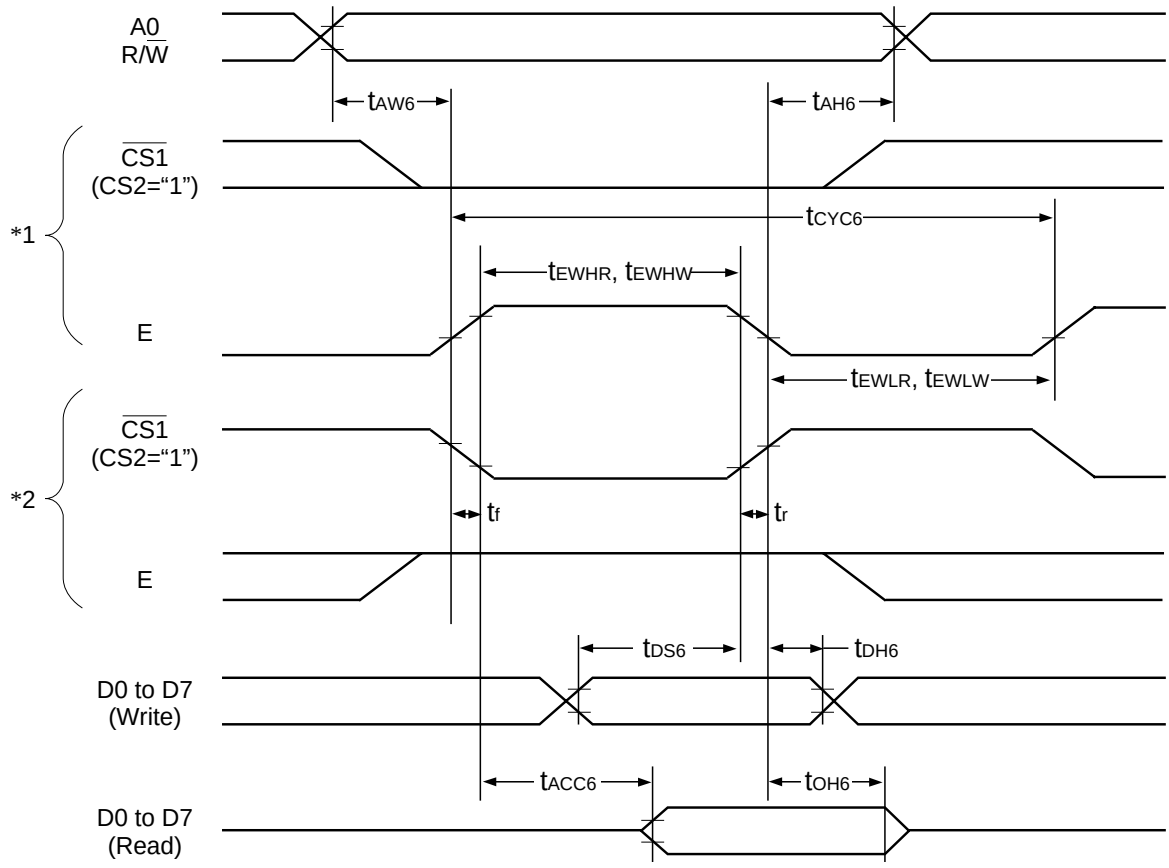


Fig. 10.2

Table 10.2.1

[V_{DD} = 3.0V to 3.6V, Ta = –40 to +85°C]

Parameter		Signal	Symbol	Condition	Specified value		Unit
					Min.	Max.	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns
System write cycle time System read cycle time		E	t_{WCYC6} t_{RCYC6}		200 300	— —	
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		20 10	— —	
Access time Output disable time			t_{ACC6} t_{OH6}	C_L=100pF	— 10	80 80	
Enable HIGH-pulse width	Read Write	E	t_{EWHR} t_{EWHW}		100 60	— —	
Enable LOW-pulse width	Read Write	E	t_{EWLR} t_{EWLW}		100 60	— —	

Table 10.2.2

[V_{DD} = 2.4V to 3.0V, Ta = –40 to +85°C]

Parameter		Signal	Symbol	Condition	Specified value		Unit
					Min.	Max.	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns
System write cycle time System read cycle time		E	t_{WCYC6} t_{RCYC6}		300 400	— —	
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		30 15	— —	
Access time Output disable time			t_{ACC6} t_{OH6}	C_L=100pF	— 10	120 120	
Enable HIGH-pulse width	Read Write	E	t_{EWHR} t_{EWHW}		150 80	— —	
Enable LOW-pulse width	Read Write	E	t_{EWLR} t_{EWLW}		150 80	— —	

Table 10.2.3

[V_{DD} = 1.7V to 2.4V, Ta = –40 to +85°C]

Parameter		Signal	Symbol	Condition	Specified value		Unit
					Min.	Max.	
Address hold time Address setup time		A0	t_{AH6} t_{AW6}		0 0	— —	ns
System write cycle time System read cycle time		E	t_{WCYC6} t_{RCYC6}		400 600	— —	
Data setup time Data hold time		D0 to D7	t_{DS6} t_{DH6}		40 20	— —	
Access time Output disable time			t_{ACC6} t_{OH6}	C_L=100pF	— 10	200 200	
Enable HIGH-pulse width	Read Write	E	t_{EWHR} t_{EWHW}		250 100	— —	
Enable LOW-pulse width	Read Write	E	t_{EWLR} t_{EWLW}		250 140	— —	

*1 This is in case of making the access by E, setting the $\overline{CS1}$ = LOW.
*2 This is in case of making the access by $\overline{CS1}$, setting the E = HIGH.
*3 The rise time and the fall time (tr & tf) of the input signals should be set to 15ns or less. When it is necessary to use the system cycle time at high speed, the rise time and the fall time should be so set to conform to $(tr+tf) \leq (t_{CVC6}-t_{EWLW}-t_{EWHW})$ or $(tr+tf) \leq (t_{CYC6}-t_{EWLR}-t_{EWHR})$.
*4 All the timing should basically be set to 20% and 80% of the "V_{DD}".
*5 t_{EWLW}, t_{EWLR} should be set to the overlapping zone where the $\overline{CS1}$ is on the LOW level (CS2 = HIGH level) and where the E is on the HIGH level.

(3) Serial interface

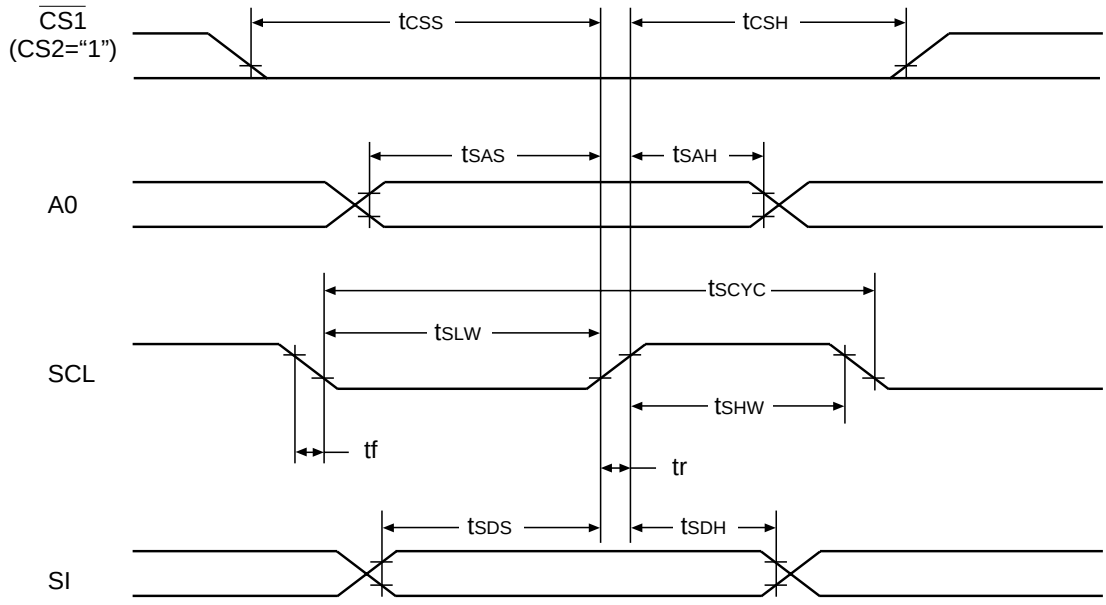


Figure 10.3

Table 10.3.1

[V_{DD} = 3.0V to 3.6V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value		Unit
				Min.	Max.	
Serial clock period	SCL	t_{SCYC}		100	—	ns
SCL HIGH pulse width		t_{SHW}		40	—	
SCL LOW pulse width		t_{SLW}		40	—	
Address setup time	A0	t_{SAS}		80	—	
Address hold time		t_{SAH}		80	—	
Data setup time	SI	t_{SDS}		20	—	
Data hold time		t_{SDH}		20	—	
CS-SCL time	CS	t_{CSS}		80	—	
		t_{CSH}		150	—	

Table 10.3.2

[V_{DD} = 2.4V to 3.0V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value		Unit
				Min.	Max.	
Serial clock period	SCL	t_{SCYC}		125	—	ns
SCL HIGH pulse width		t_{SHW}		50	—	
SCL LOW pulse width		t_{SLW}		50	—	
Address setup time	A0	t_{SAS}		100	—	
Address hold time		t_{SAH}		100	—	
Data setup time	SI	t_{SDS}		30	—	
Data hold time		t_{SDH}		30	—	
CS-SCL time	CS	t_{CSS}		100	—	
		t_{CSH}		200	—	

Table 10.3.3

[V_{DD} = 1.7V to 2.4V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value		Unit
				Min.	Max.	
Serial clock period	SCL	t_{SCYC}		154	—	ns
SCL HIGH pulse width		t_{SHW}		60	—	
SCL LOW pulse width		t_{SLW}		60	—	
Address setup time	A0	t_{SAS}		120	—	
Address hold time		t_{SAH}		140	—	
Data setup time	SI	t_{SDS}		40	—	
Data hold time		t_{SDH}		40	—	
CS-SCL time	CS	t_{CSS}		120	—	
		t_{CSH}		350	—	

*1. Input signal rise and fall time (tr, tf) must not exceed 15 ns.
*2. Timing is entirely specified with reference to 20% or 80% of V_{DD}.

(4) Display control output timing

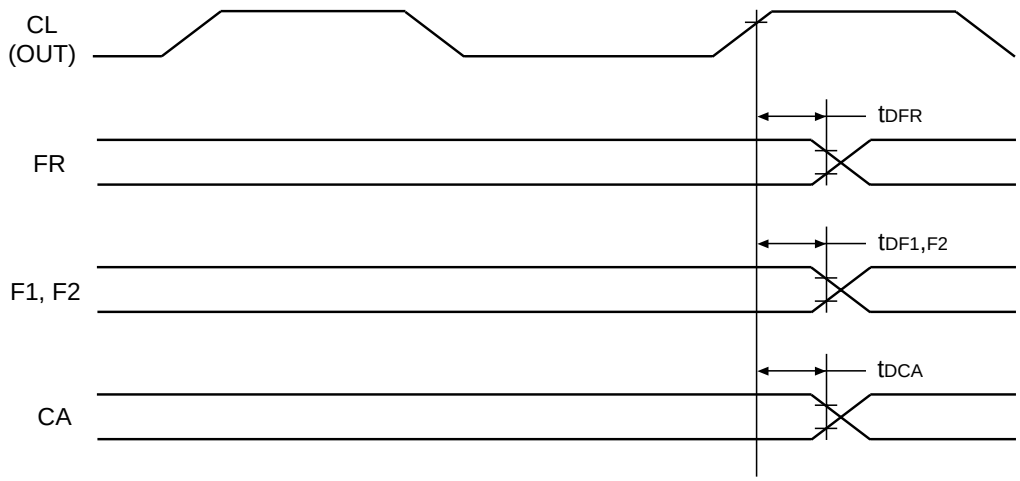


Fig. 10.4

Table 10.4.1

[V_{DD} = 3.0V to 3.6V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L = 50pF	—	125	312	ns
F1, F2 delay time	F1, F2	t_{DF1}, t_{F2}		—	125	312	ns
CA delay time	CA	t_{DCA}		—	125	312	ns

Table 10.4.2

[V_{DD} = 2.4V to 3.0V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L = 50pF	—	150	360	ns
F1, F2 delay time	F1, F2	t_{DF1}, t_{F2}		—	150	360	ns
CA delay time	CA	t_{DCA}		—	150	360	ns

Table 10.4.3

[V_{DD} = 1.7V to 2.4V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
FR delay time	FR	t_{DFR}	C_L = 50pF	—	225	514	ns
F1, F2 delay time	F1, F2	t_{DF1}, t_{F2}		—	225	514	ns
CA delay time	CA	t_{DCA}		—	225	514	ns

*1. Valid only in master operation
*2. Timing is entirely specified with reference to 20% or 80% of V_{DD}.

(5) Reset input timing

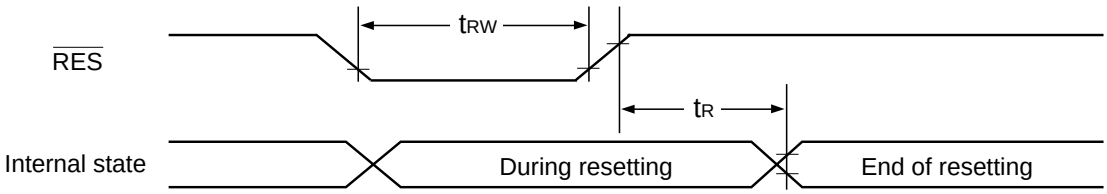


Fig. 10.5

Table 10.5.1

[V_{DD} = 3.0V to 3.6V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
Reset time		t_R		—	—	0.5	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW}		0.5	—	—	

Table 10.5.2

[V_{DD} = 2.4V to 3.0V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1.0	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1.0	—	—	

Table 10.5.3

[V_{DD} = 1.7V to 2.4V, Ta = –40 to +85°C]

Parameter	Signal	Symbol	Condition	Specified value			Unit
				Min.	Typ.	Max.	
Reset time		t_R		—	—	1.5	µs
Reset LOW pulse width	$\overline{RES}$	t_{RW}		1.5	—	—	

*1. Timing is entirely specified with reference to 20% or 80% of V_{DD}.

11. MPU INTERFACE (Reference Example)

The S1D15E06 series can be connected to the 80 series MPU and 68 series MPU. Use of a serial interface allows operation with a smaller number of signal lines.
You can expand the display area using the S1D15E06 series as a multi-chip. In this case, the IC to be accesses can be selected individually by the chip select signal. After initialization by the $\overline{RES}$ pin, each input terminal of the S1D15E06 series must be placed under normal control.

(1) 80 series MPU

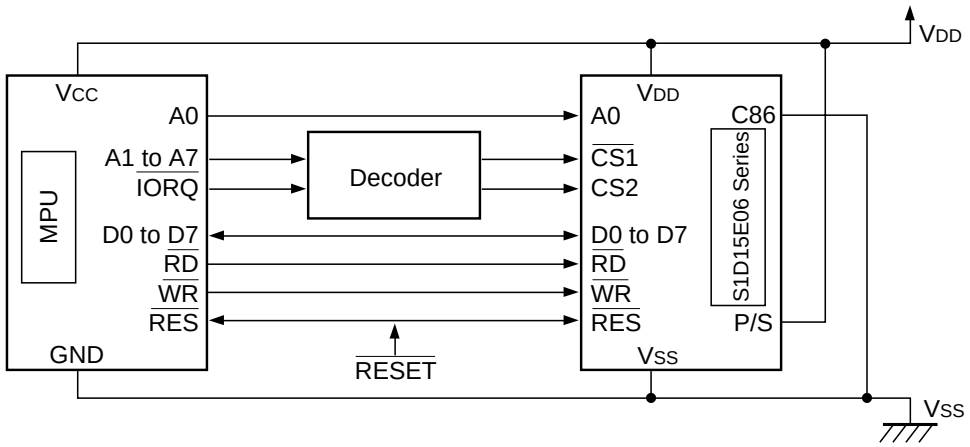


Fig. 11.1

(2) 68 series MPU

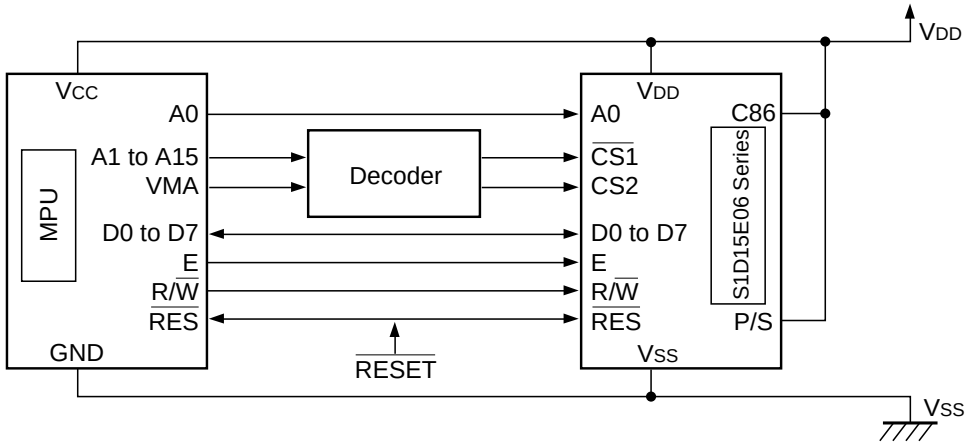


Fig. 11.2

(3) Serial interface

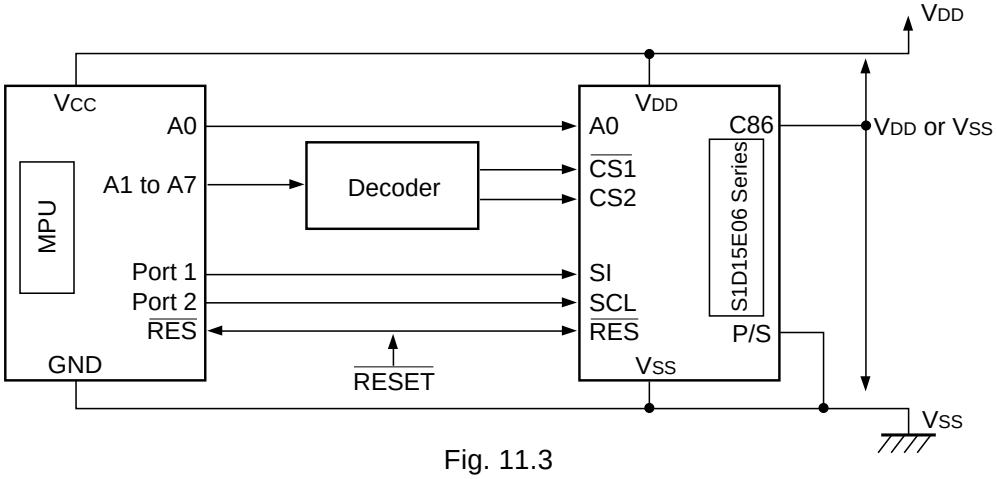


Fig. 11.3

12. CONNECTION BETWEEN LCD DRIVERS (Reference example)

You can easily expand the liquid crystal display area using the S1D15E06 series as a multi-chip. In this case, use the same model as the master and slave systems.

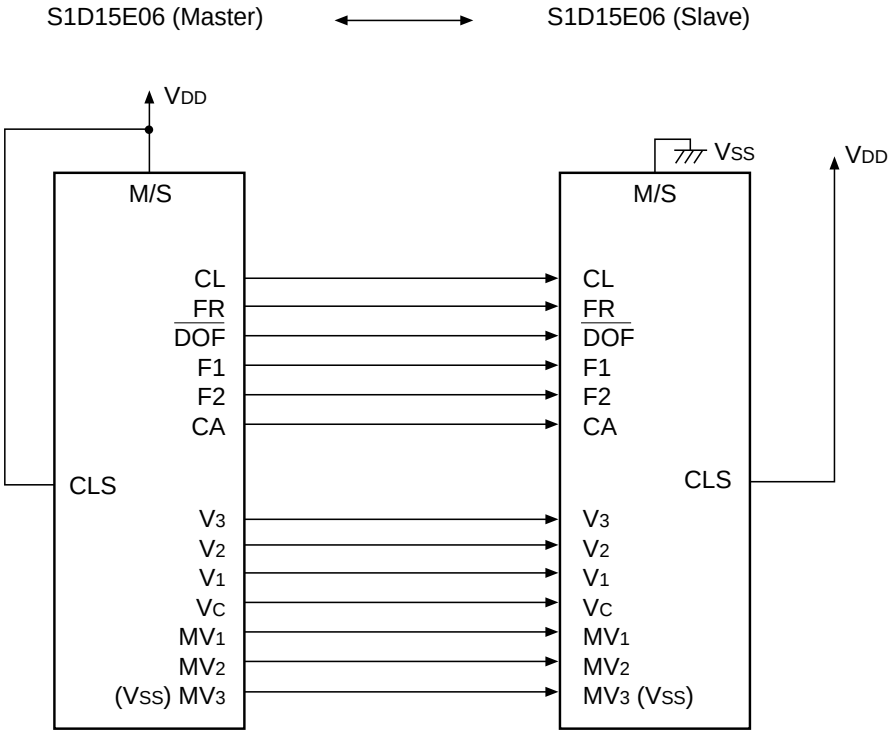


Fig. 12 Master/slave connection example (S1D15E06)

13. LCD PANEL WIRING (Reference example)

You can easily expand the liquid crystal display area using the S1D15E06 series as a multi-chip. In the case of multi-chip configuration, use the same models.

(1) Single chip configuration example

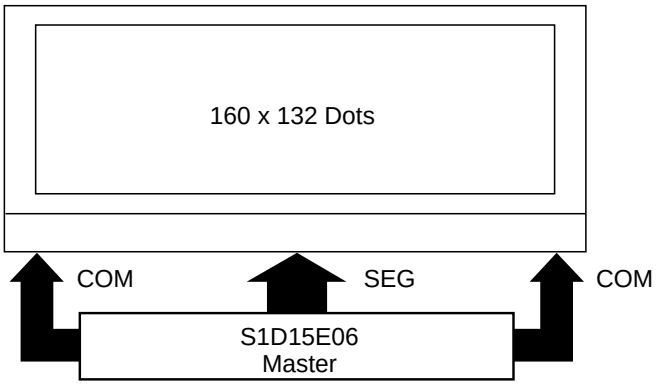


Fig. 13.1 Single chip configuration example (S1D15E06)

(2) Double chip configuration example

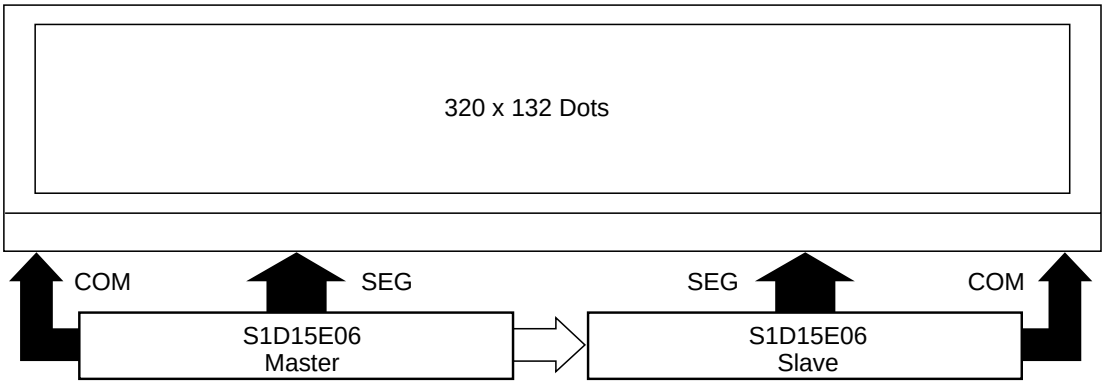
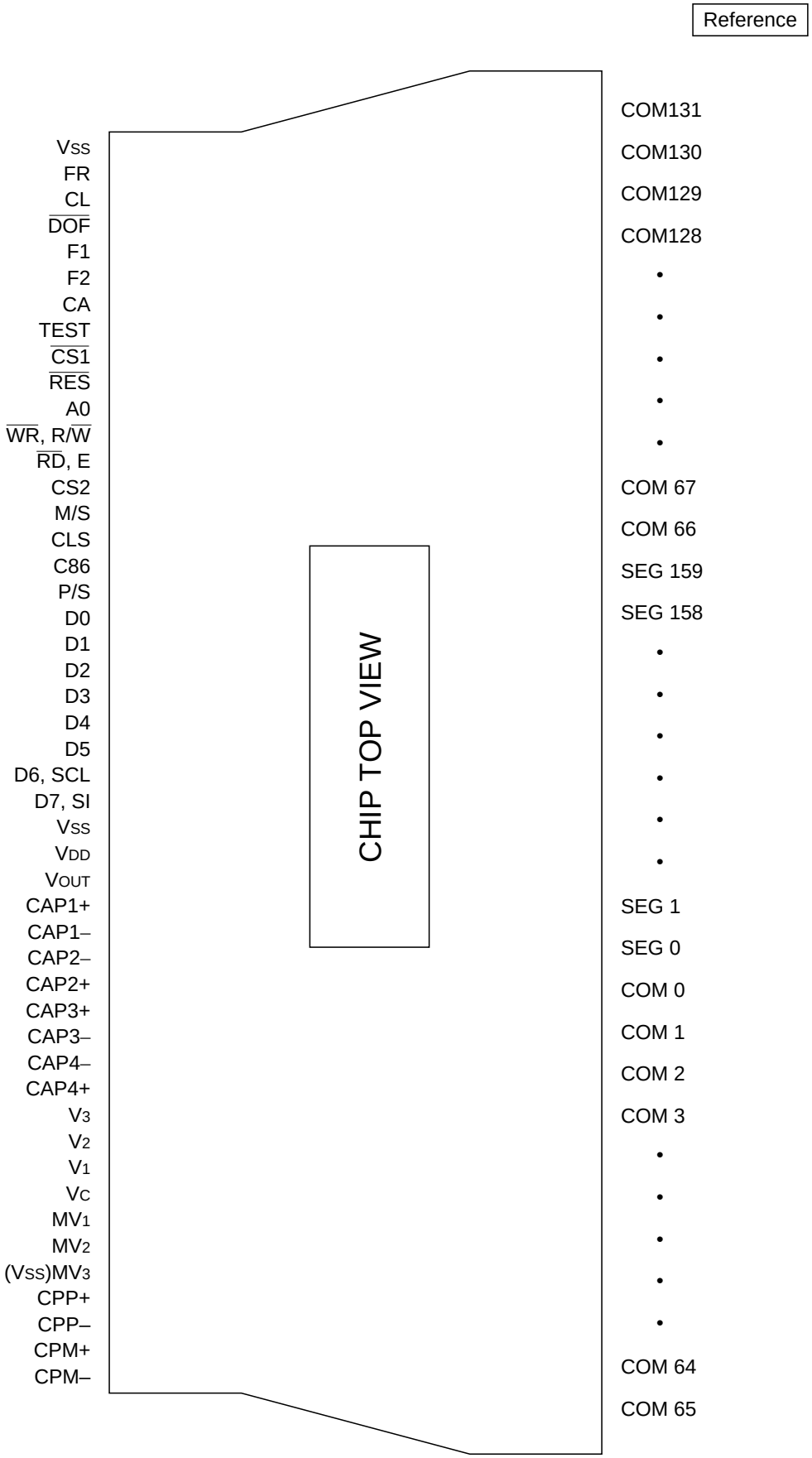


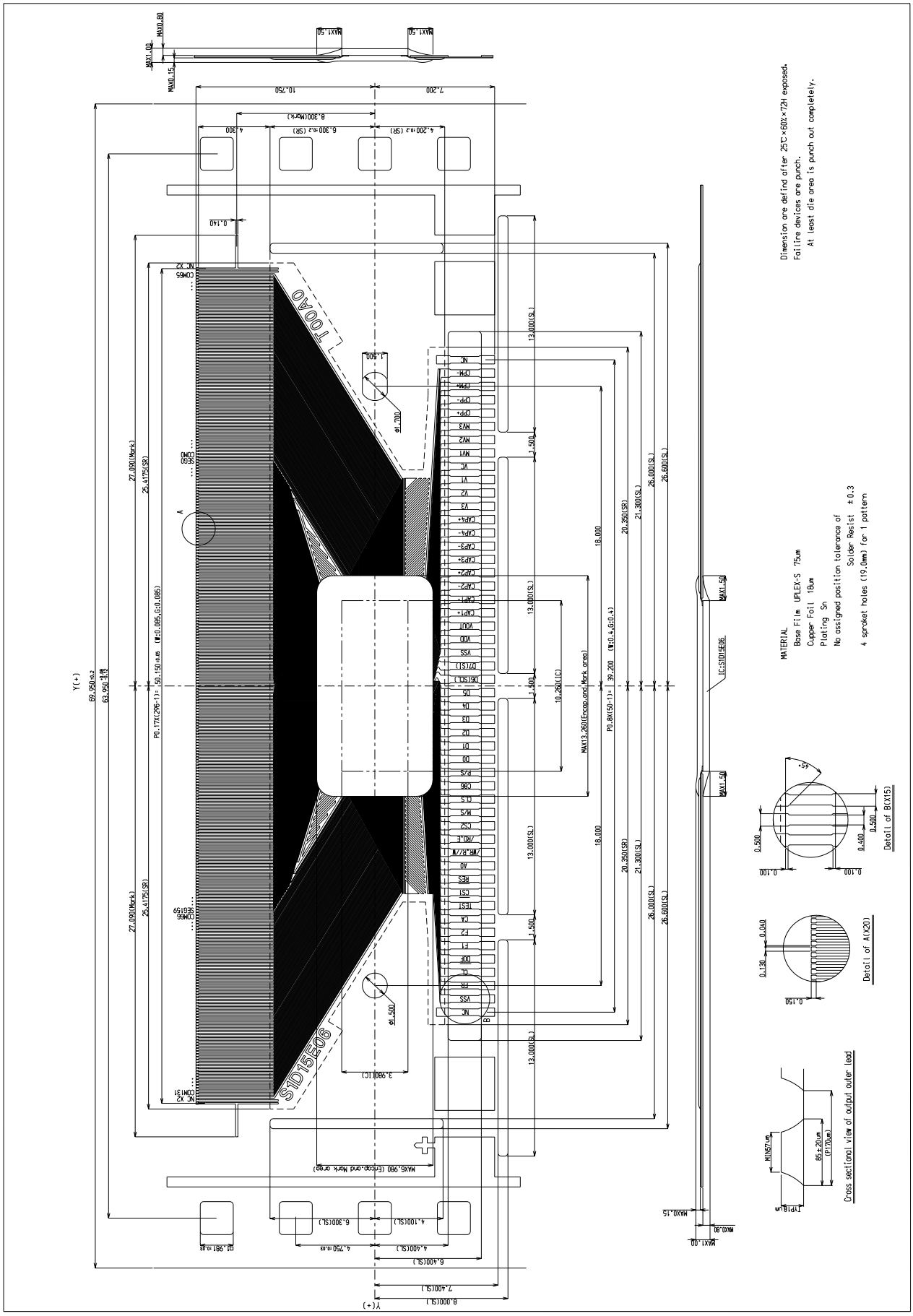
Fig. 13.2 Double chip configuration example (S1D15E06)

14. S1D15E06T00A*** TCP PIN LAYOUT

Note: This does not specify the TCP outside shape.



15. TCP DIMENSIONS (Reference example)



16. CAUTIONS

Cautions must be exercised on the following points when using this Development Specification:

1. This Development Specification is subject to change for engineering improvement.
2. This Development Specification does not guarantee execution of the industrial proprietary rights or other rights, or grant a license. Examples of applications described in This Development Specification are intended for your understanding of the Product. We are not responsible for any circuit problem or the like arising from the use of them.
3. Reproduction or copy of any part or whole of this Development Specification without permission of our company, or use thereof for other business purposes is strictly prohibited.

For the use of the semi-conductor,cautions must be exercised on the following points:

[Cautions against Light]

The semiconductor will be subject to changes in characteristics when light is applied. If this IC is exposed to light, operation error may occur. To protect the IC against light, the following points should be noted regarding the substrate or product where this IC is mounted:

(1) Designing and mounting must be provided to get a structure which ensures a sufficient resistance of the IC to light in practical use.
(2) In the inspection process, environmental configuration must be provided to ensure a sufficient resistance of the IC to light.
(3) Means must be taken to ensure resistance to light on all the surfaces, backs and sides of the IC