data sheet

*et*CSP® Package:

Amkor's *et*CSP® package is the first ball grid array capable of an extremely thin 0.5 mm maximum mounted height. This package can squeeze into applications requiring a thin form factor. The *et*CSP® package is constructed using conventional IC processing including standard wire bonding, molding and substrate infrastructure. The resulting package consists of one or two peripheral rows of 0.3 mm diameter solder balls to allow common SMT processing.

There are many advantages as a direct result of the unique *et*CSP® design. One key advantage is the 0.5 mm mounted height of the package, the result of solder ball diameter and thin core laminate substrate. Every other aspect of the package, die, wires and moldcap are within the dimensions of the substrate and solderballs. Another direct result of the *et*CSP® design is the superior moisture resistance. Since die attach materials are not used to mount the die, there is reduced capability to trap moisture. Therefore, popcorn induced delamination is reduced.

The *et*CSP® package can also be designed with the capability of stacking completely tested packages, i.e., packaged memory, into a single footprint on the motherboard. In this manner, two stacked *et*CSP™ packages can be tested before mounting and the combined height is less than 1.0 mm.

*et*CSP®

Features:

- Up to 176 ball count
- 7-12 mm body size
- Thinnest CSP available at 0.5 mm max mounted height
- JEDEC Level 1 Reliability to 260 °C reflow temperature
- Conventional process flow with proven wirebond technology
- Standardized footprints at 0.5 mm pitch
- Package stacking potential of tested packages
- Two stacked die potential

Thermal Performance:

12 x 12 mm body; 176 I/O; Typical 39 °C/W
Amkor's initial *et*CSP® packages are offered for low power applications. Higher thermal performance can be achieved by adding a heat spreader or heat sink to the die's exposed backside. In addition, future die-up configurations will provide a direct heat dissipation path into the product motherboard through the die backside.

Electrical:

	Min	Max
Inductance (nH)	0.735	1.546
Capacitance (pF)	0.176	0.319
Resistance (mOhms)	47.9	89.83

Package Dimensions:
7 x 7 mm body; 89 I/O; 0.3 mm ball diameter; 100 MHz

Reliability:

Package Level*:

- Moisture sensitivity — JEDEC Level 1 @ 260 °C
- Temp Cycle — -55° C/+125 °C, 1000 cycles
- Temp/Humidity — 85 °C/ 85% RH, 1000 hrs
- High Temp Storage — 150 °C, 1000 hrs
- PCT/HAST — 130 °C, 85% RH, 96 hrs

*Data for 12 x 12 mm body; 176 I/O; 7.62 mm DC die, 0.15 mm thick

Board Level:

- Thermal cycle — -55 °C / 125 °C 2 cycles / hour, 1000 cycles
- First failure 1100 cycles
- Lead free solder

Applications:

Amkor's *et*CSP® design makes this package type ideal for PCMCIA card applications, mini disk drives, thin wireless handsets, Flash or EEPROM memory and other portable products where vertical height is limited. Because of the unique design of the *et*CSP® package, stacking is easily achieved with proper substrate designs. This creates an opportunity to multiply memory capacity without increasing board area.

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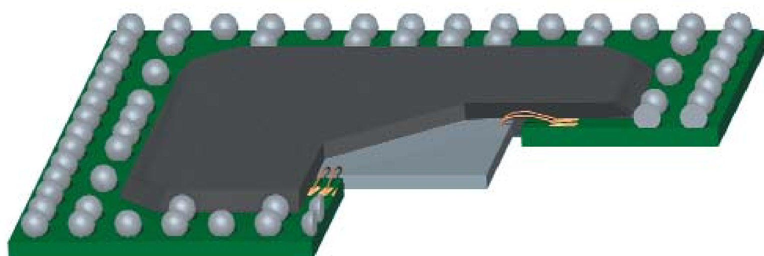
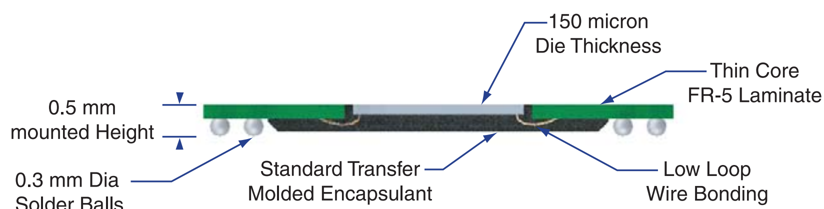
data sheet

*et*CSP®

Cross-section *et*CSP®





Process Highlights

Die thickness (max)	150 µm
Wire bonding	Standard; low loop
Die attach adhesive	Not required
Package marking	Laser

Standard Materials

Package substrate	Thin core FR5 or equivalent
Au wire	20 µm diameter
Encapsulant	Standard EMC
Solder balls	0.3 mm dia. 63 Sn/37Pb & SnAgCu
Top coating	Conductive epoxy (option)

Shipping

*et*CSP® packages are shipped in JEDEC trays or tape and reel if final electrical testing is performed.

Daisy Chain Availability

*et*CSP® 80, 7 x 7, 0.5 mm ball pitch
*et*CSP® 176, 12 x 12, 0.5 mm ball pitch

Configuration Options:

etCSP® Standard Package Offering (units in mm)

Package Size	Max Die Size	Max I/O (2 rows)
7 x 7	3.6	96
8 x 8	4.6	112
9 x 9	5.6	128
10 x 10	6.6	144
11 x 11	7.6	160

*Maximum die size may increase +1 mm.

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