GR-909 TESTING WITH THE Si321X PROSLIC®

1. Introduction

This document describes how line fault testing (such as GR-909) may be implemented using the Si321X family of ProSLIC devices. Demonstration code for each test is available.

2. GR-909 Metallic Loop Tests

The five metallic loop tests described by GR-909 are as follows:

1. ***Hazardous Potential Test***
   Under any condition, the following must be detected
   >50 V_{RMS} ac voltage from TIP-GND or RING-GND
   >135 V dc voltage from TIP-GND or RING-GND
2. ***Foreign Voltage Test***
   Under any condition, the following voltages not generated by the SLIC must be detected
   >10 V_{RMS} ac from TIP-GND or RING-GND
   >6 V dc from TIP-GND or RING-GND
3. ***Resistive Faults Test***
   Detect the following resistive line faults
   <150 kΩ TIP-RING, TIP-GND, or RING-GND
4. ***Receiver Off-hook Test***
   Distinguish between resistive fault <150 kΩ and an off-hook receiver
5. ***Ringing Equivalency Number Test***
   Determine the REN (Ringer Equivalency Number) of the terminating receiver is between 0.175 REN and 5 REN. Reject if outside that range.

Each of these tests can be implemented on the Si321x devices. Table 1 enumerates the test cases, the measurement method implemented, and the failing criteria.

Table 1. GR-909 Metallic Loop Tests

GR-909 Test	Test Description	Linefeed State	Measurement	Failure Criteria
1	Hazardous Potential	OPEN	V_{TIP} and V_{RING}	> 50 Vrms ac > 135 V dc
2	Foreign Voltage	OPEN	V_{TIP} and V_{RING}	> 10 Vrms ac > 6 V dc
3	Resistive Faults	TIP-OPEN, RING-OPEN	R_{TG}, R_{RG}, R_{TR}	>150 kΩ
4	Offhook	TIP-OPEN	R_{TR}	Detect/No-detect
5	REN	RINGING	PQ2	> 5 REN

3. Tests 1 & 2: Hazardous Potential and Foreign Voltages

These tests employ the same measurement technique; so, they can be implemented as a single test to save time, assuming that the source of the hazardous potential is always foreign (not generated by the SLIC). The exception would be if the user implements high-voltage ringing on a short loop, which may result in a ring signal that delivers >50 V_{RMS} to the load and/or a dc potential >135 V between ring bursts. The user must be cognizant of this possibility.

The dc voltage on TIP and RING can be directly read from Direct Registers 80 and 81 while in the OPEN linefeed state; however, in the presence of a foreign ac voltage, it is very inaccurate. If a large enough sample set is taken at timed intervals to reconstruct an ac voltage at a minimum of 20 Hz, both the ac and dc voltages are quantified.

If N samples are taken at fixed intervals, the ac and dc voltages on TIP (or RING) may be calculated as follows:

$$V_{TIP.DC} = \frac{1}{N} \sum_{n=0}^{N-1} V_{TIP}(n)$$

Equation 1.

$$V_{TIP.AC} = \sqrt{\frac{1}{N} \sum_{n=0}^{N-1} (V_{TIP}(n) - V_{TIP.DC})^2}$$

Equation 2.

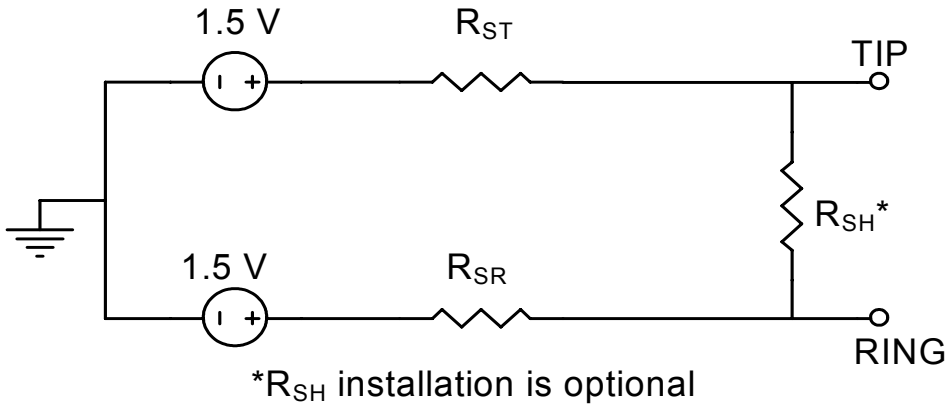

Figure 1. Si321X OPEN Linefeed State DC Equivalent Circuit

Refer to the demonstration code for an example of implementing ac voltage measurement.

4. Test 3: Resistive Faults

Since the small change in loop or longitudinal currents introduced by high impedance line faults may be too small to detect with the Si321x current monitoring, the large source impedance of the open terminal in the TIP-OPEN and RING-OPEN linefeed states can be utilized to force a large voltage change on the open terminal that can easily be detected. To measure resistive faults to GND (either TIP-GND or RING-GND), it is necessary to install the optional shunt resistor, RSH, to provide a small loop current reference. When a fault to GND is present on the OPEN terminal, the longitudinal current is altered, and the impedance may be calculated.

If R_{SH} is not installed, resistive faults between TIP and RING can still be measured. However, faults from TIP-GND or RING-GND must be detected using a less accurate method, which will only account for gross faults (<30 kΩ).

4.1. Condition 1: No Resistive Fault

If no resistive faults are present, the voltage on the TIP lead while in the TIP-OPEN linefeed state and the voltage on the RING lead while in the RING-OPEN linefeed state is said to be at the critical voltage. It is necessary to identify this because if a resistance is to be calculated as a function of the open terminal voltage, there are limiting voltage values that result in an infinite resistance calculation. Though an infinite resistance is a valid measurement, software applications need to avoid making a calculation with an infinite result. By first identifying the voltage in which there are no line faults present, this calculation can be avoided. An equation for the critical voltage will be derived in the following sections. In a no-fault loop (see Figure 2), the following equations apply:

$$V_{TIP} = 1.5\ V - R_{ST} \times I_{LOOP}$$

$$I_{LOOP} = \frac{V_{TIP} - V_{RING}}{R_{SH}}$$

$$V_{TIP} = \frac{1.5 \times R_{SH} + R_{ST} \times V_{RING}}{R_{ST} + R_{SH}}$$

where I_{LOOP} is the quiescent loop current flowing due to the shunt resistor added across TIP and RING; R_{ST} is the TIP source impedance, and R_{SH} is the resistor added to create the loop current. Table 2 shows the values for R_{ST}, R_{SR}, and R_{SH} for the applicable linefeed states and BOM options.

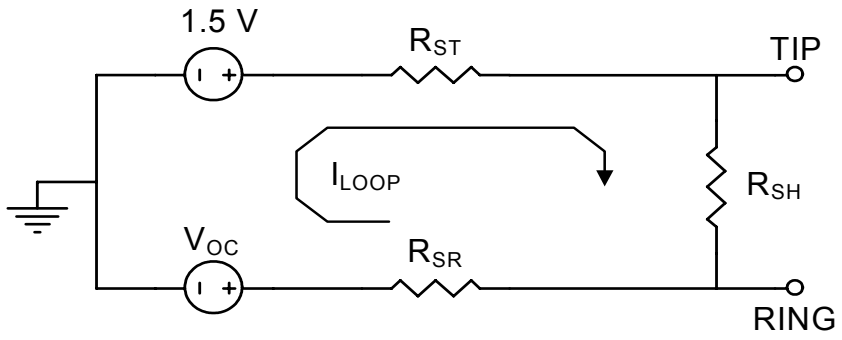

Figure 2. No-Fault TIP-OPEN DC Equivalent Circuit

Table 2. DC Source Resistances

Resistor	BOM Option	Tip-Open	Ring-Open	Open
R_{ST}	Standard	200 kΩ	160 Ω	200 kΩ
	High Voltage	340 kΩ	160 Ω	340 kΩ
R_{SR}	Standard	160 Ω	200 kΩ	200 kΩ
	High Voltage	160 Ω	340 kΩ	340 kΩ
R_{SH}	Standard	680 kΩ	680 kΩ	680 kΩ
	High Voltage	1 MΩ	1 MΩ	1 MΩ

4.2. Condition 2: TIP to RING Fault

If a resistive fault from TIP to RING (R_{TR}) is present (see Figure 3), the loop impedance is reduced; thus, the loop current, I_{LOOP}, increases, which results in a larger drop across R_{ST} (TIP source impedance) and a more negative voltage at the TIP terminal that can easily be detected.

From the voltages at TIP and RING, the resistive fault, R_{TR}, may be calculated from the following equation:

$$R_{TR} = \frac{R_{SH} \times R_{ST}(|V_{RING}| - |V_{TIP}|)}{R_{SH}(1.5 + |V_{TIP}|) - R_{ST}(|V_{RING}| - |V_{TIP}|)}$$

Equation 3.

Examining Equation 3, there is a single value for V_{TIP} in which the denominator is zero and R_{TR} is infinite. This is the critical voltage, V_{TIP_CRIT}. Solving the denominator for V_{TIP}, the critical voltage is expressed as follows:

$$V_{TIP\_CRIT} = \frac{R_{ST} \times |V_{RING}| - 1.5 \times R_{SH}}{R_{SH} + R_{ST}}$$

Equation 4.

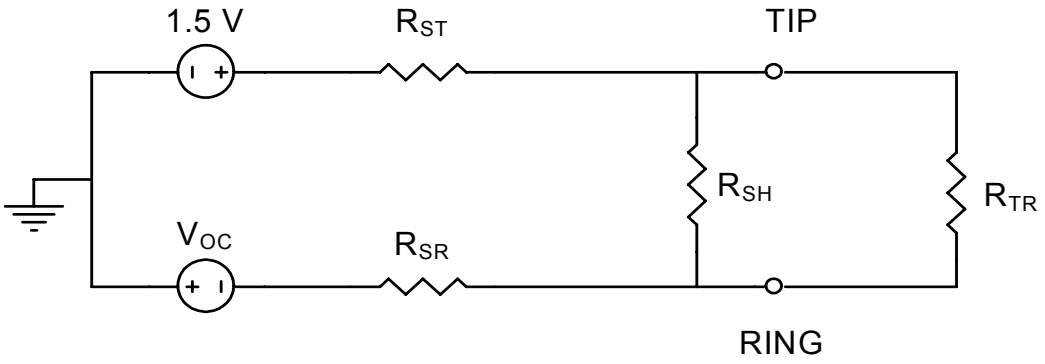

Figure 3. TIP-OPEN Linefeed State with TIP to RING Resistive Fault

If R_{SH} is not installed, a resistive fault present between TIP and RING will provide enough loop current to cause the voltage on the TIP lead to drop. Since all of the loop current passes through the resistive fault, R_{TR}, the equation for R_{TR} becomes as follows:

$$R_{TR} = \frac{R_{ST}(|V_{RING}| - |V_{TIP}|)}{1.5 + |V_{TIP}|}$$

Equation 5.

4.3. Condition 3: TIP to GND Fault

Resistive faults from TIP to GND are also detected in the TIP-OPEN linefeed state. In this case, the resistive fault from TIP to GND (R_{TG}) reduces the longitudinal current through R_{ST} (see Figure 4); thus, a more positive voltage is present at the TIP terminal. Equation 6 describes R_{TG} as a function of the TIP and RING voltages. Note that the denominator is the same as in the R_{TR} calculation; so, the same critical voltage applies.

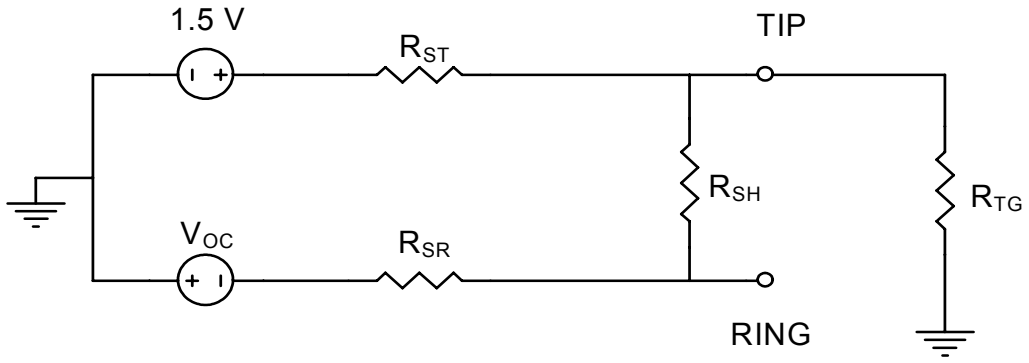

Figure 4. TIP-OPEN Linefeed State with TIP to GND Resistive Fault

From the voltages measured at TIP and RING, the resistive fault from TIP to GND may be expressed as follows:

$$R_{TG} = \frac{-|V_{TIP}| \times R_{ST} \times R_{SH}}{R_{SH}(1.5 + |V_{TIP}|) - R_{ST}(|V_{RING}| - |V_{TIP}|)}$$

Equation 6.

If R_{SH} is not installed, a gross measurement of the impedance from TIP-GND may be made in the FORWARD ACTIVE linefeed state. By applying a high common-mode voltage to TIP and keeping the differential voltage to 0 V (V_{OC} = 0), a resistive fault will form a voltage divider along with the 160 Ω output impedance of the TIP lead in the FORWARD ACTIVE state (see Figure 5).

If the common mode voltage is high enough and R_{TG} is low enough, a detectable longitudinal current will result.

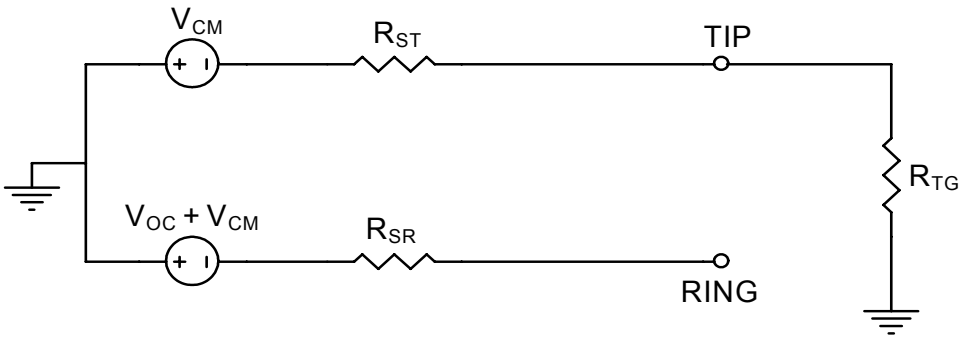

Figure 5. Forward Active State with TIP-GND Fault

Since V_{CM} is only limited by V_{BAT}, and the minimum detectable longitudinal current is 1.25 mA, the minimum detectable fault is as follows:

$$R_{TG} = \frac{|V_{BAT}|}{1.25\ mA} + R_{ST}$$

Equation 7.

For a typical V_{BAT} of –74 V, the minimum detectable resistive fault is ~60 kΩ.

4.4. Condition 4: RING to GND Fault

Resistive faults from RING to GND are also detected in the same manner as the TIP to GND case, except the line-feed is now in the RING-OPEN state (see Figure 6). As before, the addition of the resistive fault, R_{TG}, results in an increased voltage at the RING terminal.

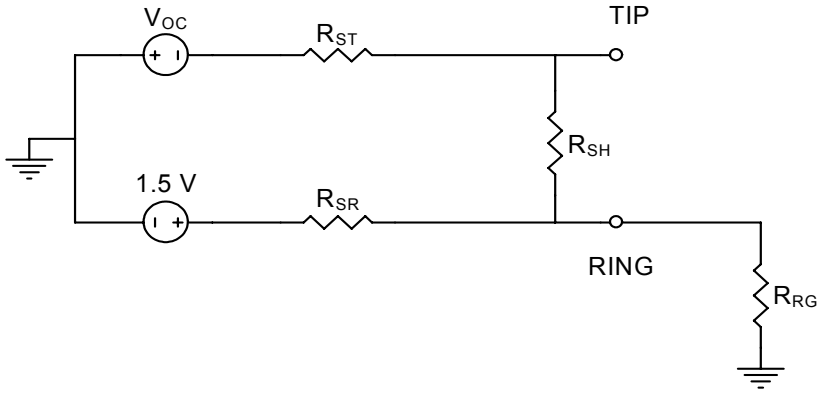

Figure 6. RING-OPEN Linefeed State with RING to GND Resistive Fault

From the voltages measured at TIP and RING, the resistive fault from RING to GND may be expressed as:

$$R_{RG} = \frac{-|V_{RING}| \times R_{SR} \times R_{SH}}{R_{SH}(1.5 + |V_{RING}|) - R_{SR}(|V_{TIP}| - |V_{RING}|)}$$

Equation 8.

If R_{SH} is not installed, the RING-GND impedance is measured just as the TIP-GND impedance was measured (see Equation 7).

5. Test 4: Receiver Off-Hook Test

GR-909 requires that the SLIC be able to differentiate between an off hook handset and a resistive fault. The dc impedance presented to the SLIC by a typical telephone varies with applied voltage; therefore, this nonlinearity may be exploited to determine whether a telephone is present.

By measuring the TIP lead in the TIP-OPEN linefeed state at two V_{OC} settings, the two dc impedances R_{TR} (refer to Equation 3) may be compared. If these two measurements differ by more than ~50% and they are within the expected range, an off hook telephone may be present. If a resistive fault is present, the variation will be within the resistance measurement accuracy, typically 10–25%.

This test may be performed with or without R_{SH} installed. If R_{SH} is not installed, refer to Equation 5 to calculate R_{TR}.

5.1. Test 5: REN Test

The Si321X can detect relatively small capacitive loads on the line. Line capacitance can be measured by either measuring the time constant of a decaying voltage on RING when in the OPEN mode (single-slope conversion) or by detecting longitudinal current when a subthreshold ring signal is applied. From the measured loop capacitance, the REN load may be estimated to within ± 0.5 REN.

5.1.1. Single-Slope Conversion

After charging the RING lead to V_{RING} in the FORWARD ACTIVE linefeed state, if the linefeed state is switched to the OPEN state, the voltages between the TIP and RING leads will discharge through their series output resistance (see Figure 1). By measuring the time delay from V_{RING} = upper threshold to V_{RING} = lower threshold, the capacitance can be calculated and the REN load estimated. This is ideal for detecting very small REN loads.

Because high REN loads present such a large capacitance and, therefore, very large time constants, it may be more advantageous to implement a subthreshold ringing method. It is only recommended that the single-slope method be used for loads less than 0.75 REN.

5.1.2. Subthreshold Ringing Method

The best method for estimating REN load when the load is >0.75 REN is by applying a small amplitude ring signal to the line and correlating the power dissipated in the linefeed pullup (Q2) to a known REN load. This requires the user to calibrate his hardware/software to known 1, 3, and 5 REN loads. This calibration determines the slope and offset of a straight line that correlates the REN load to the Q2 power dissipation. Once calibrated, future measurements utilize curve fitting to estimate the REN load.

Figure 7 shows the relationship between Q2 power dissipation and an applied REN load for a typical Si321X hardware design. By calibrating the hardware and identifying two straight lines, REN can be measured with ~± 0.5 REN accuracy.

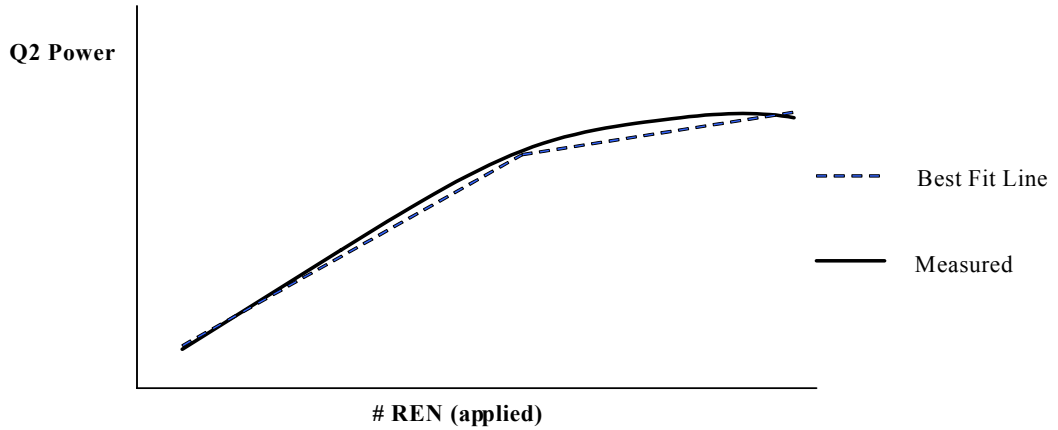

Figure 7. Typical Q2 Power vs. Applied REN Load

CONTACT INFORMATION

Silicon Laboratories Inc.

4635 Boston Lane
Austin, TX 78735
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email: ProSLICinfo@silabs.com
Internet: www.silabs.com

SILICON LABORATORIES