DATA SHEET

MOS INTEGRATED CIRCUIT

μPD16307

41bit DC-PDP ROW DRIVER ICs

DESCRIPTION

The uPD16307 is a ROW driver utilized high voltage Bi-CMOS process for DC plasma display panel. It consists of a 41bit bi-directional shift-register and high voltage NPN transitors. It operates 5V (CMOS input level) and drives High Voltage of 150V and High Current of 300mA. (Open collector output)

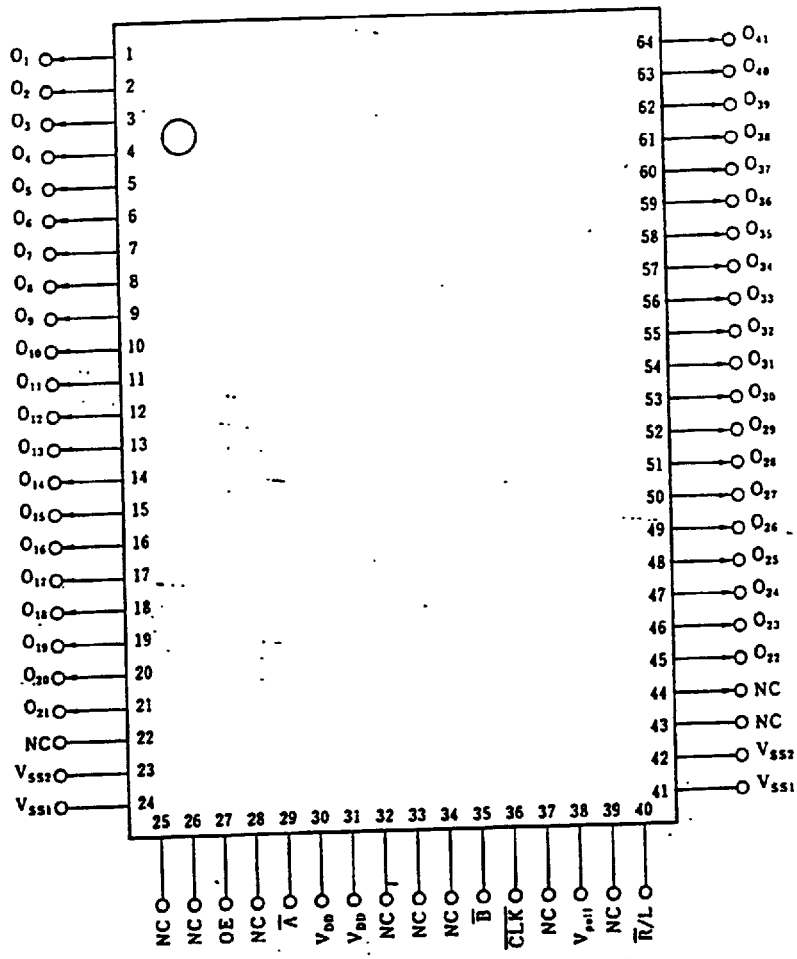
FEATURES

- High Voltage Transistor + CMOS structure
- +300mA Output Sink Current Capability
- Low Output Saturation Voltage (V_O=5V max. @I_O=220mA)
- 41bit Bi-directional Shift-register
- Low Power Consumption (I_{DD}=1mA max. Ta=-40 to +85°C)
- Symmetry pin configuration by three sided lead QFP.
- Wide Operating Temperature (-40 to +85°C)

ORDER INFORMATION

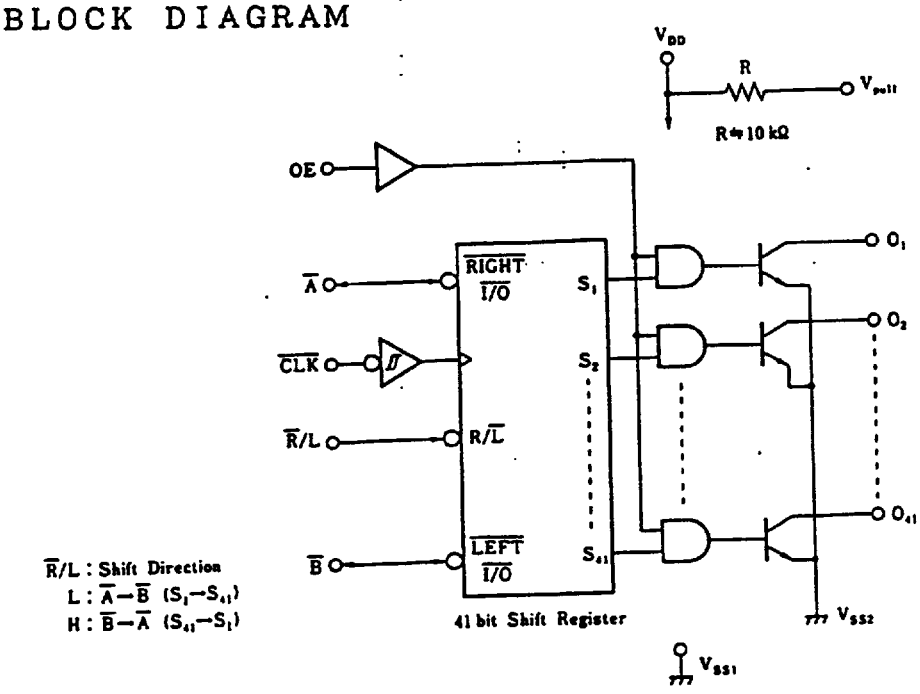
Part No.	Package	Quarity Level
uPD16307GF-3L9	80pin Plastic QFP (3 sided, 14 x 20)	Standard

PIN CONNECTION DIAGRAM (Top View)



Please connect outside between the same power supply pins.
Please open the No. 33 pin because of connecting lead frame.

BLOCK DIAGRAM



High Voltage Open Collector Outputs

PIN CONFIGURATION

SYMBOL	PIN NAME	PIN No.	EXPLANATION
CLK	Shift Clock Input	36	Data is read and shifted while CLK is going high level to Low level.
A	Right Data Input/Output	29	R/L=L ; A → O_1 → O_{41} → B R/L=H ; B → O_{41} → O_1 → A
B	Left Data Output/Input	35	
R/L	Shift Direction Control Input	40	
O_1-O_{41}	Driver Outputs	1 - 21, 45 - 64	High Voltage Outputs 150V +300mA max.
OE	Output Enabel Input	27	
V_{DD}	Logic Power Supply	30, 31	4.5V - 5.5V
V_{SS1}	Logic Ground	24, 41	Connect to system ground.
V_{SS2}	Power Ground	23, 42	
NC	Non Connect	22, 25, 26, 28, 32 33, 34, 37, 39, 43 44	Please open the No. 33 pin.
V_{PULL}	Pull Up Level Output	38	This pin is connected VDD throuth the 10kΩ internaly.

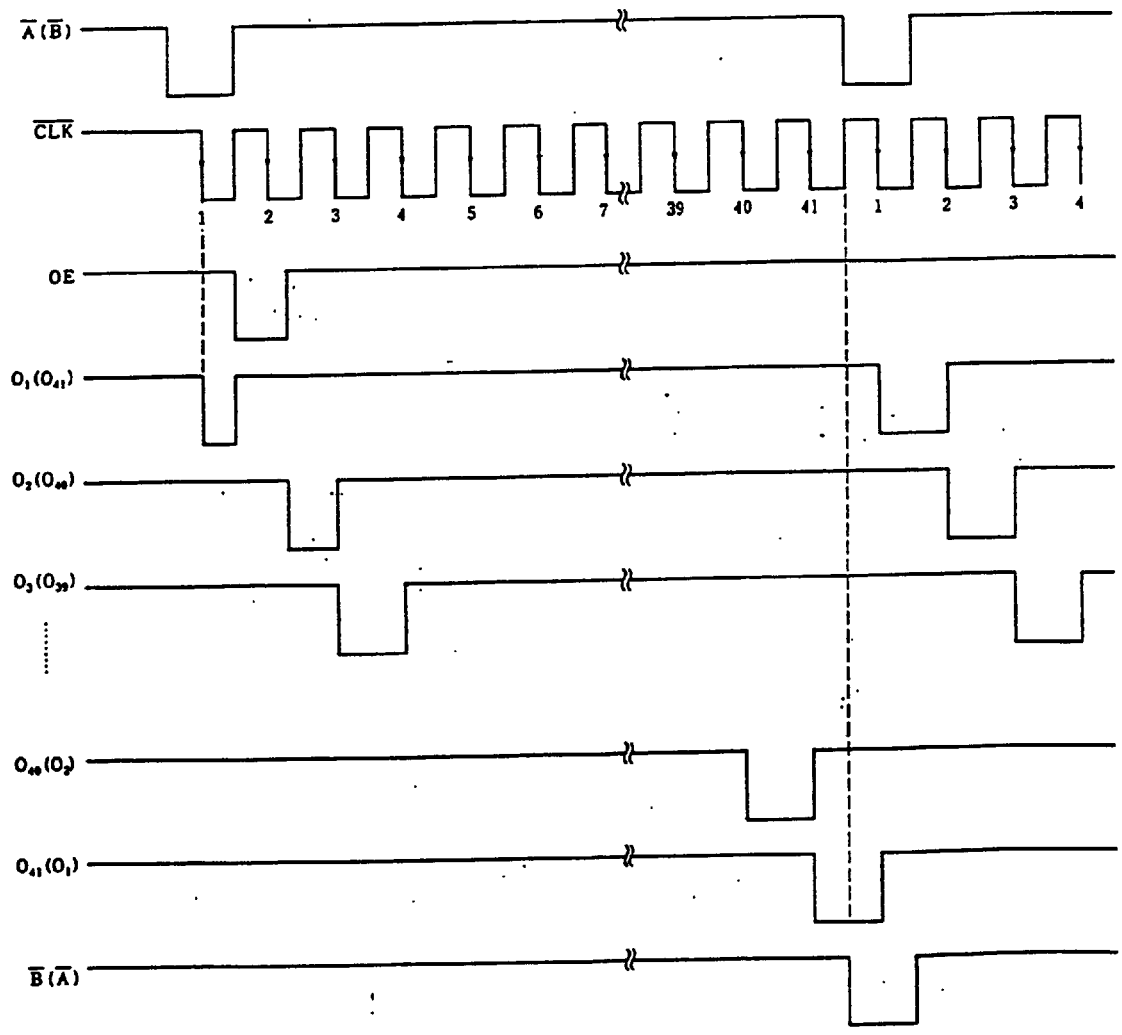
TRUTH TABLE1 (SHIFT-REGISTER)

INPUT		INPUT/OUTPUT		SHIFT-REGISTER STATUS
R/L	CLK	A	B	
L	↓	IN	OUT	RIGHT SHIFT (1 → 41)
L	↑			No CHANGE
H	↓	OUT	IN	LEFT SHIFT (41 → 1)
H	↑			No CHANGE

TRUTH TABLE2 (DRIVER)

DATA	OE	OUTPUT	REMARKS
×	L	Z	All Drivers are truned off.
H	H	Z	
L	H	L	

TIMING CHART



ABSOLUTE MAXIMUM RATINGS (Ta=25℃, Vss=0V)

Logic Power Supply Voltage	V_{DD}	−0.5 to +7.0	V
Input Voltage	V_I	−0.5 to VDD+0.5	V
Logic Output Voltage	V_{O1}	−0.5 to VDD+0.5	V
Driver Output Voltage	V_{O2}	−0.5 to 150	V
Driver OFF State Break Down Voltage	V_{O2Z}	−0.5 to 180*	V
Maximum Turn ON Time	t_{ON}	100	μs
Maximum Driving Duty Cycle	Duty(max)	1/41	−
Driver Current	I_{O2}	300	mA
Power Dissipation/Package	P_D	1000**	mW
Operating Temperature	$T_{opt.}$	−40 to +85	℃
Storage Temperature	$T_{stg.}$	−65 to 150	℃

* Maximum duty cycle is 10us/16ms while V_{O2Z} is between 150V and 180V.
** For Ta above 25℃, derate linearly at the rate of -8mW/℃.

RECOMMENDED OPERATING CONDITIONS

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Logic Power Supply Voltage	V_{DD}	4.5	5.0	5.5	V	
High Level Input Voltage	V_{IH}	0.7V_{DD}		V_{DD}	V	
Low Level Input Voltage	V_{IL}	0		0.2V_{DD}	V	
Driver Output Voltage	V_{O2}	0		110	V	
Driver Output Current	I_{O2}			220	mA	

ELECTRICAL CHARACTERISTICS (Ta=-40 to +85℃, V_{DD}=4.5 to 5.5V, V_{SS}=0V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
High Level Output Voltage	V_{OH1}	0.9V_{DD}			V	Logic Output, I_{OH1}=-1mA
Low Level Output Voltage	V_{OL1}			0.1V_{DD}	V	Logic Output, I_{OL1}=1mA
Low Level Output Voltage	V_{OL2}		3.0	5.0	V	O_1-O_{41}, I_{OL2}=220mA
Output Leakage Current	I_{TL1}			10	μA	O_1-O_{41} (Each Output) V_{O2}=110V, OE=0V
Output Leakage Current	I_{TL2}			41	μA	O_1-O_{41} (Total) V_{O2}=110V, OE=0V
Input Current	I_I			±1	μA	V_I=V_{DD} or V_{SS}
High Level Input Voltage	V_{IH}	0.7V_{DD}			V	
Low Level Input Voltage	V_{IL}			0.2V_{DD}	V	
Hysterisis Voltage Width	V_H	0.3	0.6	1.0	V	CLK
Quiescent Supply Current	I_{DD}			100	μA	Ta=25℃
				1.0	mA	Ta=-40 to +85℃

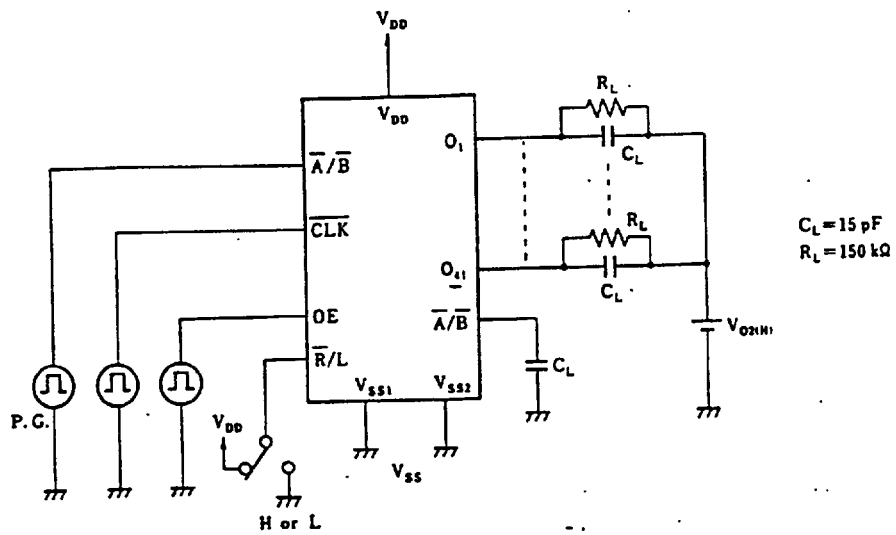
SWITCHING CHARACTERISITICS (Ta=-40 to +85°C, V_{DD}=4.5 to 5.5V, $V_{O2(H)}$=100V, C_L=15pF, R_L=150kΩ)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Propagation Delay Time	t_{PHL1}	10	120	400	ns	CLK to A/B (Serial Output)
	t_{PLH1}	10	120	400	ns	
	t_{PZL2}		120	520	ns	CLK to O_1-O_{41}
	t_{PLZ2}		1.1	3.5	us	
	t_{PZL3}		35	120	ns	OE to O_1-O_{41}
	t_{PLZ3}		1.1	3.5	us	
Output Rise Time	t_{TLZ}		18	30	us	O_1-O_{41}
Output Fall time	t_{TZL}		35	100	ns	
Maximum Clock Frequency	f_{max}	1.2	6		MHz	Duty Cycle=50%
Input Capacitance	C_I		10	15	pF	Ta=25°C

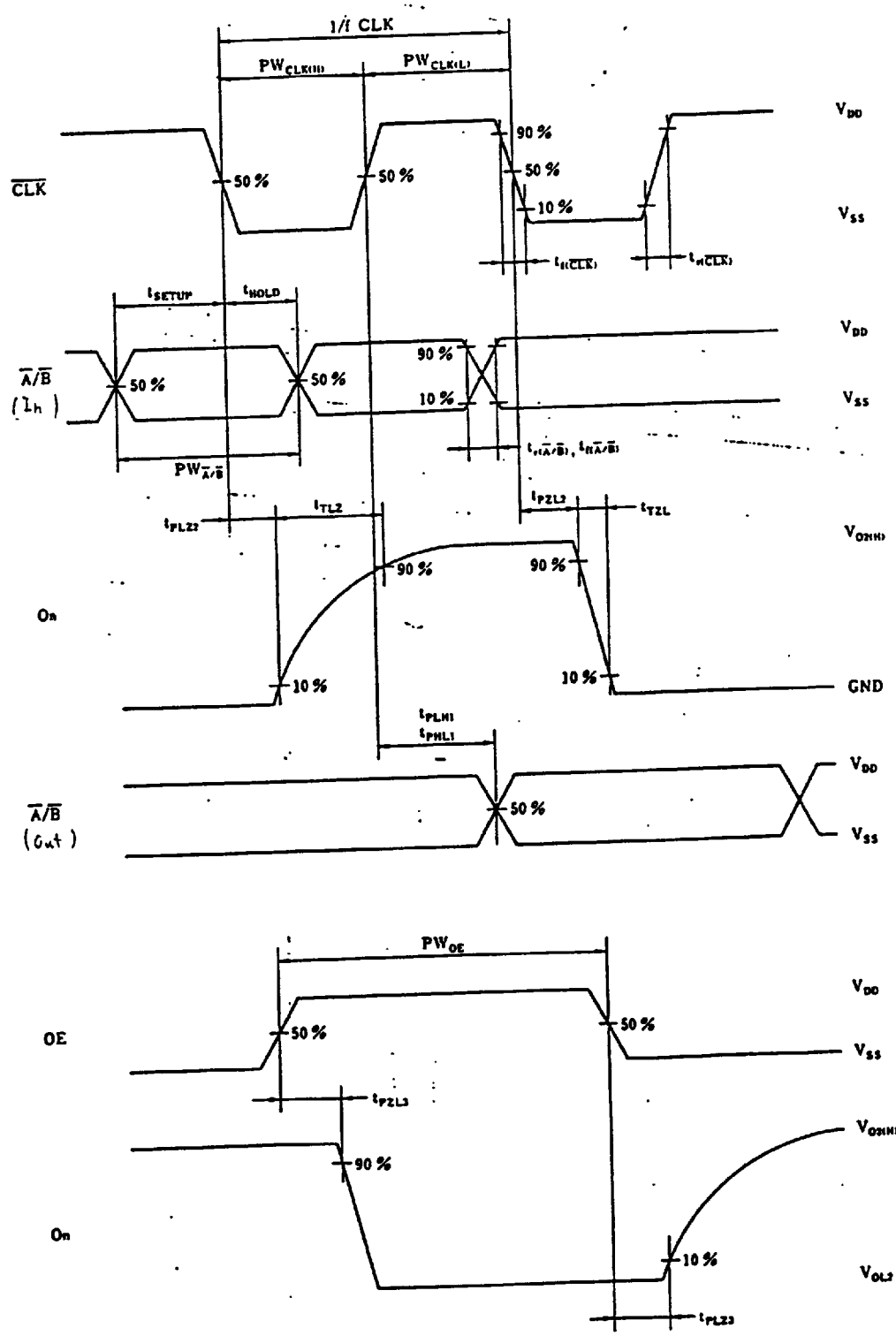
TIMING REQUIREMENT CONDITION (Ta=-40 to +85°C, VDD=4.5 to 5.5V)

ITEM	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Clock Pulse Width	PW_{CLK}	300			ns	
OE Pulse Width	PW_{OE}	1.2			us	
Data Set Up Time	t_{SETUP}	0			ns	
Data Hold Time	t_{HOLD}	200			ns	
Clock Pulse Rise Time	tr_{CLK}			500	ns	
Clock Pulse Fall Time	tf_{CLK}			500	ns	
Data Pulse Rise Time	$tr_{A/B}$			500	ns	
Data Pulse Fall Time	$tf_{A/B}$			500	ns	

SWITCHING TEST CIRCUIT

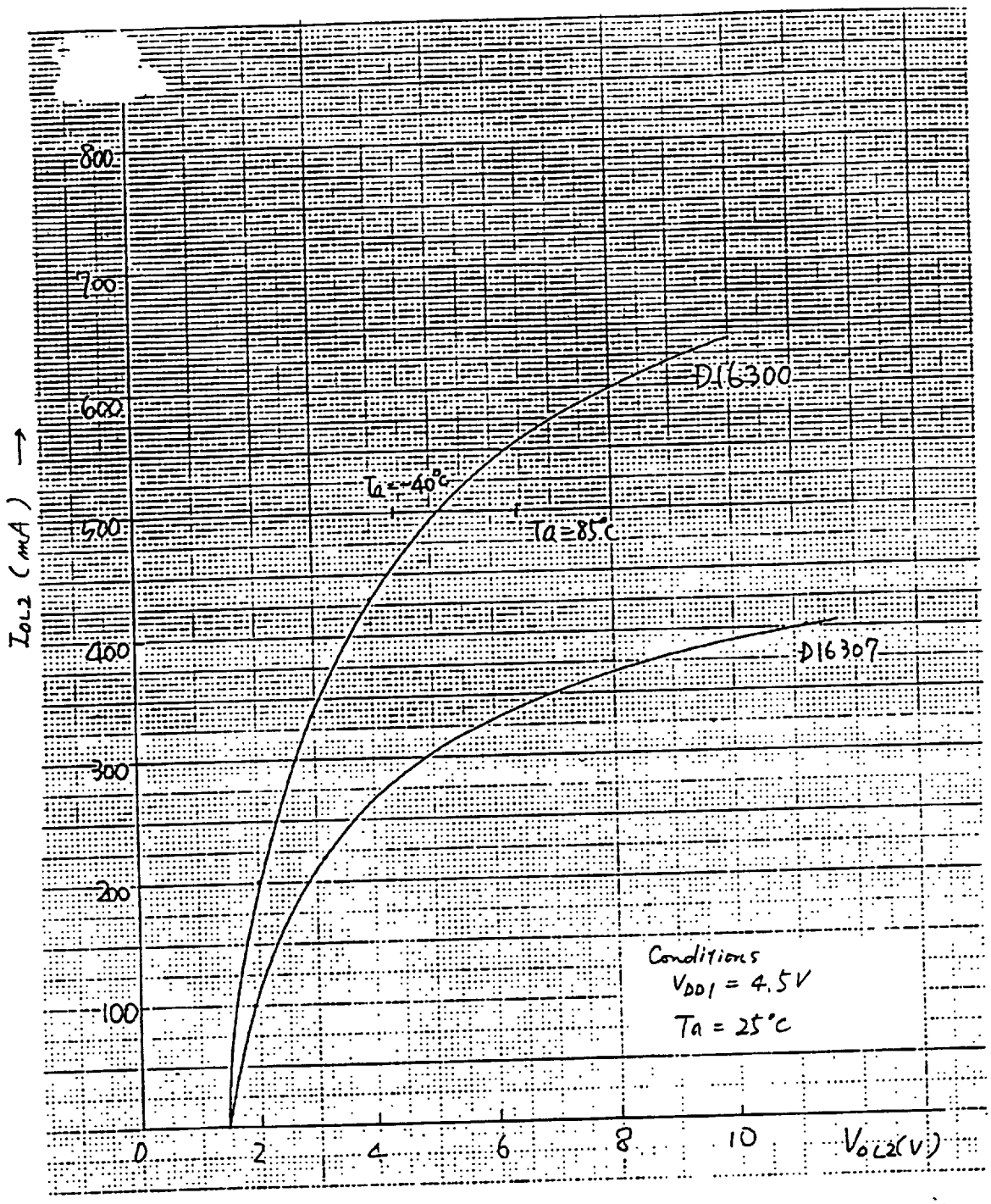


SWITCHING CHARACTERISTICS WAVEFORM



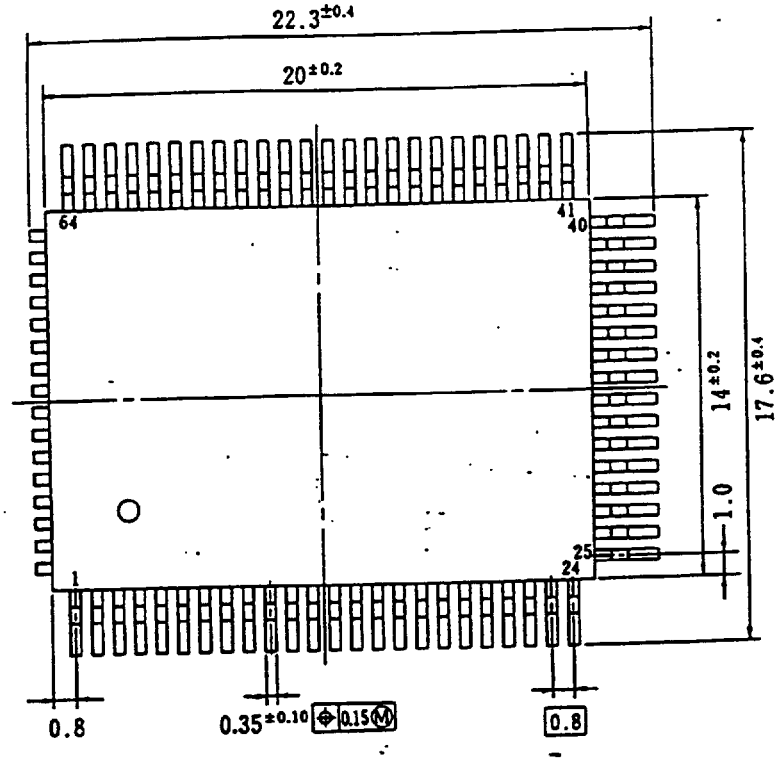
TYPICAL CHARACTERISTICS

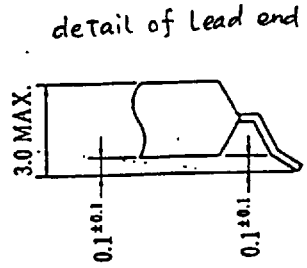
HIGH VOLTAGE OUTPUT VOLTAGE - OUTPUT CURRENT CURVE

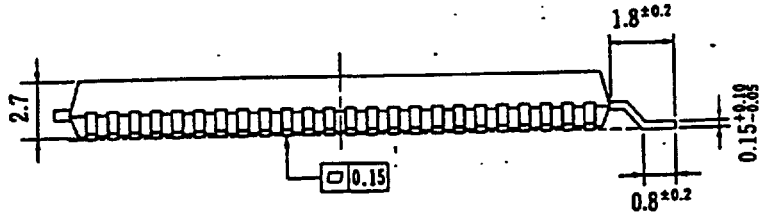


PACKAGE DIMENSIONS

80 PIN PLASTIC QFP (14 x 20 , 3 SIDED LEADS) UNIT (mm)







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