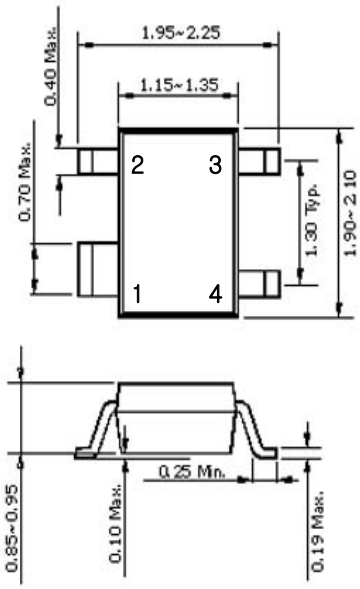
Preliminary Specification	**TMF3202Z**

N-Channel Dual-Gate MOSFET

☐ *Description*

The TMF3202Z is an enhancement type N-channel field-effect transistor. The source and substrate are interconnected. Internal bias circuits enable DC stabilization and a very good cross-modulation performance during AGC. Integrated diodes between the gates and source protect against excessive input voltage surges. The transistor has a SOT343 micro-miniature plastic package.

SOT343 **Unit in mm**



1. SOURCE **3. GATE 2**

2. DRAIN **4. GATE 1**

☐ *Features*

- Gain controlled amplifier with AGC
- Integrated gate protection diodes
- High AGC-range, high gain, low noise figure

☐ *Applications*

- Gain controlled input stage for UHF and VHF tuners
- Professional communications equipment

☐ *Absolute Maximum Ratings* (T_a = 25 ℃)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	10	V
Drain Current	I_D	30	mA
Gate 1 Current	I_{G1}	±10	mA
Total Power Dissipation	P_{tot}	200	mW
Storage Temperature	Tstg	-65 ~ 150	℃
Operating Junction Temperature	T_j	150	℃

Caution : **E**lectro **S**tatic **D**ischarge sensitive device, observe handling precaution

☐ DC Characteristics

(T_j = 25 ℃, unless otherwise specified)

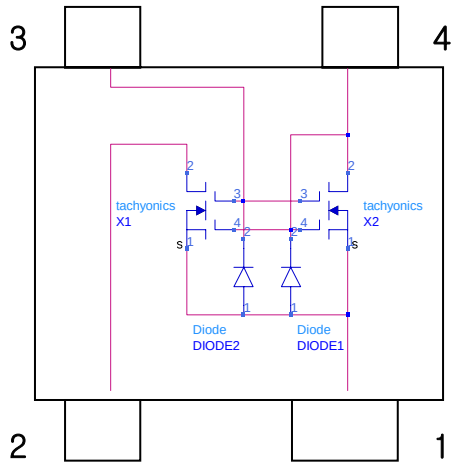
PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{G1-S}=V_{G2-S}=0; I_D=10㎂	10	–	V
Gate1-source breakdown voltage	$V_{(BR)G1-SS}$	V_{G2-S}=V_{DS}=0; I_{G1-S}=10㎃	6	10	V
Gate2-source breakdown voltage	$V_{(BR)G2-SS}$	V_{G1-S}=V_{DS}=0; I_{G2-S}=10㎃	6	10	V
Forward source-gate1 voltage	$V_{(F)S-G1}$	V_{G2-S}=V_{DS}=0; I_{S-G1}=10㎃	0.5	1.5	V
Forward source-gate2 voltage	$V_{(F)S-G2}$	V_{G1-S}=V_{DS}=0; I_{S-G2}=10㎃	0.5	1.5	V
Gate1-source threshold voltage	$V_{G1-S(th)}$	V_{DS}=5V; V_{G2-S}=4V; I_D=100㎂	0.3	1.0	V
Gate2-source threshold voltage	$V_{G2-S(th)}$	V_{DS}=5V; V_{G1-S}=4V; I_D=100㎂	0.3	1.2	V
Drain-source current	I_{DSX}	V_{G2-S}=4V; V_{DS}=5V; R_G=62㏀	8	16	㎃
Gate1 cut-off current	I_{G1-S}	V_{G1-S}=5V; V_{G2-S}=V_{DS}=0	–	10	nA
Gate2 cut-off current	I_{G2-S}	V_{G2-S}=5V; V_{G1-S}=V_{DS}=0	–	10	nA

☐ AC Characteristics

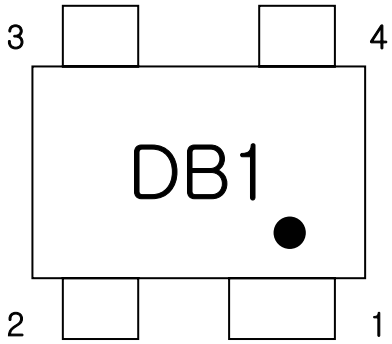
(Common source; T_a = 25 ℃, V_{G2-S} = 4V, V_{DS} =5V, I_D =12mA ;unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Forward transfer admittance	$\|y_{FS}\|$	Tj=25℃	25	30	40	mS
Input capacitance at gate1	C_{ig1-ss}	f=1MHz	–	1.7	2.2	pF
Input capacitance at gate2	C_{ig2-ss}	f=1MHz	–	3.3	–	pF
Output capacitance	C_{oss}	f=1MHz	–	0.9	–	pF
Reverse transfer capacitance	C_{rss}	f=1MHz	–	15	25	fF
Power gain	Gtr	f=200MHz; $Z_i = S_{11}^*$, $Z_o = S_{22}^*$	30	33	–	dB
		f=400MHz; $Z_i = S_{11}^*$, $Z_o = S_{22}^*$	27	30	–	dB
		f=800MHz; $Z_i = S_{11}^*$, $Z_o = S_{22}^*$	24	27	–	dB
Noise figure	NF	f=400MHz; $Z_i = S_{11\ opt(NF)}$	–	1.2	–	dB
		f=800MHz; $Z_i = S_{11\ opt(NF)}$	–	1.5	2.0	dB
Cross-modulation	X_{mod}	k=1%, fw=50MHz; funw=60MHz AGC = 0dB	90	–	–	dB㎶
		k=1%, fw=50MHz; funw=60MHz AGC = 10dB	–	92	–	dB㎶
		k=1%, fw=50MHz; funw=60MHz AGC = 40dB	100	105	–	dB㎶

☐ Equivalent circuit (Top view)



☐ Making



☐ Pin Configuration

PIN	DESCRIPTION
1	SOURCE
2	DRAIN
3	GATE2
4	GATE1

☐ Test circuit

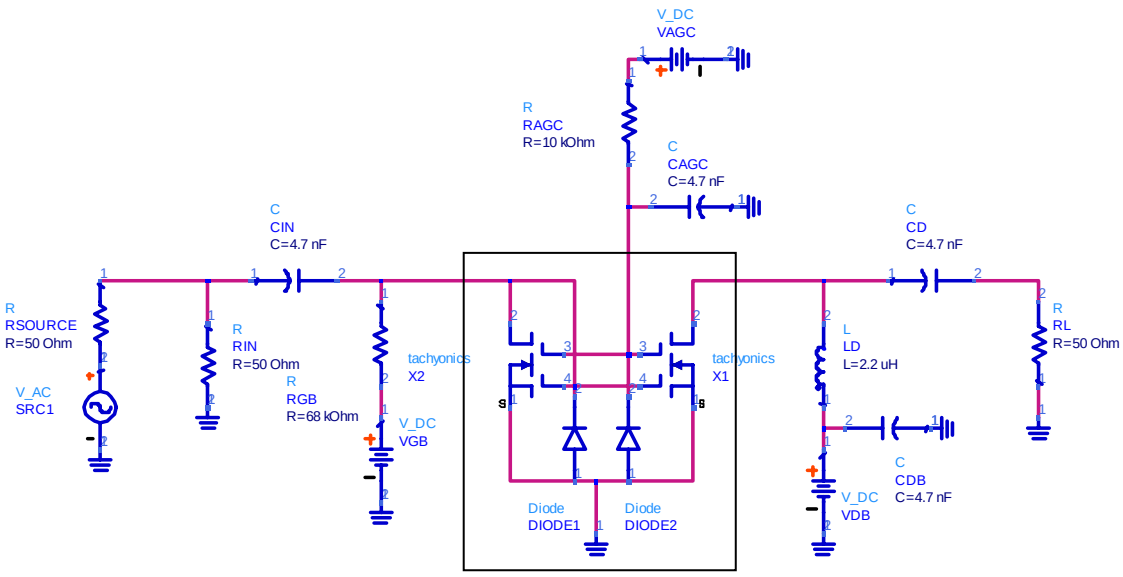
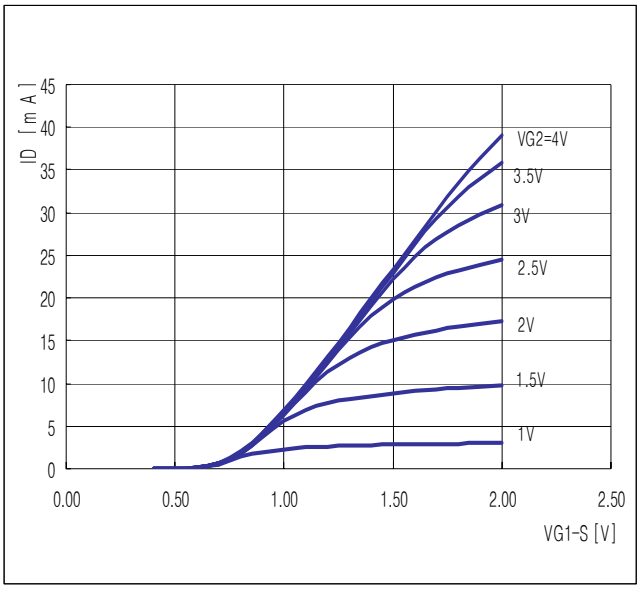


Fig1. Test Cross-modulation test set-up

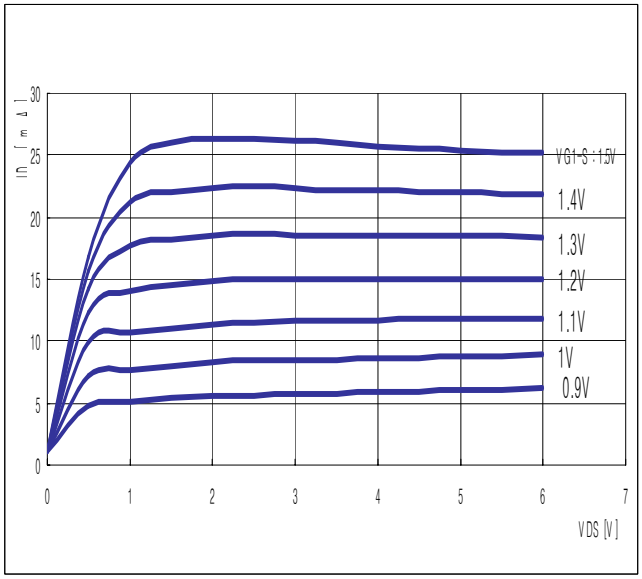
Scattering parameters

☐ Graphs



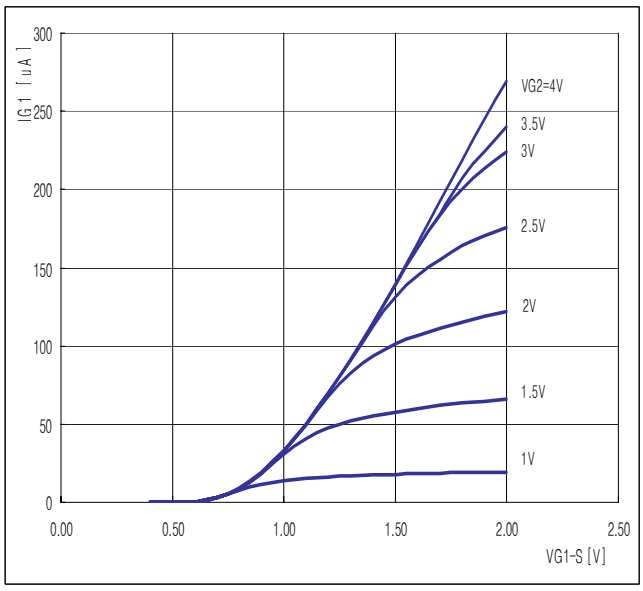
V_{DS} =5V, T_j = 25 ℃

Fig.2 Transfer characteristics



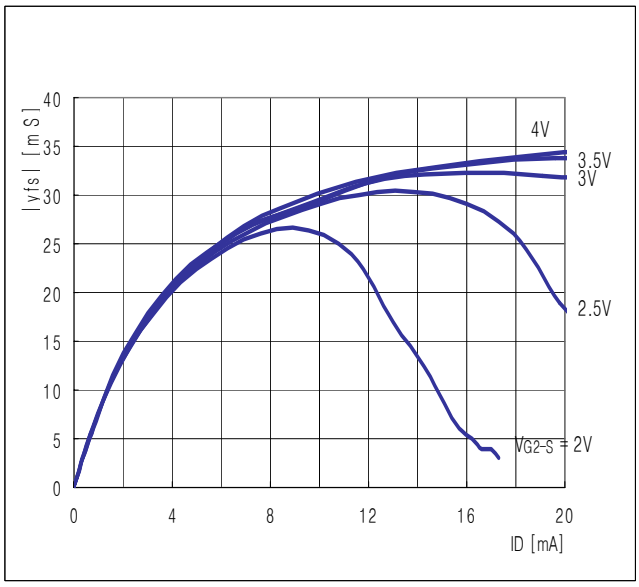
V_{G2-S} = 4V, T_j = 25 ℃

Fig3. Output characteristics



V_{DS} =5V, T_j = 25 ℃

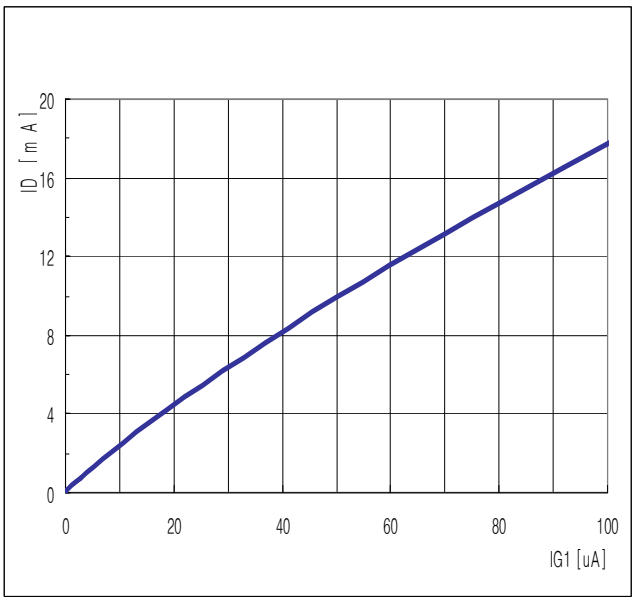
Fig.4 Gate1 Current as a function of gate1 Voltage



V_{DS} =5V, T_j = 25 ℃

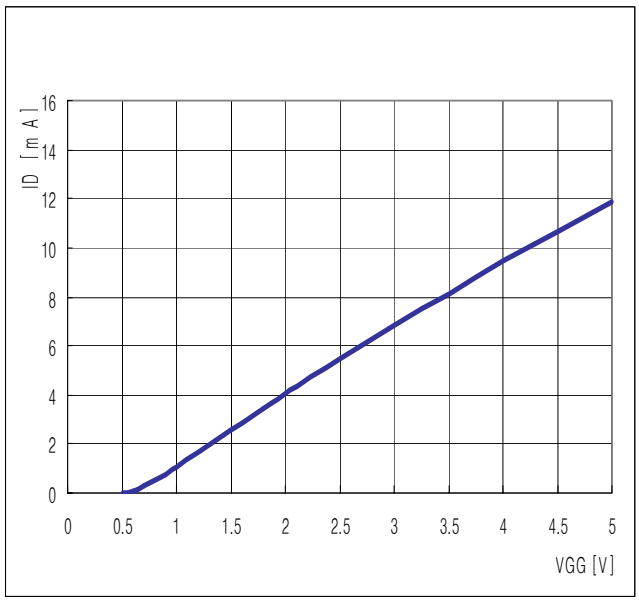
Fig5. Forward transfer admittance as a function of drain current

☐ Graphs



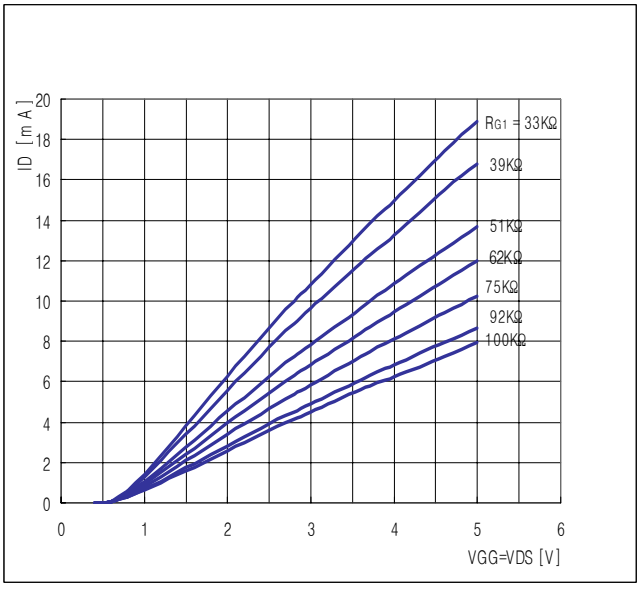
V_{DS}= 5V, V_{G2-S} = 4V, T_j = 25 ℃

Fig6. Drain current as a function of gate1 current



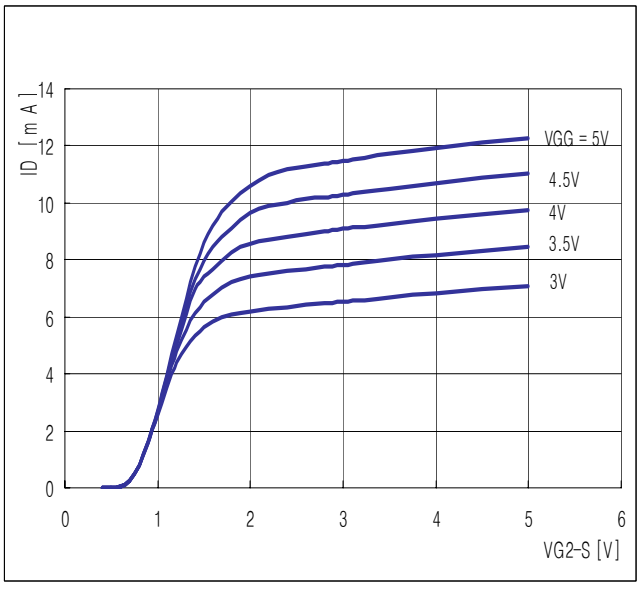
V_{DS}= 5V, V_{G2-S} = 4V, R_{GB}=62kΩ, T_j = 25 ℃

Fig7. Drain current as a function of gate1 supply voltage



V_{G2-S} = 4V, T_j = 25 ℃, R_{GB}= (Connected to VGG)

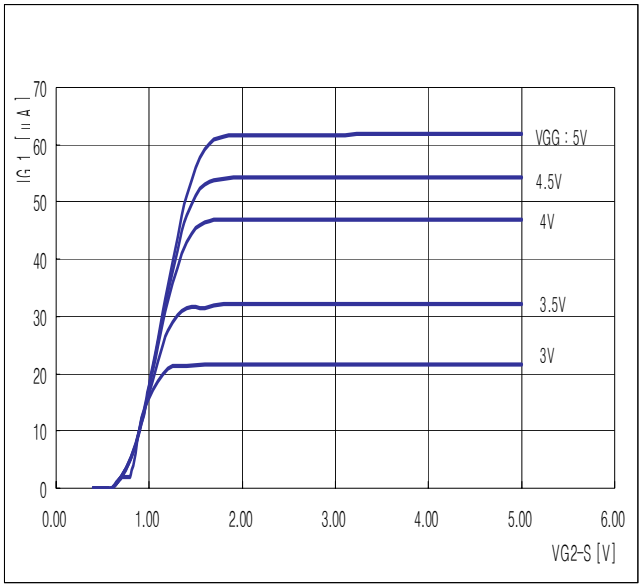
Fig8. Drain current as a function of gate1 and drain supply voltage ; see Fig1



V_{DS}= 5V, T_j = 25 ℃, R_{GB}=62kΩ

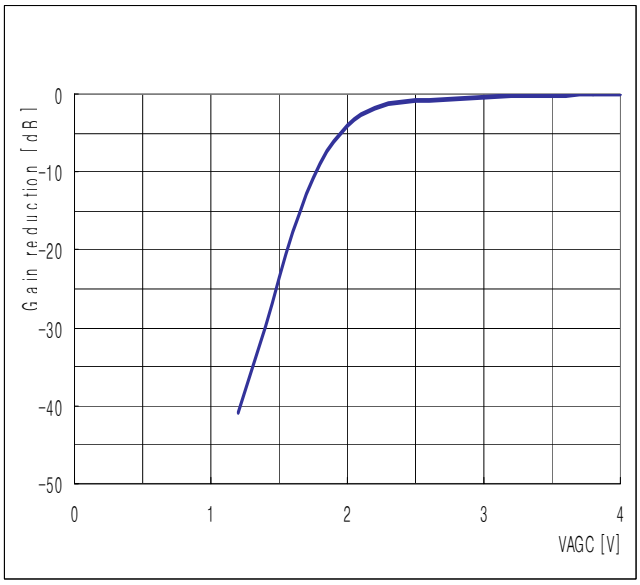
Fig9. Drain current as a function of gate2 voltage

☐ Graphs



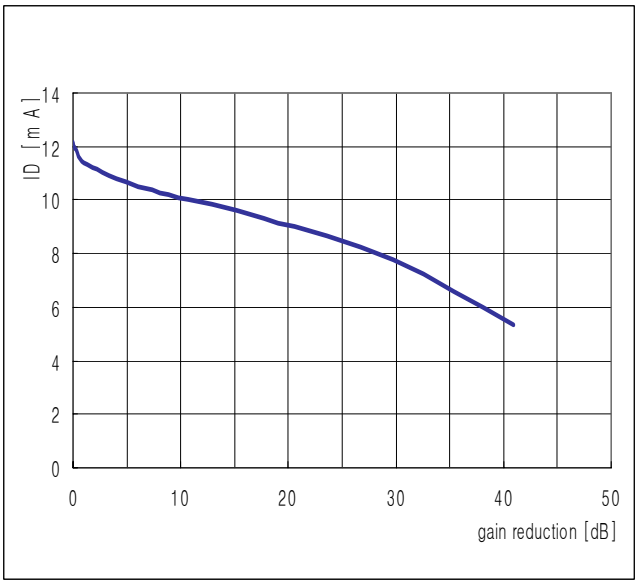
V_{DS}= 5V, R_{GB}= 62㏀, T_j = 25 ℃ ;Connected to VGB

Fig10. Gate1 current as a function of gate2 voltage



f=50MHz, Pin=-30dBm, V_{DS}= 5V, V_{GB}= 5V, R_{GB}=62㏀ T_j = 25 ℃

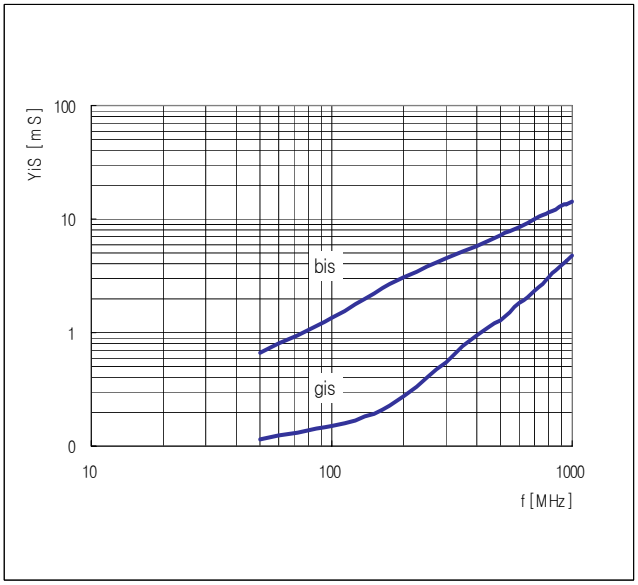
Fig11. Typical Gain reduction as a function of AGC Voltage ; see Fig1



f=50MHz, Pin=-30dBm, V_{DS}= 5V, V_{GB}= 5V, R_{GB}=62㏀

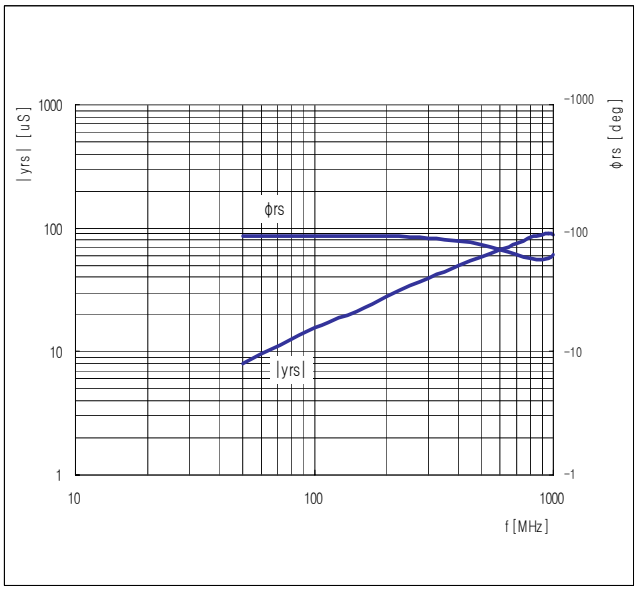
Fig12. Drain current as a function of gain reduction ; see Fig1

☐ Graphs



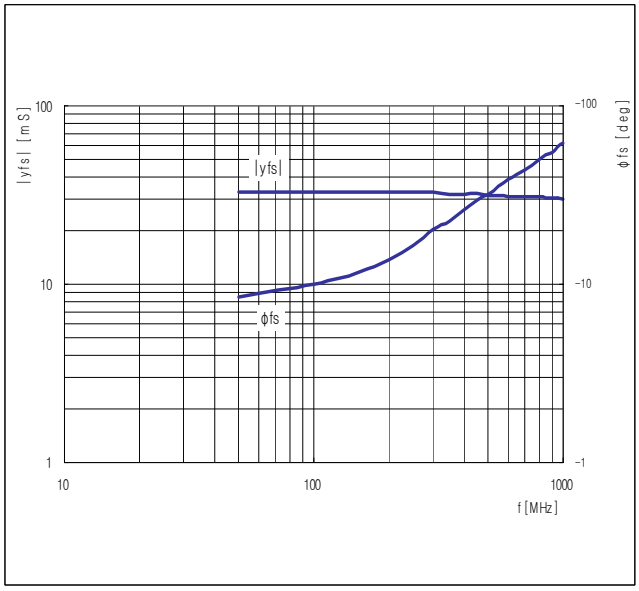
V_{DS}= 5V, V_{G2-S} = 4V

Fig13. Input admittance as a function of frequency



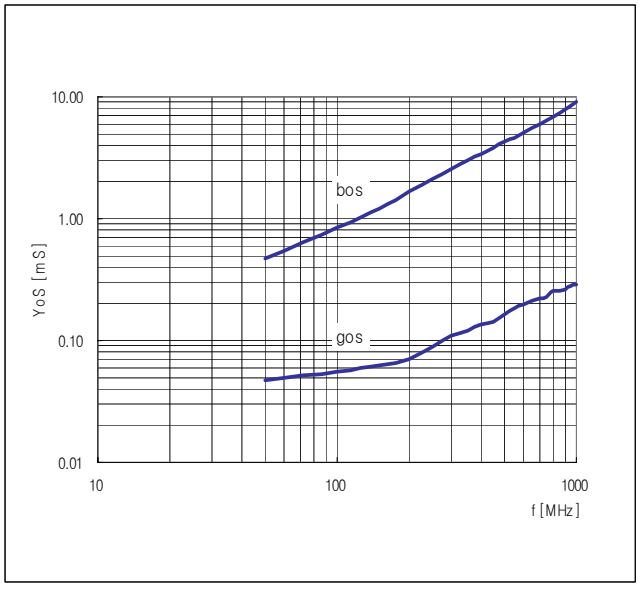
V_{DS}= 5V, V_{G2-S} = 4V

Fig14. Reverse transfer admittance and phase as a function of frequency



V_{DS}= 5V, V_{G2-S} = 4V

Fig15. Forward transfer admittance and phase as a function of frequency

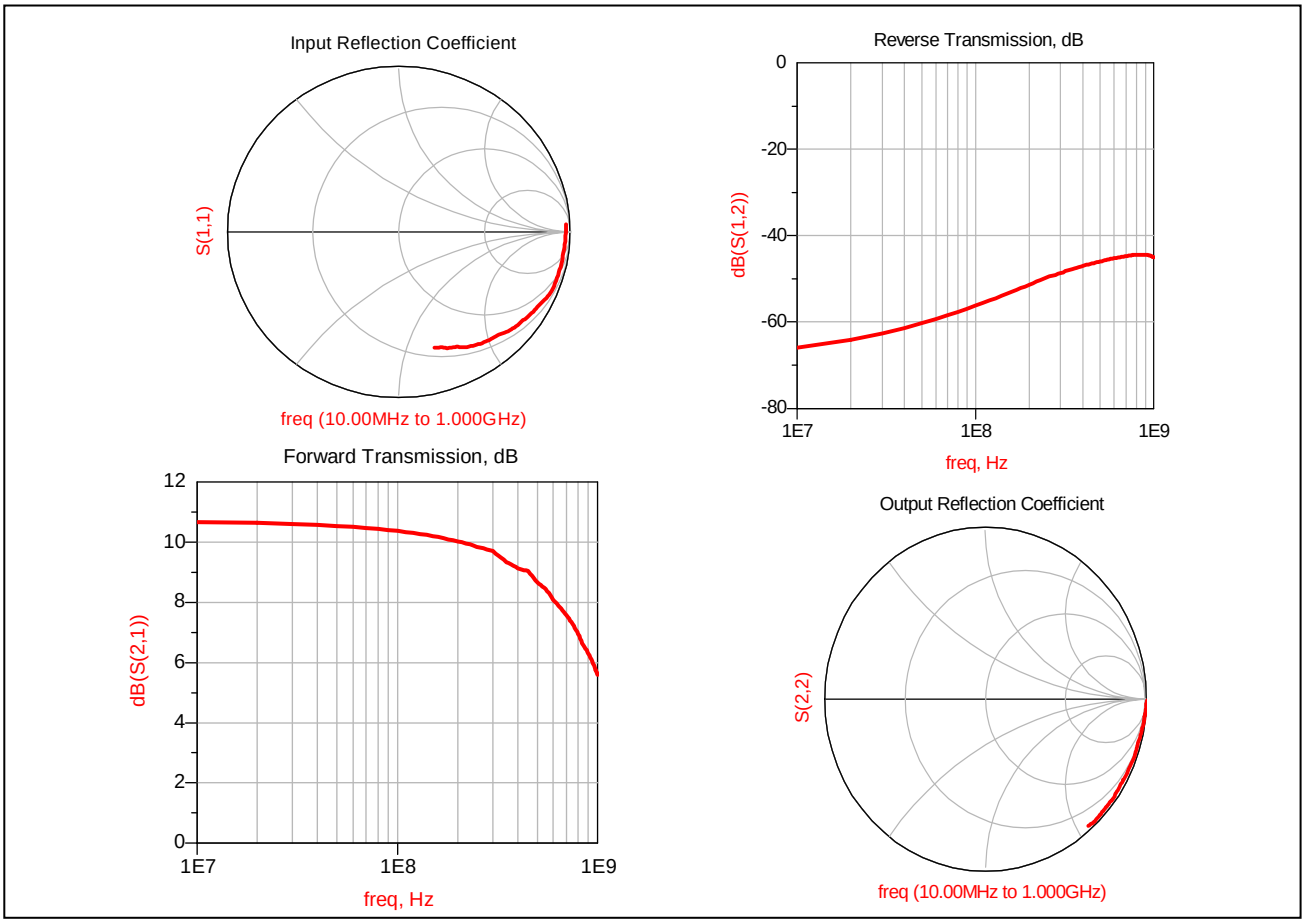


V_{DS}= 5V, V_{G2-S} = 4V

Fig16. Output admittance as a function of frequency

☐ Scattering parameters

(V_{G2-S} = 4V, V_{DS} =5V, I_D =12mA, Ta = 25 ℃)



V_{DS}=5V, V_{G2-S}=4V, I_D=12mA

f (MHz)	S11		S21		S12		S22	
	Magnitude (ratio)	Angle (deg)	Magnitude (ratio)	Angle (deg)	Magnitude (ratio)	Angle (deg)	Magnitude (ratio)	Angle (deg)
50	0.897	0.974	3.93	171.7	0.001	93.0	1.006	-1.86
100	0.915	-5.323	3.81	165.5	0.001	91.7	0.998	-4.89
200	0.952	-17.920	3.58	153.1	0.002	89	0.982	-10.97
300	0.938	-27.300	3.40	141.5	0.002	89.2	0.968	-16.13
400	0.912	-35.160	3.20	130.8	0.003	92.6	0.966	-20.8
500	0.836	-43.000	3.04	120.1	0.004	95.6	0.964	-26.01
600	0.863	-50.800	2.89	110.1	0.004	100.4	0.968	-30.59
700	0.830	-57.600	2.75	98.8	0.004	104.6	0.968	-35.8
800	0.800	-63.470	2.62	87.8	0.004	110.7	0.973	-40.87