

ASYMMETRICAL-BIDIRECTIONAL THYRISTOR SPD



TISP4A270H3BJ LCAS R<sub>LINE</sub> Protector

Optimized LCAS R<sub>LINE</sub> Protector

- TISP4A270H3BJ V<sub>(BO)</sub> Derived from:
  - Break Switch, SW1 & SW2, Ratings
  - Ring Return Switch, SW3, Rating
  - Ringing Access Switch, SW4, Rating
  - Switch Isolation Ratings
  - Battery Voltage Range of -40 V to -60 V
  - Power Fault Conditions
  - Lightning Impulse Conditions
  - LCAS Characteristic Temperature Range

TISP4A270H3BJ Designed for:

- Battery-Backed Ringing Circuits
  - Voltage Swing ..... +148 V to -206 V
  - Allows ..... 103 V rms Ringing with -60 V Battery
  - Temperature Range ..... -40 °C to +85 °C

| Device | V <sub>DRM</sub><br>V | V <sub>(BO)</sub><br>V |
|--------|-----------------------|------------------------|
| '4A270 | +160                  | +217                   |
|        | -222                  | -270                   |

Rated for International Surge Wave Shapes

| Wave Shape | Standard         | I <sub>PPSM</sub><br>A |
|------------|------------------|------------------------|
| 2/10       | GR-1089-CORE     | 500                    |
| 10/700     | ITU-T K.20/45/21 | 150                    |
| 10/1000    | GR-1089-CORE     | 100                    |

..... UL Recognized Components

Description

The TISP4A270H3BJ is an asymmetrical-bidirectional thyristor surge protective device (SPD). It is designed to limit the peak voltages on the R<sub>LINE</sub> (Ring Line) terminal of '7581/2/3 LCAS (Line Card Access Switch) devices. The TISP4A270H3BJ must have the bar-indexed terminal 1 (G) connected to the protective ground and terminal 2 (R) connected to the R<sub>LINE</sub> terminal.

The TISP4A270H3BJ voltages are chosen to give R<sub>LINE</sub> terminal protection for all LCAS switch conditions. The most potentially stressful condition is low level power cross when the switches are closed. Under this condition, the TISP4A270H3BJ limits the voltage and corresponding LCAS dissipation until the LCAS thermal trip operates and opens the switches.

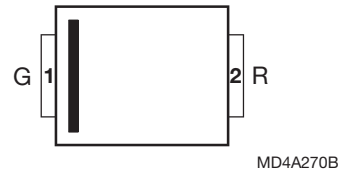
Under open-circuit ringing conditions, the R<sub>LINE</sub> terminal will have high peak voltages. For battery backed ringing, the R<sub>LINE</sub> terminal will have a larger peak negative voltage than positive, i.e. the peak voltages are asymmetric. The TISP4A270H3BJ has a similar voltage asymmetry which will allow the maximum possible ringing voltage, while still giving protection. With a connected telephone line, the LCAS T<sub>LINE</sub> (Tip Line) terminal voltage levels will be less than 50 % of the open-circuit R<sub>LINE</sub> terminal values. So the T<sub>LINE</sub> terminal can be protected by a symmetrical-bidirectional overvoltage protector of the TISP4xxxH3BJ series.

How to Order

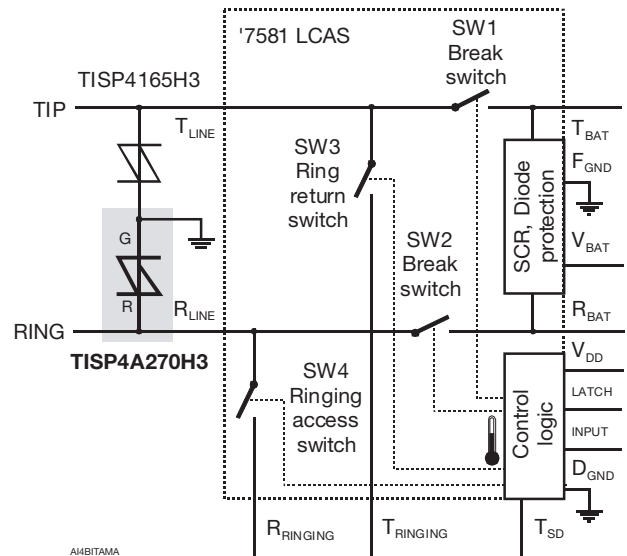
| Device        | Package                       | Carrier                  | For Standard Termination Finish Order As | For Lead Free Termination Finish Order As |
|---------------|-------------------------------|--------------------------|--|---|
| TISP4A270H3BJ | BJ (SMB/DO-214AA with J-Bend) | R (Embossed Tape Reeled) | TISP4A270H3BJR                           | TISP4A270H3BJRS                           |

\*RoHS Directive 2002/95/EC Jan 27 2003 including Annex  
 APRIL 2002 - REVISED FEBRUARY 2005  
 Specifications are subject to change without notice.  
 Customers should verify actual device performance in their specific applications.

SMB Package (Top View)



Device Symbol and Circuit Application



AHBITAMA

## Description (Continued)

These devices allow signal voltages up to the maximum off-state voltage value,  $V_{DRM}$ , see Figure 1. Voltages above  $V_{DRM}$  are clipped and will not exceed the breakover voltage,  $V_{(BO)}$ , level. If sufficient current flows due to the overvoltage, the device switches into a low-voltage on-state condition, which diverts the current from the overvoltage through the device. When the diverted current falls below the holding current,  $I_H$ , level the devices switches off and restores normal system operation.

The TISP4A270H3BJ is guaranteed to voltage limit and withstand the listed international lightning surges in both polarities. This high current protection device is in a plastic SMB package (JEDEC DO-214AA) and supplied in embossed tape reel pack.

## Absolute Maximum Ratings, $T_A = 25\text{ }^\circ\text{C}$ (Unless Otherwise Noted)

| Rating   | Symbol     | Value                 | Unit             |
|--|------------|-----------------------|------------------|
| Repetitive peak off-state voltage, (see Note 1)  | $V_{DRM}$  | +160/-222<br>148/-206 | V                |
| Non-repetitive peak on-state pulse current (see Notes 2 and 3)                                 | $I_{PPSM}$ | 500                   | A                |
| 2/10 (GR-1089-CORE, 2/10 voltage wave shape)   |            | 150                   |                  |
| 5/310 (ITU-T K.44, 10/700 $\mu\text{s}$ voltage wave shape used in K.20/45/21)                 |            | 100                   |                  |
| Non-repetitive peak on-state current (see Notes 2, 3 and 4)                                    | $I_{TSM}$  | 55                    | A                |
| 20 ms (50 Hz) full sine wave   |            | 60                    |                  |
| 16.7 ms (60 Hz) full sine wave   |            | 2.2                   |                  |
| 1000 s 50 Hz/60 Hz a.c.  |            |                       |                  |
| Initial rate of rise of on-state current, Exponential current ramp, Maximum ramp value < 200 A | $di_T/dt$  | 400                   | A/ $\mu\text{s}$ |
| Junction temperature   | $T_J$      | -40 to +150           | $^\circ\text{C}$ |
| Storage temperature range  | $T_{stg}$  | -65 to +150           | $^\circ\text{C}$ |

- NOTES: 1. See Figure 7 for voltage values at intermediate temperatures.  
 2. Initially, the TISP4A270H3BJ must be in thermal equilibrium with  $T_J = 25\text{ }^\circ\text{C}$ .  
 3. The surge may be repeated after the TISP4A270H3BJ returns to its initial conditions.  
 4. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. See Figure 6 for the current ratings at other durations. Derate current values at  $-0.61\text{ }^\circ\text{C}$  for ambient temperatures above  $25\text{ }^\circ\text{C}$ .

## Overload Ratings, $T_A = 25\text{ }^\circ\text{C}$ (Unless Otherwise Noted)

| Rating  | Symbol       | Value | Unit  |
|---|--------------|-------|-------|
| Maximum overload on-state current without open circuit, 50 Hz/60 Hz a.c. (see Note 5) | $I_{T(OV)M}$ | 60    | A rms |
| 0.03 s  |              | 40    |       |
| 0.07 s  |              | 8     |       |
| 1.6 s   |              | 7     |       |
| 5.0 s   |              | 2.2   |       |
| 1000 s  |              |       |       |

- NOTE 5: Peak overload on-state current during a.c. power cross tests of GR-1089-CORE and UL 1950/60950. These electrical stress levels may damage the TISP4A270H3BJ silicon chip. After test, the pass criterion is either that the device is functional or, if it is faulty, that it has a short circuit fault mode. In the short circuit fault mode, the following equipment is protected as the device is a permanent short across the line. The equipment would be unprotected if an open circuit fault mode developed.

## Electrical Characteristics, T<sub>A</sub> = 25 °C (Unless Otherwise Noted)

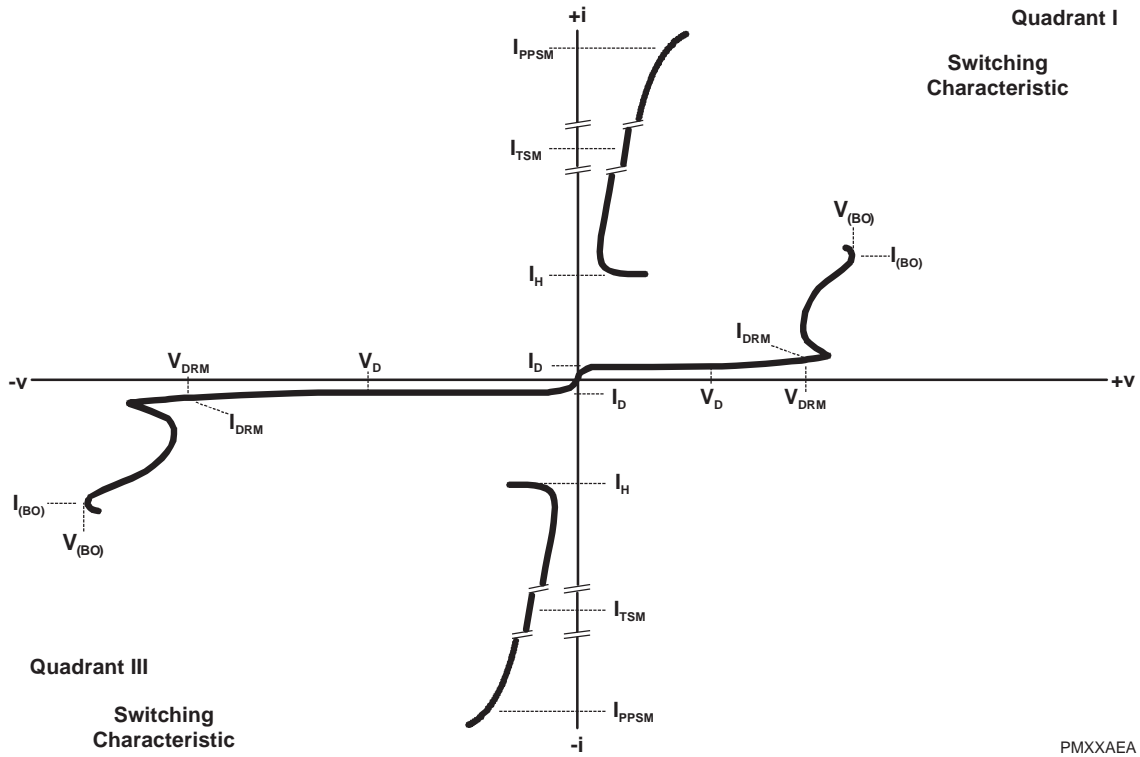
| Parameter  | Test Conditions   | Min   | Typ  | Max  | Unit  |
|--|---|-------|--|--|-------|
| I <sub>DRM</sub> Repetitive peak off-state current | V <sub>D</sub> = +100 V and -200 V<br>T <sub>A</sub> = 25 °C<br>T <sub>A</sub> = 85 °C  |       |  | ±5<br>±10  | μA    |
| V <sub>(BO)</sub> Breakover voltage                | dv/dt = ±250 V/ms, R <sub>SOURCE</sub> = 300 Ω  |       |  | +217<br>-270   | V     |
| V <sub>(BO)</sub> Ramp breakover voltage           | dv/dt ≤ ±1 kV/μs, Linear voltage ramp, Maximum ramp value = ±500 V<br>dv/dt = ±20 A/μs, Linear current ramp, Maximum ramp value = ±10 A   |       |  | +231<br>-288   | V     |
| I <sub>(BO)</sub> Breakover current                | dv/dt = ±250 V/ms, R <sub>SOURCE</sub> = 300 Ω  | ±0.15 |  | ±0.6   | A     |
| I <sub>H</sub> Holding current                     | I <sub>T</sub> = ±5 A, di/dt = +/-30 mA/ms  | ±0.15 |  | ±0.6   | A     |
| dv/dt Critical rate of rise of off-state voltage   | Linear voltage ramp, Maximum ramp value < 0.85V <sub>DRM</sub>  | ±5    |  |  | kV/μs |
| I <sub>D</sub> Off-state current                   | V <sub>D</sub> = ±50 V<br>T <sub>A</sub> = 85 °C  |       |  | ±10  | μA    |
| C <sub>off</sub> Off-state capacitance             | f = 1 MHz, V <sub>d</sub> = 1 V rms<br>V <sub>D</sub> = 100 V<br>V <sub>D</sub> = 50 V<br>V <sub>D</sub> = 10 V<br>V <sub>D</sub> = 5 V<br>V <sub>D</sub> = 2 V<br>V <sub>D</sub> = 1 V<br>V <sub>D</sub> = 0<br>V <sub>D</sub> = -1 V<br>V <sub>D</sub> = -2 V<br>V <sub>D</sub> = -5 V<br>V <sub>D</sub> = -10 V<br>V <sub>D</sub> = -50 V<br>V <sub>D</sub> = -100 V |       | 21<br>27<br>41<br>48<br>56<br>61<br>68<br>62<br>56<br>48<br>40<br>25<br>20 | 23<br>29<br>46<br>53<br>62<br>67<br>74<br>68<br>62<br>52<br>45<br>28<br>22 | pF    |

## Thermal Characteristics

| Parameter  | Test Conditions   | Min | Typ | Max | Unit |
|--|---|-----|-----|-----|------|
| R <sub>θJA</sub> Junction to free air thermal resistance | EIA/JESD51-3 PCB, I <sub>T</sub> = I <sub>TSM(1000)</sub> ,<br>T <sub>A</sub> = 25 °C, (see Note 6)                   |     |     | 113 | °C/W |
|  | 265 mm x 210 mm populated line card,<br>4-layer PCB, I <sub>T</sub> = I <sub>TSM(1000)</sub> , T <sub>A</sub> = 25 °C |     | 50  |     |      |

NOTE 6: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

Parameter Measurement Information



PMXXAEA

Figure 1. Voltage-Current Characteristic for R and G Terminal Pair  
All Measurements are Referenced to the G Terminal

## Typical Characteristics

**OFF-STATE CURRENT  
vs  
JUNCTION TEMPERATURE**

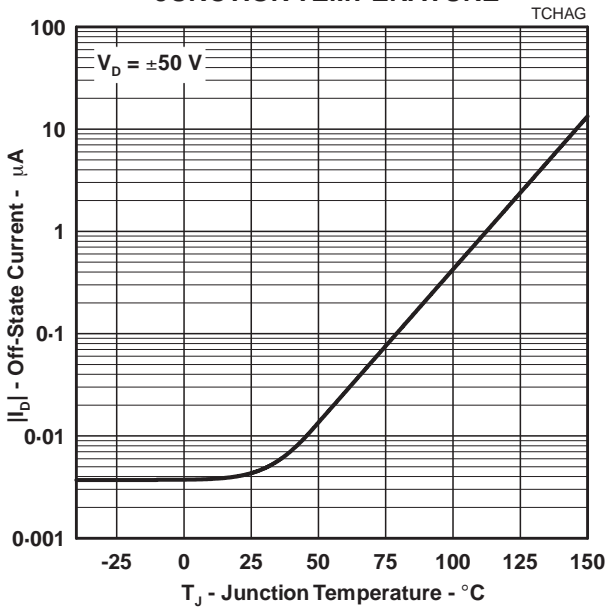


Figure 2.

**NORMALIZED BREAKOVER VOLTAGE  
vs  
JUNCTION TEMPERATURE**

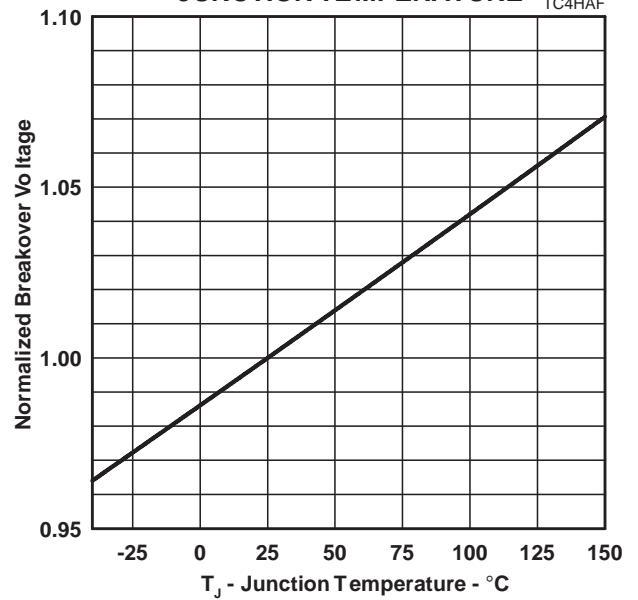


Figure 3.

**ON-STATE CURRENT  
vs  
ON-STATE VOLTAGE**

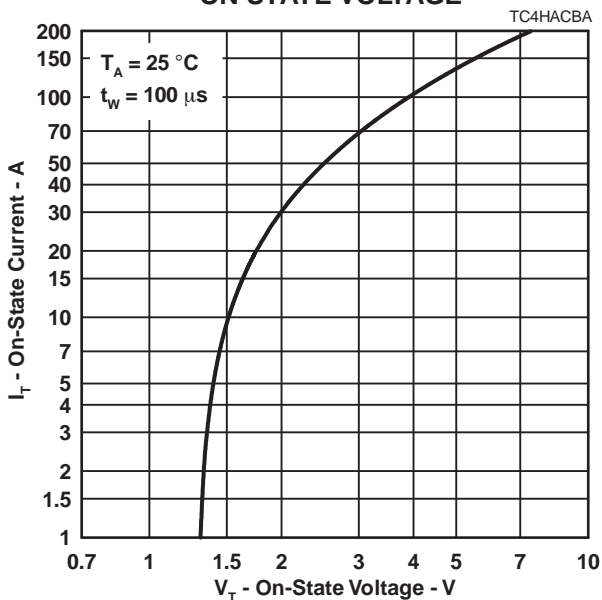


Figure 4.

**NORMALIZED HOLDING CURRENT  
vs  
JUNCTION TEMPERATURE**

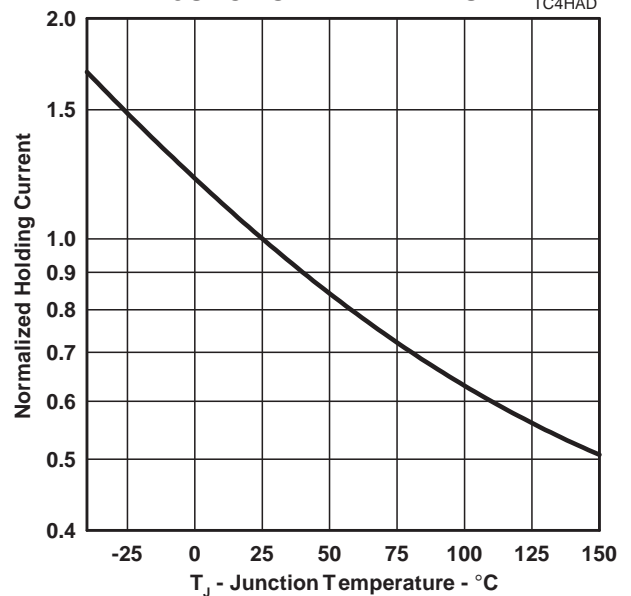


Figure 5.

## Rating and Thermal Information

### NON-REPETITIVE PEAK ON-STATE CURRENT VS CURRENT DURATION

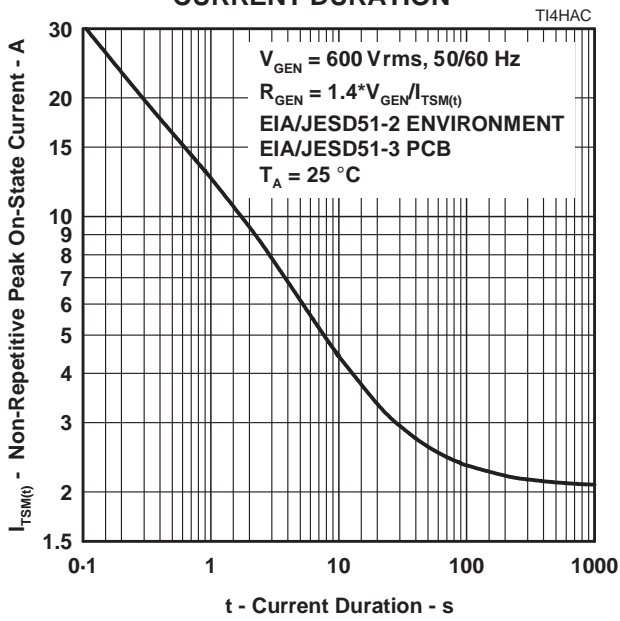


Figure 6.

### V<sub>DRM</sub> DERATING FACTOR VS MINIMUM AMBIENT TEMPERATURE

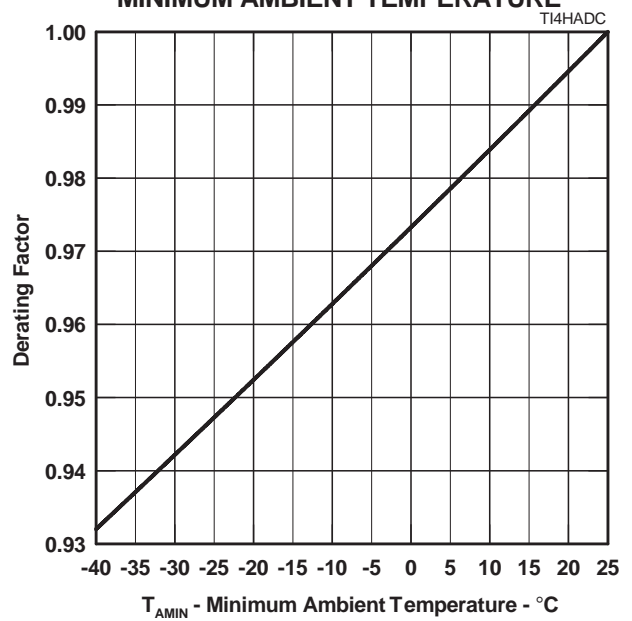
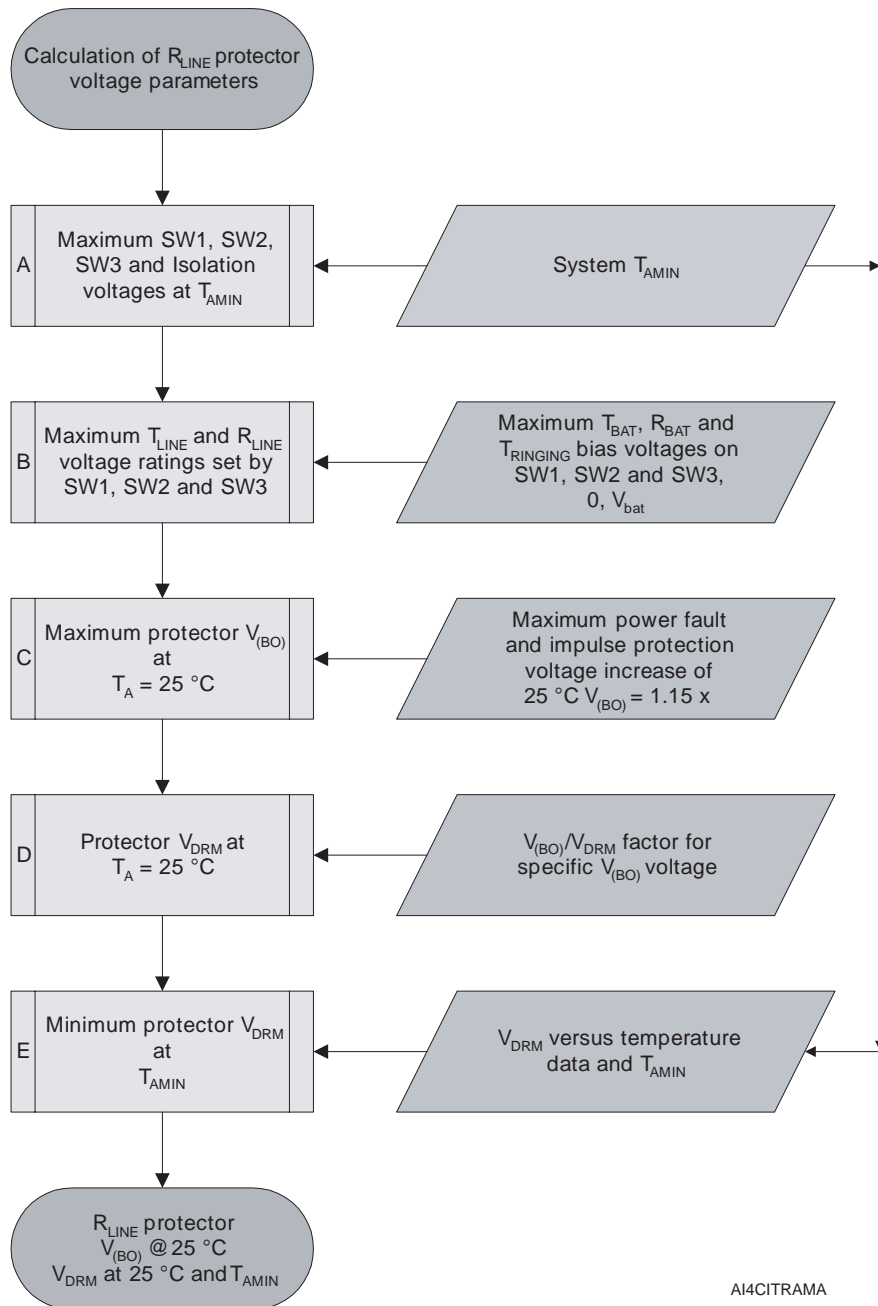


Figure 7.

## APPLICATIONS INFORMATION

### Calculation of the TISP4A270H3BJ Voltage Values

Figure 8 and the following text summarizes the derivation process for the TISP4A270H3BJ voltages. Details of the full process and other design aspects are covered by the document entitled *TISP4A270H3BJ - Optimized '758x LCAS Overvoltage Protection*.



AI4CITRAMA

Figure 8. Derivation of TISP4A270H3BJ V<sub>(BO)</sub> and V<sub>DRM</sub>

# TISP4A270H3BJ LCAS R<sub>LINE</sub> Protector

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## Calculation of the TISP4A270H3BJ Voltage Values (Continued)

**Box A:** The voltage rating of the break and ring return switches and their isolation decreases with temperature. At the minimum LCAS operating temperature of -40 °C, the switch rating is ±310 V.

**Box B:** A switch pole voltage rating to ground is reduced by any opposing bias voltage applied to the other pole. For battery-backed ringing the d.c. bias on T<sub>RINGING</sub> is zero. Bias voltages are applied to the R<sub>BAT</sub> and T<sub>BAT</sub> poles by the SLIC. For SLIC output levels of zero and -60 V, the R<sub>LINE</sub> and T<sub>LINE</sub> voltage ratings to ground become +250 V and -310 V at -40 °C.

**Box C:** Allowing for the extreme condition of a power fault at -40 °C, the overvoltage protector V<sub>(BO)</sub> at its highest temperature must not exceed +250 V and -310 V. The IEEE Standard C62.37.1-2000, IEEE Guide for the Application of Thyristor Surge Protective Devices, pp 25-27 recommends a factor of 1.15 for the ratio of the power fault V<sub>(BO)</sub> to the 25 °C V<sub>(BO)</sub>. Applying this factor makes the 25 °C V<sub>(BO)</sub> voltage values +217 V and -270 V.

**Box D:** From the V<sub>(BO)</sub> values the values of protector 25 °C V<sub>DRM</sub> were determined as +160 V and -222 V.

**Box E:** Derating the 25 °C V<sub>DRM</sub> down to the LCAS minimum operating temperature gives -40 °C V<sub>DRM</sub> values of +148 V and -206 V. A further rating check has to be done on the ringing access switch, SW4. The limit condition is in the negative ringing polarity. The applied ringing voltage to the R<sub>RINGING</sub> terminal must not exceed -205 V when the R<sub>LINE</sub> terminal is at +250 V. For a battery voltage of -40 V and -60 V the a.c. ringing levels must not exceed 117 V rms and 102 V rms respectively. In IVD (Integrated Voice Data) applications the a.c. ringing level must be reduced by the level of digital signal applied to the line. For a 20 V peak ADSL signal level, the ringing voltages reduce to 103 V rms and 89 V rms respectively.

Figure 9 shows a typical application circuit. Fuses F1 and F2 need high breaking capacity to safely interrupt 40 A rms (UL 60950) and 60 A rms (Telcordia GR-1089-CORE) currents from a 600 V rms source. The Bourns® Telefuse™ type B1250T is a surface mount fuse which has UL recognition for these UL and Telcordia standards. The TISP4A270H3BJ is overload rated to carry currents up to 60 A rms for the time period that it takes the fuse to operate.

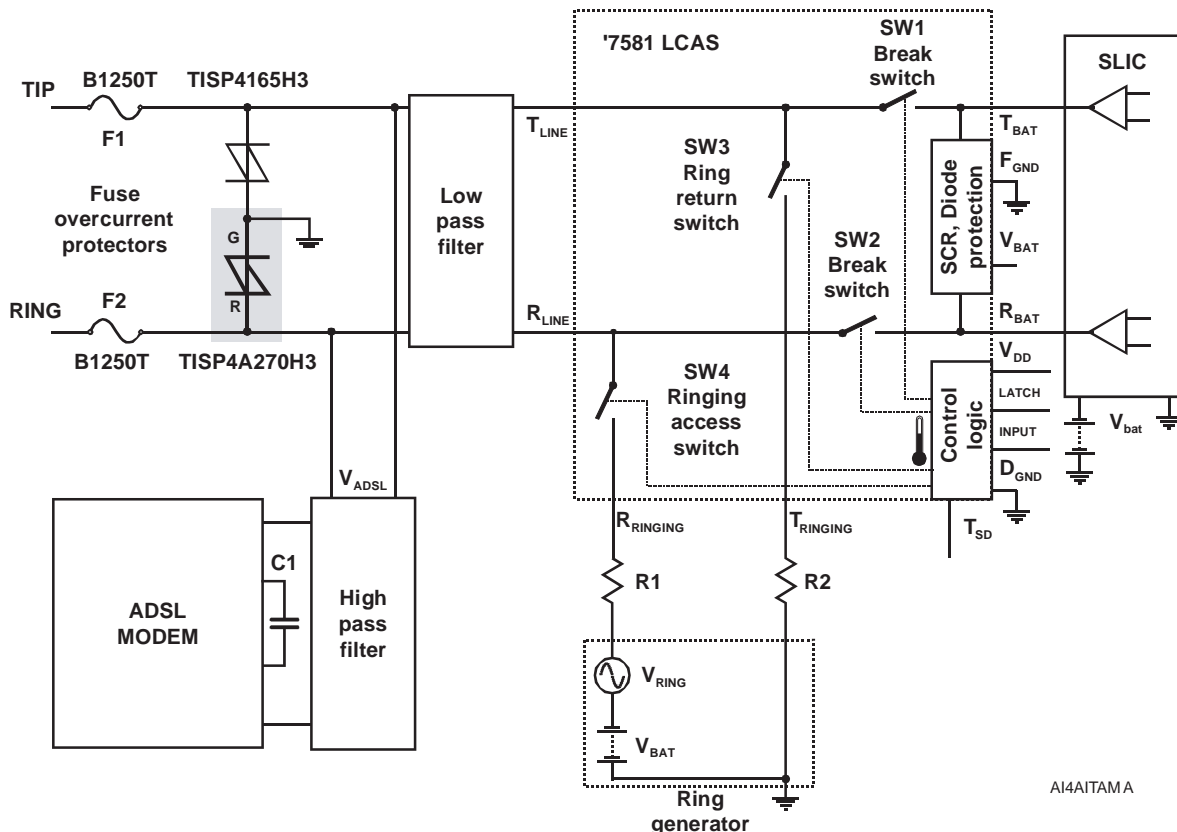
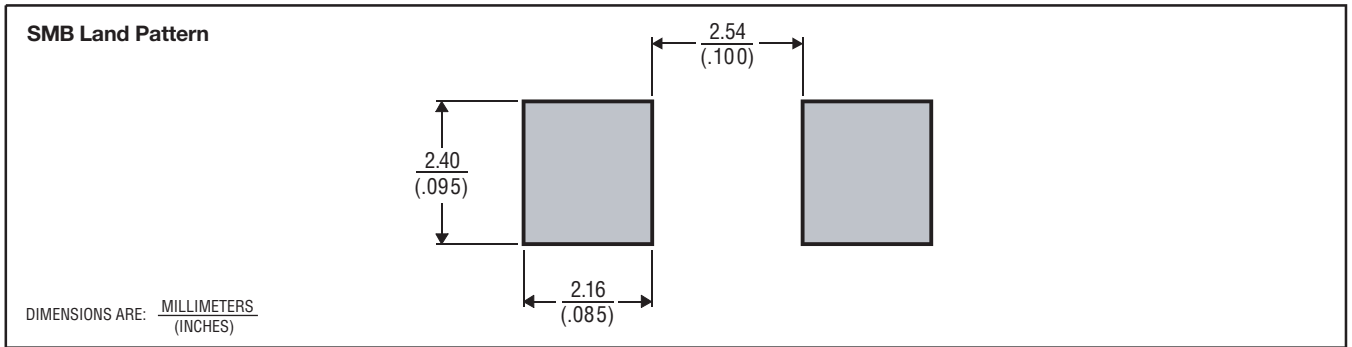


Figure 9. ADSL IVD using Common Protection



## MECHANICAL DATA

### Recommended Printed Wiring Land Pattern Dimensions



MDXXBID

### Device Symbolization Code

Devices will be coded as below. Terminal 1 is indicated by an adjacent bar marked on the package body.

| Device        | Symbolization Code |
|---------------|--------------------|
| TISP4A270H3BJ | 4A270H             |

### Carrier Information

For production quantities, the carrier will be embossed tape reel pack. Evaluation quantities may be shipped in bulk pack or embossed tape.

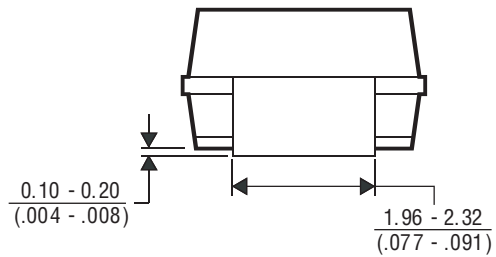
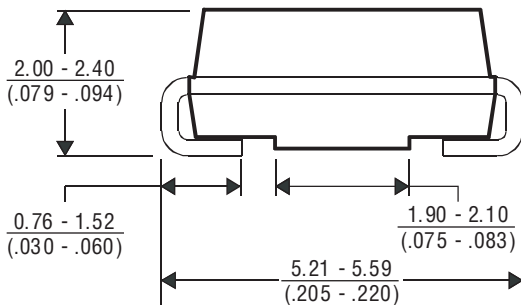
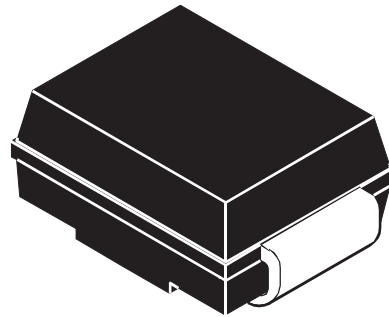
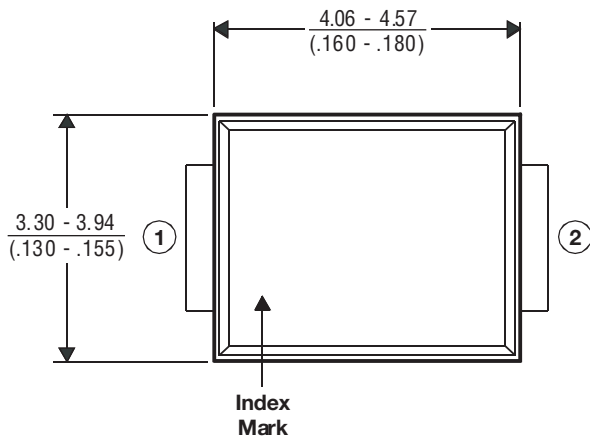
| Package | Carrier                 | Standard Quantity |
|---------|-------------------------|-------------------|
| SMB     | Embossed Tape Reel Pack | 3000              |

MECHANICAL DATA

SMB (DO-214AA) Plastic Surface Mount Diode Package

This surface mount package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

SMB02



DIMENSIONS ARE:  $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$

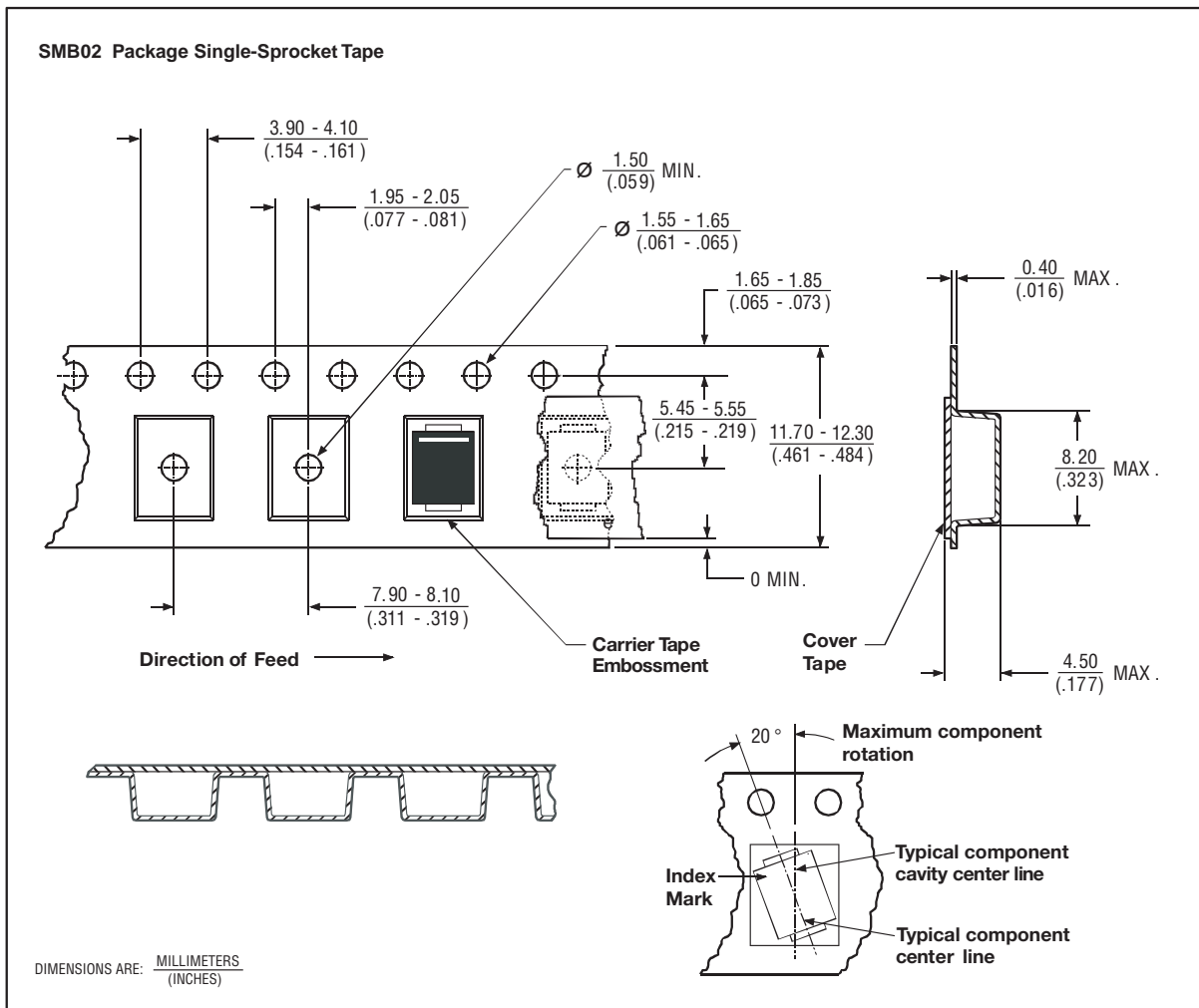
MDXXBHG

# TISP4A270H3BJ LCAS R<sub>LINE</sub> Protector

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## MECHANICAL DATA

### Tape Dimensions



NOTES: A. The clearance between the component and the cavity must be within 0.05 mm (.002 in) MIN. to 0.65 mm (.026 in) MAX. so that the component cannot rotate more than 20° within the determined cavity.

MDXXBHF

B. Taped devices are supplied on a reel of the following dimensions:-

Reel diameter: 330 mm ± 3.0 mm (12.99 in ± .118 in)  
 Reel hub diameter: 75 mm (2.95 in) MIN.  
 Reel axial hole: 13.0 mm ± 0.5 mm (.512 in ± .020 in)

C. 3000 devices are on a reel.

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